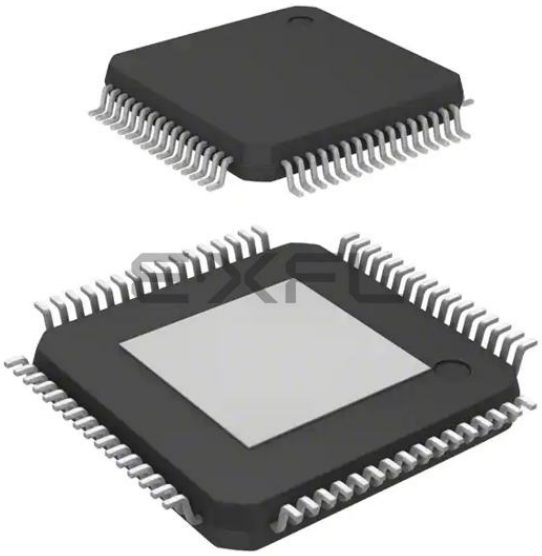
Infineon Technologies - XE162HN24F80LAAFXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	40
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	26K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe162hn24f80laafxuma1

16-Bit

Architecture

XE162FN, XE162HN

16-Bit Single-Chip
Real Time Signal Controller
XE166 Family / Value Line

Data Sheet

V1.5 2013-02

Microcontrollers

XE162xN Data Sheet
Revision History: V1.5 2013-02

Previous Versions:
V1.4, 2011-07
V1.3, 2010-04
V1.2, 2009-07
V1.1, 2009-07
V1.0, 2009-03 Preliminary

Page	Subjects (major changes since last revision)
26	Added AB step marking.
76	Errata SWD_X.P002 implemented: V_{SWD} tolerance boundaries for 5.5 V are changed.
78	Clarified “Coding of bit fields LEVxV” descriptions. Matched with Operating Conditions: marked some coding values “out of valid operation range”.
79	Errata FLASH_X.P001 implemented: Test Condition for Flash parameter N_{ER} corrected

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1.2 Definition of Feature Variants

The XE162xN types are offered with several Flash memory sizes. **Table 2** and **Table 3** describe the location of the available Flash memory.

Table 2 Continuous Flash Memory Ranges

Total Flash Size	1st Range[1)]	2nd Range	3rd Range
320 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C4'FFFF_H$	n.a.
192 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C1'FFFF_H$	$C4'0000_H$ … $C4'FFFF_H$
128 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C4'0000_H$ … $C4'FFFF_H$	n.a.

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

Table 3 Flash Memory Module Allocation (in Kbytes)

Total Flash Size	Flash 0[1)]	Flash 1
320	256	64
192	128	64
128	64	64

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

The XE162xN types are offered with different interface options. **Table 4** lists the available channels for each option.

Table 4 Interface Channel Association

Total Number	Available Channels / Message Objects
7 ADC0 channels	CH0, CH2, Ch4, CH8, CH10, CH13, CH15
2 ADC1 channels	CH0, CH4
2 CAN nodes	CAN0, CAN1 64 message objects
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1

The XE162xN types are offered with several SRAM memory sizes. **Figure 1** shows the allocation rules for PSRAM and DSRAM. Note that the rules differ:

- PSRAM allocation starts from the **lower** address
- DSRAM allocation starts from the **higher** address

For example 8 Kbytes of PSRAM will be allocated at E0’0000h-E0’1FFFh and 8 Kbytes of DSRAM will be at 00’C000h-00’DFFFh.

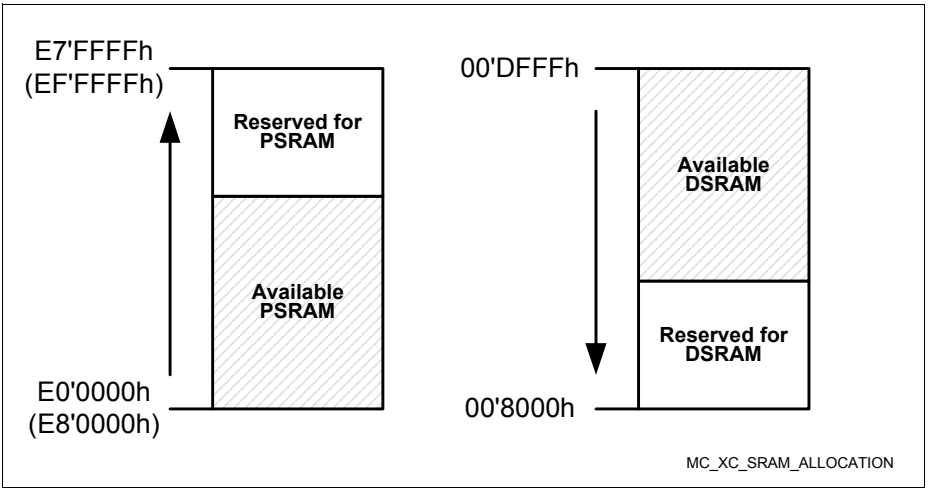

Figure 1 SRAM Allocation

2 General Device Information

The XE162xN series (16-Bit Single-Chip
Real Time Signal Controller) is a part of the Infineon XE166 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 80 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

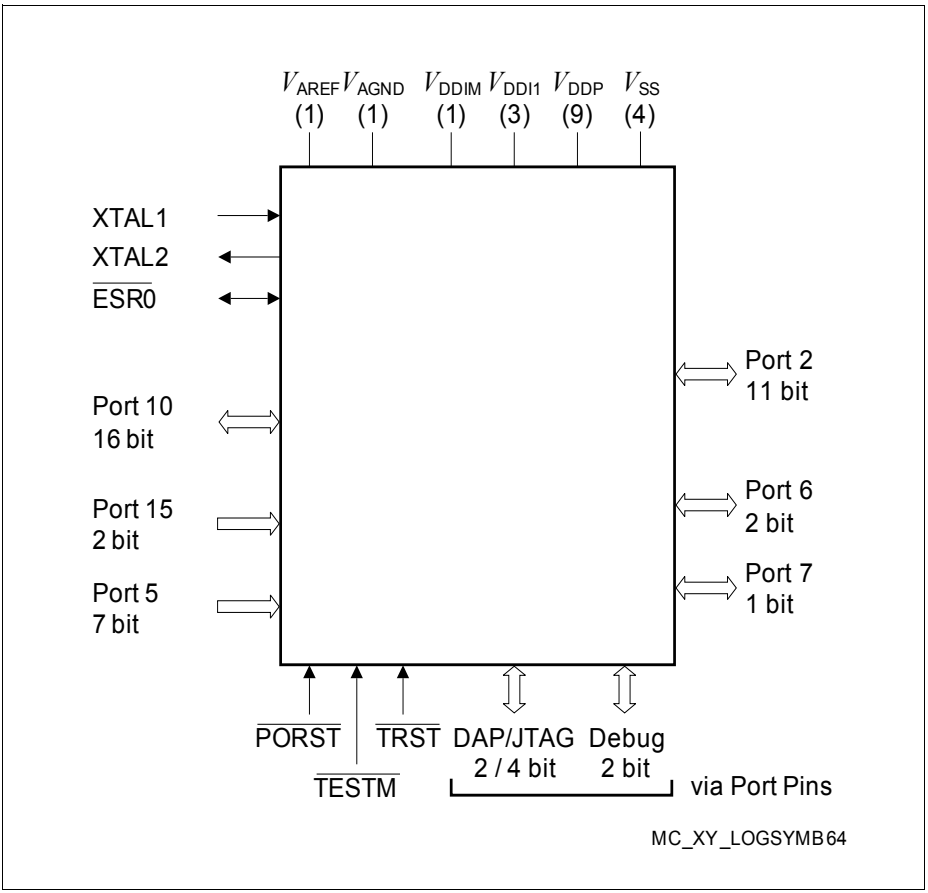

Figure 2 XE162xN Logic Symbol

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
35	P2.7	O0 / I	St/B	**Bit 7 of Port 2, General Purpose Input/Output**
	U0C1_SELO 0	O1	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	U0C0_SELO 1	O2	St/B	**USIC0 Channel 0 Select/Control 1 Output**
	CC2_CC20	O3 / I	St/B	**CAPCOM2 CC20IO Capture Inp./ Compare Out.**
	U0C1_DX2C	I	St/B	**USIC0 Channel 1 Shift Control Input**
	RxDC1C	I	St/B	**CAN Node 1 Receive Data Input**
	ESR2_7	I	St/B	**ESR2 Trigger Input 7**
36	P2.8	O0 / I	DP/B	**Bit 8 of Port 2, General Purpose Input/Output**
	U0C1_SCLK OUT	O1	DP/B	**USIC0 Channel 1 Shift Clock Output**
	EXTCLK	O2	DP/B	**Programmable Clock Signal Output**
	CC2_CC21	O3 / I	DP/B	**CAPCOM2 CC21IO Capture Inp./ Compare Out.**
	U0C1_DX1D	I	DP/B	**USIC0 Channel 1 Shift Clock Input**
37	P2.9	O0 / I	St/B	**Bit 9 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	TxDC1	O2	St/B	**CAN Node 1 Transmit Data Output**
	CC2_CC22	O3 / I	St/B	**CAPCOM2 CC22IO Capture Inp./ Compare Out.**
	CLKIN1	I	St/B	**Clock Signal Input 1**
	TCK_A	IH	St/B	**DAP0/JTAG Clock Input** If JTAG pos. A is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 0 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
55	P10.12	O0 / I	St/B	**Bit 12 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	TDO_B	OH / IH	St/B	**JTAG Test Data Output / DAP1 Input/Output** If DAP pos. 1 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	U1C0_DX0C	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX1E	I	St/B	**USIC1 Channel 0 Shift Clock Input**
56	P10.13	O0 / I	St/B	**Bit 13 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	U1C0_SELO 3	O3	St/B	**USIC1 Channel 0 Select/Control 3 Output**
	U1C0_DX0D	I	St/B	**USIC1 Channel 0 Shift Data Input**
58	P10.14	O0 / I	St/B	**Bit 14 of Port 10, General Purpose Input/Output**
	U1C0_SELO 1	O1	St/B	**USIC1 Channel 0 Select/Control 1 Output**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	ESR2_2	I	St/B	**ESR2 Trigger Input 2**
	U0C1_DX0C	I	St/B	**USIC0 Channel 1 Shift Data Input**
59	P10.15	O0 / I	St/B	**Bit 15 of Port 10, General Purpose Input/Output**
	U1C0_SELO 2	O1	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U1C0_DOUT	O3	St/B	**USIC1 Channel 0 Shift Data Output**
	U0C1_DX1C	I	St/B	**USIC0 Channel 1 Shift Clock Input**
60	XTAL2	O	Sp/M	**Crystal Oscillator Amplifier Output**
61	XTAL1	I	Sp/M	**Crystal Oscillator Amplifier Input** To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Voltages on XTAL1 must comply to the core supply voltage V_{DDIM}.
	ESR2_9	I	St/B	**ESR2 Trigger Input 9**

With this hardware most XE162xN instructions are executed in a single machine cycle of 12.5 ns @ 80-MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle, no matter how many bits are shifted. Also, multiplication and most MAC instructions execute in one cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast; for example, a 32-/16-bit division is started within 4 cycles while the remaining cycles are executed in the background. Another pipeline optimization, the branch target prediction, eliminates the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 word-wide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank accessed by the CPU at any time. The number of these register bank copies is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided for storage of temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area); it is accessed by the CPU with the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared with the stack pointer value during each stack access to detect stack overflow or underflow.

The high performance of the CPU hardware implementation can be best utilized by the programmer with the highly efficient XE162xN instruction set. This includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The counting direction (up/down) for each timer can be programmed by software or altered dynamically with an external signal on a port pin (TxEUD). Concatenation of the timers is supported with the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can also be used to clock the CAPCOM2 timers and to initiate a reload from the CAPREL register.

The CAPREL register can capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN); timer T5 may optionally be cleared after the capture procedure. This allows the XE162xN to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) can also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time-based interrupt, to provide a system time tick independent of CPU frequency and other resources
- 48-bit timer for long-term measurements
- Alarm interrupt at a defined time

3.12 Universal Serial Interface Channel Modules (USIC)

The XE162xN features the USIC modules USIC0, USIC1, USIC2. Each module provides two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent of the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit. The inputs and outputs of each USIC channel can be assigned to different interface pins, providing great flexibility to the application software. All assignments can be made during runtime.

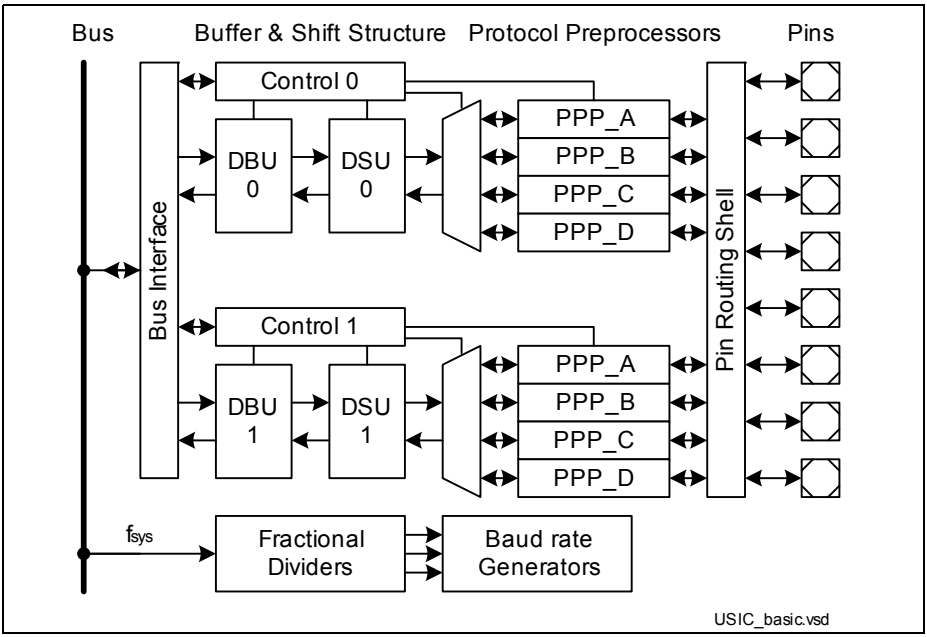

Figure 11 General Structure of a USIC Module

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols with improved performances (baud rate, buffer handling)

MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Independent CAN nodes
- Set of independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

3.14 System Timer

The System Timer consists of a programmable prescaler and two concatenated timers (10 bits and 6 bits). Both timers can generate interrupt requests. The clock source can be selected and the timers can also run during power reduction modes.

Therefore, the System Timer enables the software to maintain the current time for scheduling functions or for the implementation of a clock.

3.15 Watchdog Timer

The Watchdog Timer is one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after an application reset of the chip. It can be disabled and enabled at any time by executing the instructions DISWDT and ENWDT respectively. The software has to service the Watchdog Timer before it overflows. If this is not the case because of a hardware or software failure, the Watchdog Timer overflows, generating a prewarning interrupt and then a reset request.

The Watchdog Timer is a 16-bit timer clocked with the system clock divided by 16,384 or 256. The Watchdog Timer register is set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the Watchdog Timer is reloaded and the prescaler is cleared.

Time intervals between 3.2 μs and 13.4 s can be monitored (@ 80 MHz).

The default Watchdog Timer interval after power-up is 6.5 ms (@ 10 MHz).

3.17 Parallel Ports

The XE162xN provides up to 40 I/O lines which are organized into 4 input/output ports and 2 input ports. All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, activation of pull devices, and edge characteristics (shape) and driver characteristics (output current) of the port drivers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

All port lines have alternate input or output functions associated with them. These alternate functions can be programmed to be assigned to various port pins to support the best utilization for a given application. For this reason, certain functions appear several times in **Table 9**.

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

Table 9 Summary of the XE162xN's Ports

Port	Width	I/O	Connected Modules
P2	11	I/O	CAN, CC2, GPT12E, USIC, DAP/JTAG
P5	7	I	Analog Inputs, CCU6, DAP/JTAG, GPT12E, CAN
P6	2	I/O	ADC, CAN, GPT12E
P7	1	I/O	CAN, GPT12E, SCU, DAP/JTAG, USIC
P10	16	I/O	CCU6, USIC, DAP/JTAG, CAN
P15	2	I	Analog Inputs, GPT12E

Table 10 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

1) The Enter Power Down Mode instruction is not used in the XE162xN, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

Note: A fraction of the leakage current flows through domain DMP_A (pin V_{DDPA}). This current can be calculated as 7,000 $\times$ $e^{-\alpha}$, with α = 5000 / (273 + 1.3 $\times$ T_J). For T_J = 150°C, this results in a current of 160 μA.

Leakage Power Consumption Calculation

The leakage power consumption can be calculated according to the following formula:

$I_{LK1} = 530{,}000 \times e^{-\alpha}$ with $\alpha = 5000 / (273 + B \times T_J)$

Parameter B must be replaced by

- 1.0 for typical values
- 1.3 for maximum values

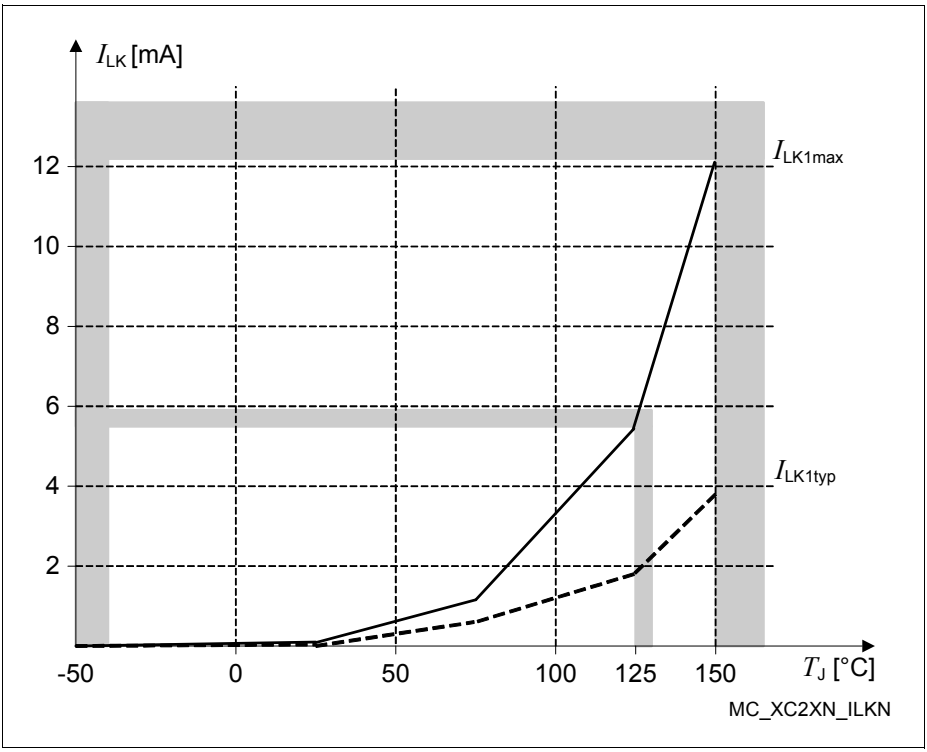

Figure 15 Leakage Supply Current as a Function of Temperature

1) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF}. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1}.
2) Overload conditions must not occur on pin XTAL1.

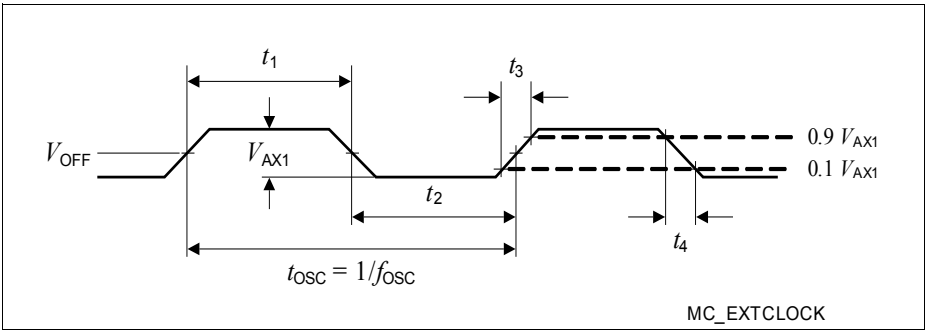

Figure 21 External Clock Drive XTAL1

Note: For crystal or ceramic resonator operation, it is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for oscillator operation.
The manufacturers of crystals and ceramic resonators offer an oscillator evaluation service. This evaluation checks the crystal/resonator specification limits to ensure a reliable oscillator operation.

Table 28 Standard Pad Parameters for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise and Fall times (10% - 90%)	t_{RF} CC	–	–	37 + 0.65 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Medium
		–	–	24 + 0.3 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Medium
		–	–	6.2 + 0.24 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Sharp
		–	–	34 + 0.3 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Slow
		–	–	500 + 2.5 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Weak

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and Σ-I_{OH}) must remain below 50 mA.

Table 36 JTAG Interface Timing for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	
TDO valid from TCK falling edge (propagation delay)[1]	t_8 CC	–	32	36	ns	
TDO high impedance to valid output from TCK falling edge[2][1]	t_9 CC	–	32	36	ns	
TDO valid output to high impedance from TCK falling edge[1]	t_{10} CC	–	32	36	ns	
TDO hold after TCK falling edge[1]	t_{18} CC	5	–	–	ns	

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

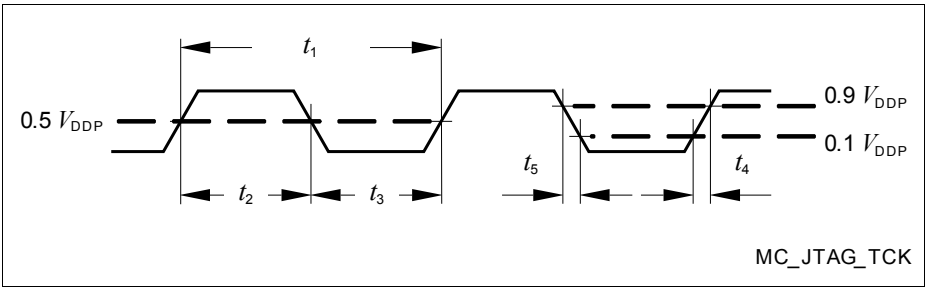

Figure 26 Test Clock Timing (TCK)

5 Package and Reliability

The XE166 Family devices use the package type PG-LQFP (Plastic Green - Low Profile Quad Flat Package). The following specifications must be regarded to ensure proper integration of the XE162xN in its target environment.

5.1 Packaging

These parameters specify the packaging rather than the silicon.

Table 37 Package Parameters (PG-LQFP-64-6)

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Exposed Pad Dimension	Ex × Ey	–	5.6 × 5.6	mm	–
Power Dissipation	P_{DISS}	–	0.8	W	–
Thermal resistance Junction-Ambient	$R_{\Theta JA}$	–	40	K/W	No thermal via[1)]
			37	K/W	4-layer, no pad[2)]
			25	K/W	4-layer, pad[3)]

1) Device mounted on a 4-layer board without thermal vias; exposed pad not soldered.

2) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad not soldered.

3) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad soldered to the board.

Note: To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground, independent of the thermal requirements.
Board layout examples are given in an application note.

Package Compatibility Considerations

The XE162xN is a member of the XE166 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Pad (if present) may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

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