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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	40
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe162hn40f80laakxuma1

Summary of Features

1.1 Device Types

The following XE162xN device types are available and can be ordered through Infineon's direct and/or distribution channels. The devices are available for the SAF temperature range. SAK types are available upon request only.

Table 1 Synopsis of XE162xN Device Types

Derivative	Flash Memory¹⁾	PSRAM DSRAM²⁾	Capt./Comp. Modules	ADC³⁾ Chan.	Interfaces³⁾
XE162FN-16F80L	128 Kbytes	8 Kbytes 8 Kbytes	CC2 CCU60	7 + 2	2 CAN Node, 6 Serial Chan.
XE162FN-24F80L	192 Kbytes	8 Kbytes 16 Kbytes	CC2 CCU60	7 + 2	2 CAN Node, 6 Serial Chan.
XE162FN-40F80L	320 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60	7 + 2	2 CAN Node, 6 Serial Chan.
XE162HN-16F80L	128 Kbytes	8 Kbytes 8 Kbytes	CC2 CCU60	7 + 2	no CAN Nodes, 6 Serial Chan.
XE162HN-24F80L	192 Kbytes	8 Kbytes 16 Kbytes	CC2 CCU60	7 + 2	no CAN Nodes, 6 Serial Chan.
XE162HN-40F80L	320 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60	7 + 2	no CAN Nodes, 6 Serial Chan.

1) Specific information about the on-chip Flash memory in [Table 2](#).

2) All derivatives additionally provide 8 Kbytes SBRAM and 2 Kbytes DPRAM.

3) Specific information about the available channels in [Table 4](#).

Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
43	P10.3	O0 / I	St/B	Bit 3 of Port 10, General Purpose Input/Output
	CCU60_COU T60	O2	St/B	CCU60 Channel 0 Output
	U0C0_DX2A	I	St/B	USIC0 Channel 0 Shift Control Input
	U0C1_DX2A	I	St/B	USIC0 Channel 1 Shift Control Input
44	P10.4	O0 / I	St/B	Bit 4 of Port 10, General Purpose Input/Output
	U0C0_SELO 3	O1	St/B	USIC0 Channel 0 Select/Control 3 Output
	CCU60_COU T61	O2	St/B	CCU60 Channel 1 Output
	U0C0_DX2B	I	St/B	USIC0 Channel 0 Shift Control Input
	U0C1_DX2B	I	St/B	USIC0 Channel 1 Shift Control Input
	ESR1_9	I	St/B	ESR1 Trigger Input 9
45	P10.5	O0 / I	St/B	Bit 5 of Port 10, General Purpose Input/Output
	U0C1_SCLK OUT	O1	St/B	USIC0 Channel 1 Shift Clock Output
	CCU60_COU T62	O2	St/B	CCU60 Channel 2 Output
	U2C0_DOUT	O3	St/B	USIC2 Channel 0 Shift Data Output
	U0C1_DX1B	I	St/B	USIC0 Channel 1 Shift Clock Input
46	P10.6	O0 / I	St/B	Bit 6 of Port 10, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	U1C0_SELO 0	O3	St/B	USIC1 Channel 0 Select/Control 0 Output
	U0C0_DX0C	I	St/B	USIC0 Channel 0 Shift Data Input
	U1C0_DX2D	I	St/B	USIC1 Channel 0 Shift Control Input
	CCU60_CTR APA	I	St/B	CCU60 Emergency Trap Input

General Device Information

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
62	PORST	I	In/B	Power On Reset Input A low level at this pin resets the XE162xN completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pull-up device will hold this pin high when nothing is driving it.
63	ESR0	O0 / I	St/B	External Service Request 0 After power-up, ESR0 operates as open-drain bidirectional reset with a weak pull-up.
	U1C0_DX0E	I	St/B	USIC1 Channel 0 Shift Data Input
	U1C0_DX2B	I	St/B	USIC1 Channel 0 Shift Control Input
6	V_{DDIM}	-	PS/M	Digital Core Supply Voltage for Domain M Decouple with a ceramic capacitor, see Data Sheet for details.
24, 41, 57	V_{DDI1}	-	PS/I	Digital Core Supply Voltage for Domain 1 Decouple with a ceramic capacitor, see Data Sheet for details. All V_{DDI1} pins must be connected to each other.
9	V_{DDPA}	-	PS/A	Digital Pad Supply Voltage for Domain A Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. <i>Note: The A/D Converters and ports P5, P6 and P15 are fed from supply voltage V_{DDPA}.</i>

3.3 Memory Protection Unit (MPU)

The XE162xN's Memory Protection Unit (MPU) protects user-specified memory areas from unauthorized read, write, or instruction fetch accesses. The MPU can protect the whole address space including the peripheral area. This completes established mechanisms such as the register security mechanism or stack overrun/underrun detection.

Four Protection Levels support flexible system programming where operating system, low level drivers, and applications run on separate levels. Each protection level permits different access restrictions for instructions and/or data.

Every access is checked (if the MPU is enabled) and an access violating the permission rules will be marked as invalid and leads to a protection trap.

A set of protection registers for each protection level specifies the address ranges and the access permissions. Applications requiring more than 4 protection levels can dynamically re-program the protection registers.

3.4 Memory Checker Module (MCHK)

The XE162xN's Memory Checker Module calculates a checksum (fractional polynomial division) on a block of data, often called Cyclic Redundancy Code (CRC). It is based on a 32-bit linear feedback shift register and may, therefore, also be used to generate pseudo-random numbers.

The Memory Checker Module is a 16-bit parallel input signature compression circuitry which enables error detection within a block of data stored in memory, registers, or communicated e.g. via serial communication lines. It reduces the probability of error masking due to repeated error patterns by calculating the signature of blocks of data.

The polynomial used for operation is configurable, so most of the commonly used polynomials may be used. Also, the block size for generating a CRC result is configurable via a local counter. An interrupt may be generated if testing the current data block reveals an error.

An autonomous CRC compare circuitry is included to enable redundant error detection, e.g. to enable higher safety integrity levels.

The Memory Checker Module provides enhanced fault detection (beyond parity or ECC) for data and instructions in volatile and non volatile memories. This is especially important for the safety and reliability of embedded systems.

Functional Description

to a dedicated vector table location). The occurrence of a hardware trap is also indicated by a single bit in the trap flag register (TFR). Unless another higher-priority trap service is in progress, a hardware trap will interrupt any ongoing program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Depending on the package option up to 3 External Service Request (ESR) pins are provided. The ESR unit processes their input values and allows to implement user controlled trap functions (System Requests SR0 and SR1). In this way reset, wakeup and power control can be efficiently realized.

Software interrupts are supported by the 'TRAP' instruction in combination with an individual trap (interrupt) number. Alternatively to emulate an interrupt by software a program can trigger interrupt requests by writing the Interrupt Request (IR) bit of an interrupt control register.

3.6 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system built into the XE162xN provides a broad range of debug and emulation features. User software running on the XE162xN can be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface. This either consists of the 2-pin Device Access Port (DAP) or of the JTAG port conforming to IEEE-1149. The debug interface can be completed with an optional break interface.

The debugger controls the OCDS with a set of dedicated registers accessible via the debug interface (DAP or JTAG). In addition the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported, as is the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU halt, a monitor call, a data transfer, or/and the activation of an external signal.

Tracing of data can be obtained via the debug interface, or via the external bus interface for increased performance.

Tracing of program execution is supported by the XE166 Family emulation device. With this device the DAP can operate on clock rates of up to 20 MHz.

The DAP interface uses two interface signals, the JTAG interface uses four interface signals, to communicate with external circuitry. The debug interface can be amended with two optional break lines.

3.8 Capture/Compare Units CCU6x

The XE162xN types feature the CCU60 unit(s).

CCU6 is a high-resolution capture and compare unit with application-specific modes. It provides inputs to start the timers synchronously, an important feature in devices with several CCU6 modules.

The module provides two independent timers (T12, T13), that can be used for PWM generation, especially for AC motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features

- Three capture/compare channels, where each channel can be used either as a capture or as a compare channel.
- Supports generation of a three-phase PWM (six outputs, individual signals for high-side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Automatic start on a HW event (T12HR, for synchronization purposes)

Timer 13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period match and compare match
- Single-shot mode supported
- Automatic start on a HW event (T13HR, for synchronization purposes)

Additional Features

- Block commutation for brushless DC drives implemented
- Position detection via Hall sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC drives
- Output levels can be selected and adapted to the power stage

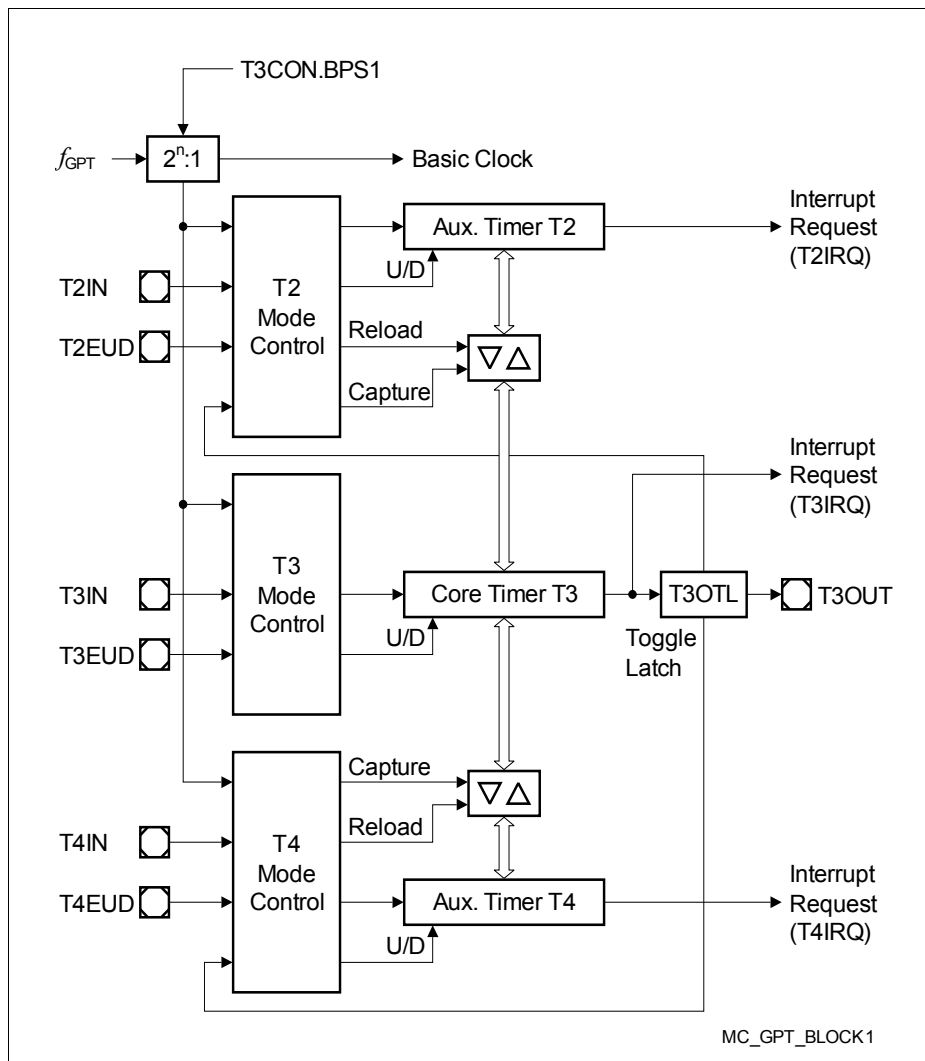


Figure 8 Block Diagram of GPT1

3.12 Universal Serial Interface Channel Modules (USIC)

The XE162xN features the USIC modules USIC0, USIC1, USIC2. Each module provides two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent of the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit. The inputs and outputs of each USIC channel can be assigned to different interface pins, providing great flexibility to the application software. All assignments can be made during runtime.

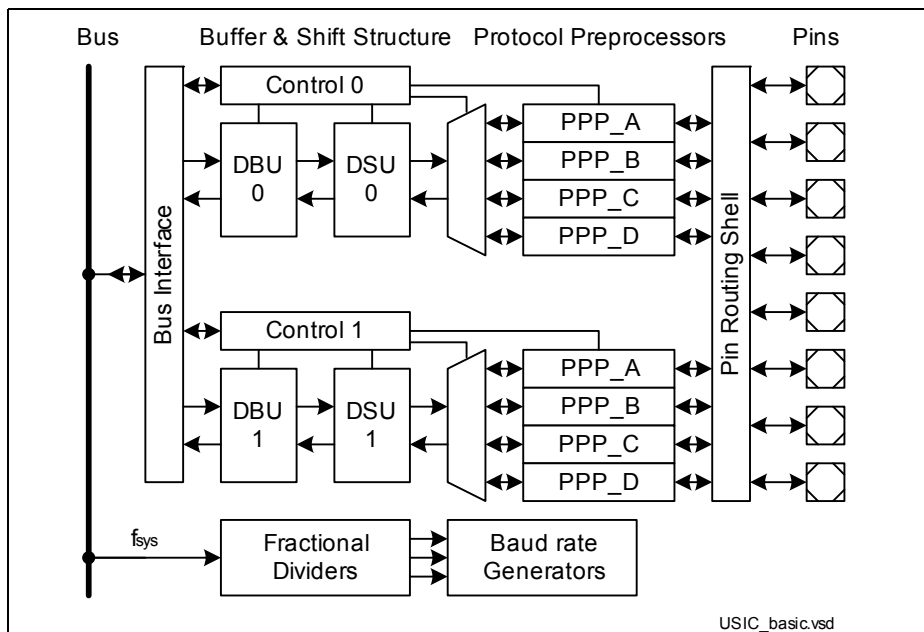


Figure 11 General Structure of a USIC Module

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols with improved performances (baud rate, buffer handling)

Target Protocols

Each USIC channel can receive and transmit data frames with a selectable data word width from 1 to 16 bits in each of the following protocols:

- **UART** (asynchronous serial channel)
 - module capability: maximum baud rate = $f_{\text{SYS}} / 4$
 - data frame length programmable from 1 to 63 bits
 - MSB or LSB first
- **LIN** Support (Local Interconnect Network)
 - module capability: maximum baud rate = $f_{\text{SYS}} / 16$
 - checksum generation under software control
 - baud rate detection possible by built-in capture event of baud rate generator
- **SSC/SPI** (synchronous serial channel with or without data buffer)
 - module capability: maximum baud rate = $f_{\text{SYS}} / 2$, limited by loop delay
 - number of data bits programmable from 1 to 63, more with explicit stop condition
 - MSB or LSB first
 - optional control of slave select signals
- **IIC** (Inter-IC Bus)
 - supports baud rates of 100 kbit/s and 400 kbit/s
- **IIS** (Inter-IC Sound Bus)
 - module capability: maximum baud rate = $f_{\text{SYS}} / 2$

Note: Depending on the selected functions (such as digital filters, input synchronization stages, sample point adjustment, etc.), the maximum achievable baud rate can be limited. Please note that there may be additional delays, such as internal or external propagation delays and driver delays (e.g. for collision detection in UART mode, for IIC, etc.).

MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Independent CAN nodes
- Set of independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
 - Can be assigned to one of the CAN nodes
 - Configurable as transmit or receive objects, or as message buffer FIFO
 - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
 - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

3.14 System Timer

The System Timer consists of a programmable prescaler and two concatenated timers (10 bits and 6 bits). Both timers can generate interrupt requests. The clock source can be selected and the timers can also run during power reduction modes.

Therefore, the System Timer enables the software to maintain the current time for scheduling functions or for the implementation of a clock.

3.15 Watchdog Timer

The Watchdog Timer is one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after an application reset of the chip. It can be disabled and enabled at any time by executing the instructions DISWDT and ENWDT respectively. The software has to service the Watchdog Timer before it overflows. If this is not the case because of a hardware or software failure, the Watchdog Timer overflows, generating a prewarning interrupt and then a reset request.

The Watchdog Timer is a 16-bit timer clocked with the system clock divided by 16,384 or 256. The Watchdog Timer register is set to a prespecified reload value (stored in WDTRRL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the Watchdog Timer is reloaded and the prescaler is cleared.

Time intervals between 3.2 μ s and 13.4 s can be monitored (@ 80 MHz).

The default Watchdog Timer interval after power-up is 6.5 ms (@ 10 MHz).

3.16 Clock Generation

The Clock Generation Unit can generate the system clock signal f_{SYS} for the XE162xN from a number of external or internal clock sources:

- External clock signals with pad voltage or core voltage levels
- External crystal or resonator using the on-chip oscillator
- On-chip clock source for operation without crystal/resonator
- Wake-up clock (ultra-low-power) to further reduce power consumption

The programmable on-chip PLL with multiple prescalers generates a clock signal for maximum system performance from standard crystals, a clock input signal, or from the on-chip clock source. See also [Section 4.7.2](#).

The Oscillator Watchdog (OWD) generates an interrupt if the crystal oscillator frequency falls below a certain limit or stops completely. In this case, the system can be supplied with an emergency clock to enable operation even after an external clock failure.

All available clock signals can be output on one of two selectable pins.

3.18 Instruction Set Summary

Table 10 lists the instructions of the XE162xN.

The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the “**Instruction Set Manual**”.

This document also provides a detailed description of each instruction.

Table 10 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

Functional Description
Table 10 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2 / 4
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH/POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Unused instruction ¹⁾	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENWDT	Disable/Enable Watchdog Timer	4
EINIT	End-of-Initialization Register Lock	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTENDED Register sequence	2
EXTP(R)	Begin EXTENDED Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTENDED Segment (and Register) sequence	2 / 4

Electrical Parameters
Table 12 Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload current coupling factor for digital I/O pins	K_{OVD} CC	—	1.0×10^{-2}	3.0×10^{-2}	-	$I_{OV} < 0$ mA; not subject to production test
		—	1.0×10^{-4}	5.0×10^{-3}	-	$I_{OV} > 0$ mA; not subject to production test
Absolute sum of overload currents	$\Sigma I_{OV} $ SR	—	—	50	mA	not subject to production test
Digital core supply voltage for domain M ⁸⁾	V_{DDIM} CC	—	1.5	—		
Digital core supply voltage for domain 1 ⁸⁾	V_{DDI1} CC	—	1.5	—		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	3.0	—	5.5	V	
Digital ground voltage	V_{SS} SR	—	0	—	V	

- 1) To ensure the stability of the voltage regulators the EVRs must be buffered with ceramic capacitors. Separate buffer capacitors with the recommended values shall be connected as close as possible to each V_{DDIM} and V_{DDI1} pin to keep the resistance of the board tracks below 2 Ohm. Connect all V_{DDI1} pins together. The minimum capacitance value is required for proper operation under all conditions (e.g. temperature). Higher values slightly increase the startup time.
- 2) Use one Capacitor for each pin.
- 3) This is the reference load. For bigger capacitive loads, use the derating factors listed in the pad properties section.
- 4) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C_L).
- 5) The operating frequency range may be reduced for specific device types. This is indicated in the device designation (...FxxL). 80 MHz devices are marked ...F80L.
- 6) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{IHmax}$ ($I_{OV} > 0$) or $V_{OV} < V_{ILmin}$ ($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed 50 mA. The supply voltages must remain within the specified limits. Proper operation under overload conditions depends on the application. Overload conditions must not occur on pin XTAL1 (powered by V_{DDIM}).

Pullup/Pulldown Device Behavior

Most pins of the XE162xN feature pullup or pulldown devices. For some special pins these are fixed; for the port pins they can be selected by the application.

The specified current values indicate how to load the respective pin depending on the intended signal level. **Figure 13** shows the current paths.

The shaded resistors shown in the figure may be required to compensate system pull currents that do not match the given limit values.

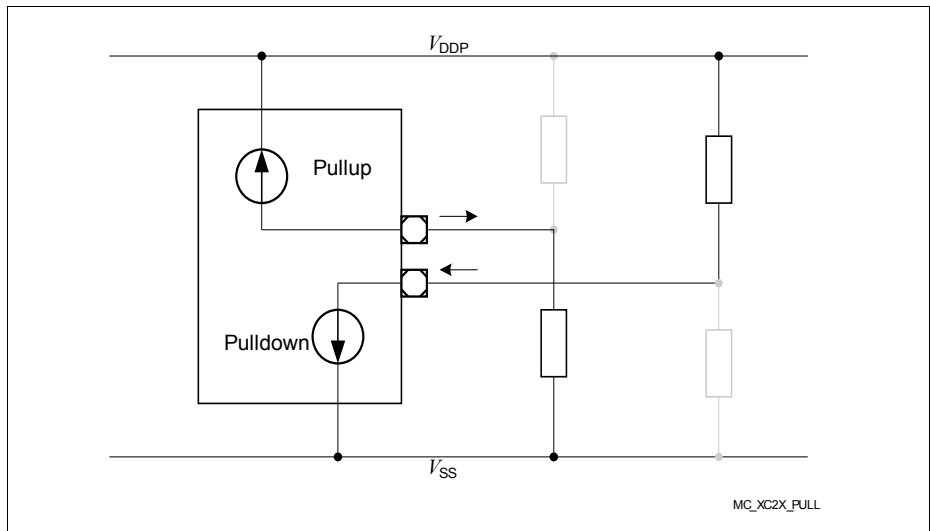


Figure 13 Pullup/Pulldown Current Definition

Electrical Parameters
Table 19 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Broken wire detection delay against VAGND ²⁾	t_{BWG} CC	—	—	50 ³⁾		
Broken wire detection delay against VAREF ²⁾	t_{BWR} CC	—	—	50 ⁴⁾		
Conversion time for 8-bit result ²⁾	t_{c8} CC	$(11+S \cdot TC) \times t_{ADCI} + 2 \times t_{SYS}$	—	—		
Conversion time for 10-bit result ²⁾	t_{c10} CC	$(13+S \cdot TC) \times t_{ADCI} + 2 \times t_{SYS}$	—	—		
Total Unadjusted Error	TUE CC	—	1	2	LSB	⁵⁾
Wakeup time from analog powerdown, fast mode	t_{WAF} CC	—	—	4	μs	
Wakeup time from analog powerdown, slow mode	t_{WAS} CC	—	—	15	μs	
Analog reference ground	V_{AGND} SR	$V_{SS} - 0.05$	—	1.5	V	
Analog input voltage range	V_{AIN} SR	V_{AGND}	—	V_{AREF}	V	⁶⁾
Analog reference voltage	V_{AREF} SR	$V_{AGND} + 1.0$	—	$V_{DDPA} + 0.05$	V	

1) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation. At room temperature and nominal supply voltage the following typical values can be used: $C_{AINTyp} = 12$ pF, $C_{AINStyp} = 5$ pF, $R_{AINTyp} = 1.0$ kOhm, $C_{AREFTyp} = 15$ pF, $C_{AREFSTyp} = 10$ pF, $R_{AREFTyp} = 1.0$ kOhm.

2) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result. Values for the basic clock t_{ADCI} depend on programming.

3) The broken wire detection delay against V_{AGND} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 500 μs. Result below 10% (66μ)

Electrical Parameters

- 1) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF} . This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1} .
- 2) Overload conditions must not occur on pin XTAL1.

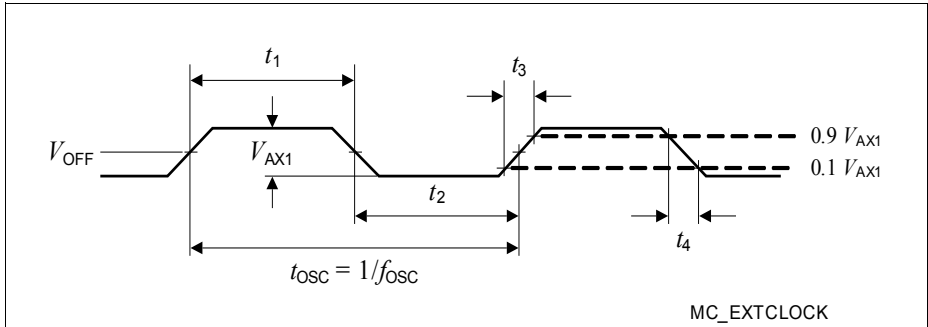


Figure 21 External Clock Drive XTAL1

Note: For crystal or ceramic resonator operation, it is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for oscillator operation. The manufacturers of crystals and ceramic resonators offer an oscillator evaluation service. This evaluation checks the crystal/resonator specification limits to ensure a reliable oscillator operation.

Electrical Parameters

Table 35 JTAG Interface Timing for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK low time	t_3 SR	16	—	—	ns	
TCK clock rise time	t_4 SR	—	—	8	ns	
TCK clock fall time	t_5 SR	—	—	8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	—	—	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6	—	—	ns	
TDO valid from TCK falling edge (propagation delay) ²⁾	t_8 CC	—	25	29	ns	
TDO high impedance to valid output from TCK falling edge ³⁾²⁾	t_9 CC	—	25	29	ns	
TDO valid output to high impedance from TCK falling edge ²⁾	t_{10} CC	—	25	29	ns	
TDO hold after TCK falling edge ²⁾	t_{18} CC	5	—	—	ns	

1) Under typical conditions, the JTAG interface can operate at transfer rates up to 20 MHz.

2) The falling edge on TCK is used to generate the TDO timing.

3) The setup time for TDO is given implicitly by the TCK cycle time.

Table 36 is valid under the following conditions: $C_L = 20$ pF; voltage_range= lower

Table 36 JTAG Interface Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50	—	—	ns	
TCK high time	t_2 SR	16	—	—	ns	
TCK low time	t_3 SR	16	—	—	ns	
TCK clock rise time	t_4 SR	—	—	8	ns	
TCK clock fall time	t_5 SR	—	—	8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	—	—	ns	

Electrical Parameters

Table 36 JTAG Interface Timing for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TDI/TMS hold after TCK rising edge	t_7 SR	6	—	—	ns	
TDO valid from TCK falling edge (propagation delay) ¹⁾	t_8 CC	—	32	36	ns	
TDO high impedance to valid output from TCK falling edge ²⁾¹⁾	t_9 CC	—	32	36	ns	
TDO valid output to high impedance from TCK falling edge ¹⁾	t_{10} CC	—	32	36	ns	
TDO hold after TCK falling edge ¹⁾	t_{18} CC	5	—	—	ns	

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

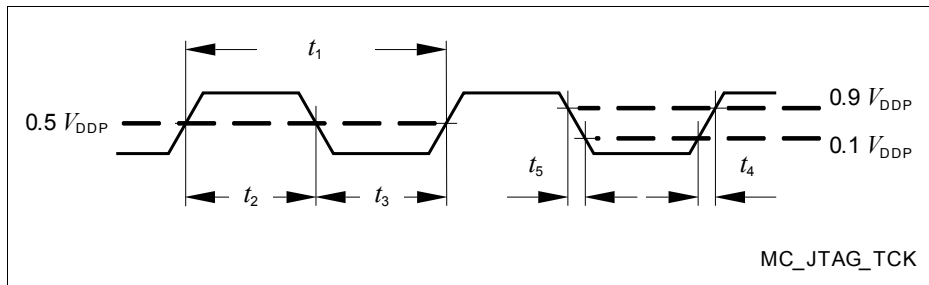


Figure 26 Test Clock Timing (TCK)

5 Package and Reliability

The XE166 Family devices use the package type PG-LQFP (Plastic Green - Low Profile Quad Flat Package). The following specifications must be regarded to ensure proper integration of the XE162xN in its target environment.

5.1 Packaging

These parameters specify the packaging rather than the silicon.

Table 37 Package Parameters (PG-LQFP-64-6)

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Exposed Pad Dimension	$E_x \times E_y$	–	5.6×5.6	mm	–
Power Dissipation	P_{DISS}	–	0.8	W	–
Thermal resistance Junction-Ambient	$R_{\Theta JA}$	–	40	K/W	No thermal via ¹⁾
			37	K/W	4-layer, no pad ²⁾
			25	K/W	4-layer, pad ³⁾

1) Device mounted on a 4-layer board without thermal vias; exposed pad not soldered.

2) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad not soldered.

3) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad soldered to the board.

Note: To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground, independent of the thermal requirements.

Board layout examples are given in an application note.

Package Compatibility Considerations

The XE162xN is a member of the XE166 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Pad (if present) may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.