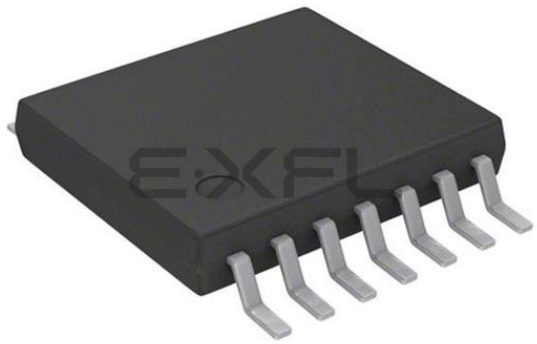

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 11 |
| Program Memory Size | 3.5KB (2K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V |
| Data Converters | A/D 8x10b; D/A 1x9b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 14-TSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | 14-TSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16f753-e-st |

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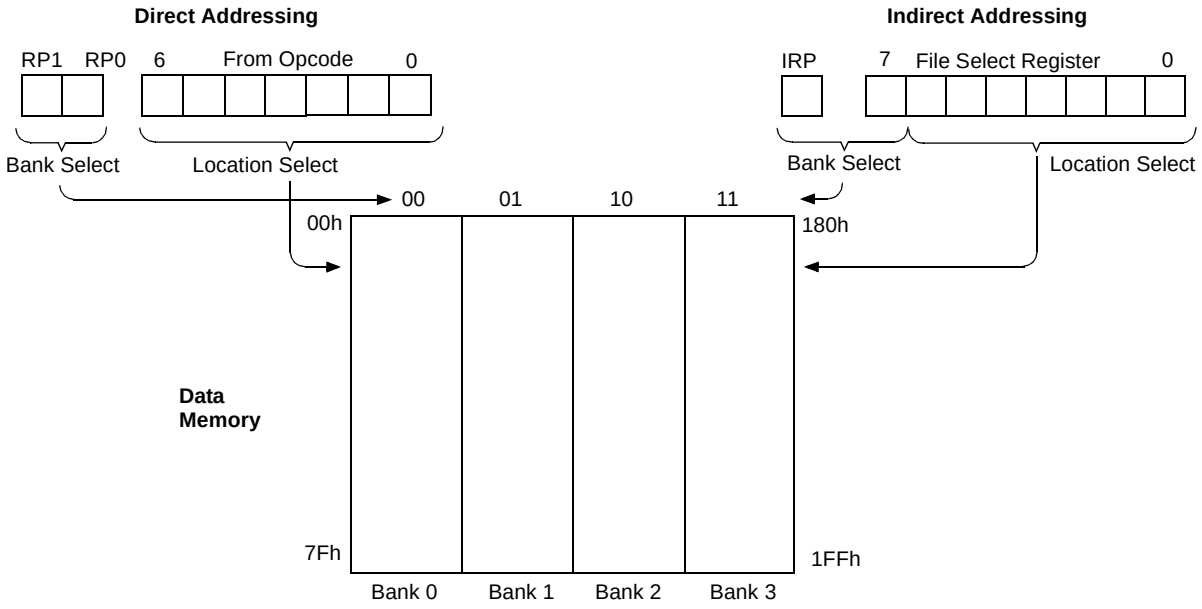
**TABLE 1-1: PIC16F753/HV753 PINOUT DESCRIPTION (CONTINUED)**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| RC2/AN6/SLPCIN/ OPA1OUT/C1IN2-/C2IN2- | RC2 | TTL | CMOS | General purpose I/O with IOC and WPU. |
| | AN6 | AN | — | A/D Channel 6 input. |
| | OPA1OUT | AN | HP | Op amp output. |
| | C1IN2- | AN | — | Comparator C1 negative input. |
| | C2IN2- | AN | — | Comparator C2 negative input. |
| RC3/AN7/C1IN3-/C2IN3- | RC3 | TTL | CMOS | General purpose I/O with IOC and WPU. |
| | AN7 | AN | — | A/D Channel 7 input. |
| | C1IN3- | AN | — | Comparator C1 negative input. |
| | C2IN3- | AN | — | Comparator C2 negative input. |
| RC4/COG1OUT1/C2OUT | RC4 | TTL | CMOS | General purpose I/O with IOC and WPU. |
| | COG1OUT1 | — | CMOS | COG output Channel 1. |
| | C2OUT | — | HP | Comparator C2 output. |
| RC5/COG1OUT0/CCP1 | RC5 | TTL | CMOS | General purpose I/O with IOC and WPU. |
| | COG1OUT0 | — | CMOS | COG output Channel 0. |
| | CCP1 | — | HP | Capture/Compare/PWM 1. |
| VDD | VDD | Power | — | Positive supply. |
| VSS | VSS | Power | — | Ground reference. |

**Legend:** AN = Analog input or output CMOS = CMOS compatible input or output
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels
HP = High Power HV = High Voltage
* Alternate pin function.

**Note 1:** Input only.
**2:** Default pin function via the APFCON register.
**3:** Alternate pin function via the APFCON register.
**4:** RA3 pull-up is enabled when pin is configured as $\overline{\text{MCLR}}$ in Configuration Word.

**FIGURE 2-4: DIRECT/INDIRECT ADDRESSING PIC16F753/HV753**




For memory map detail, see Figure 2-2.

## 3.0 FLASH PROGRAM MEMORY SELF-READ/SELF-WRITE CONTROL

The Flash program memory is readable and writable during normal operation (full $V_{DD}$ range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers (see Registers 3-1 to 3-5). There are six SFRs used to read and write this memory:

- PMCON1
- PMCON2
- PMDATL
- PMDATH
- PMADRL
- PMADRH

When interfacing the program memory block, the PMDATL and PMDATH registers form a two-byte word which holds the 14-bit data for read/write, and the PMADRL and PMADRH registers form a two-byte word which holds the 10-bit address of the Flash location being accessed. These devices have 1K words of program Flash with an address range from 0000h to 03FFh.

The program memory allows a single-word read and a four-word write. A four-word write automatically erases the row of the location and writes the new data (erase before write).

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the voltage range of the device for byte or word operations.

When the device is code-protected, the CPU may continue to read and write the Flash program memory.

Depending on the settings of the Flash Program Memory Enable (WRT<1:0>) bits, the device may or may not be able to write certain blocks of the program memory; however, reads of the program memory are allowed.

When the Flash program memory Code Protection ($\overline{CP}$) bit in the Configuration Word register is enabled, the program memory is code-protected, and the device programmer (ICSP™) cannot access data or program memory.

### 3.1 PMADRH and PMADRL Registers

The PMADRH and PMADRL registers can address up to a maximum of 1K words of program memory.

When selecting a program address value, the Most Significant Byte (MSB) of the address is written to the PMADRH register and the Least Significant Byte (LSB) is written to the PMADRL register.

### 3.2 PMCON1 and PMCON2 Registers

PMCON1 is the control register for the data program memory accesses.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear.

PMCON2 is not a physical register. Reading PMCON2 will read all '0's. The PMCON2 register is used exclusively in the Flash memory write sequence.

## 4.3 System Clock Output

The CLKOUT pin is available for general purpose I/O or system clock output. The $\overline{\text{CLKOUTEN}}$ bit of the Configuration Word controls the function of the CLKOUT pin.

When the $\overline{\text{CLKOUTEN}}$ bit is cleared, the CLKOUT pin is driven by the selected internal oscillator frequency divided by 4. The corresponding I/O pin always reads '0' in this configuration.

The CLKOUT signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements.

When the $\overline{\text{CLKOUTEN}}$ bit is set, the system clock out function is disabled and the CLKOUT pin is available for general purpose I/O.

## 4.4 Oscillator Delay upon Wake-Up, Power-Up, and Base Frequency Change

In applications where the OSCTUNE register is used to shift the HFINTOSC frequency, the application should not expect the frequency to stabilize immediately. In this case, the frequency may shift gradually toward the new value. The time for this frequency shift is less than eight cycles of the base frequency.

A short delay is invoked upon power-up and when waking from sleep to allow the memory bias circuitry to stabilize. Table 4-1 shows examples where the oscillator delay is invoked.

**TABLE 4-1: OSCILLATOR DELAY EXAMPLES**

| Switch From | Switch To | Frequency | Oscillator Delay |
|---|---|---|---|
| Sleep/POR | INTOSC | 31 kHz to 8 MHz | 10 μs internal delay to allow memory bias to stabilize. |
| Sleep/POR | EC | DC – 20 MHz | |

**REGISTER 7-2: T1GCON: TIMER1 GATE CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-x | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TMR1GE | T1GPOL | T1GTM | T1GSPM | T1GGO/$\overline{\text{DONE}}$ | T1GVAL | T1GSS<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **TMR1GE:** Timer1 Gate Enable bit

If TMR1ON = 0:
This bit is ignored
If TMR1ON = 1:
1 = Timer1 counting is controlled by the Timer1 gate function
0 = Timer1 counts regardless of Timer1 gate function

bit 6 **T1GPOL:** Timer1 Gate Polarity bit

1 = Timer1 gate is active-high (Timer1 counts when gate is high)
0 = Timer1 gate is active-low (Timer1 counts when gate is low)

bit 5 **T1GTM:** Timer1 Gate Toggle mode bit

1 = Timer1 Gate Toggle mode is enabled.
0 = Timer1 Gate Toggle mode is disabled and toggle flip-flop is cleared
Timer1 gate flip-flop toggles on every rising edge.

bit 4 **T1GSPM:** Timer1 Gate Single-Pulse mode bit

1 = Timer1 Gate Single-Pulse mode is enabled and is controlling Timer1 gate
0 = Timer1 Gate Single-Pulse mode is disabled

bit 3 **T1GGO/$\overline{\text{DONE}}$:** Timer1 Gate Single-Pulse Acquisition Status bit

1 = Timer1 gate single-pulse acquisition is ready, waiting for an edge
0 = Timer1 gate single-pulse acquisition has completed or has not been started
This bit is automatically cleared when T1GSPM is cleared.

bit 2 **T1GVAL:** Timer1 Gate Current State bit

Indicates the current state of the Timer1 gate that could be provided to TMR1H:TMR1L.
Unaffected by Timer1 Gate Enable (TMR1GE).

bit 1-0 **T1GSS<1:0>:** Timer1 Gate Source Select bits

11 = SYNCC2OUT
10 = SYNCC1OUT
01 = Timer0 overflow output
00 = Timer1 gate pin

## 10.3 PWM Overview

Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully on and fully off states. The PWM signal resembles a square wave where the high portion of the signal is considered the on state and the low portion of the signal is considered the off state. The high portion, also known as the pulse width, can vary in time and is defined in steps. A larger number of steps applied, which lengthens the pulse width, also supplies more power to the load. Lowering the number of steps applied, which shortens the pulse width, supplies less power. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse width time and in turn the power that is applied to the load.

The term duty cycle describes the proportion of the on time to the off time and is expressed in percentages, where 0% is fully off and 100% is fully on. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied.

Figure 10-3 shows a typical waveform of the PWM signal.

### 10.3.1 STANDARD PWM OPERATION

The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the CCP1 pin with up to 10 bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- PR2 registers
- T2CON registers
- CCPR1L registers
- CCP1CON registers

Figure 10-4 shows a simplified block diagram of PWM operation.

| | |
|---|---|
| **Note 1:** | The corresponding TRIS bit must be cleared to enable the PWM output on the CCP1 pin. |
| **2:** | Clearing the CCP1CON register will relinquish control of the CCP1 pin. |

**FIGURE 10-3: CCP1 PWM OUTPUT SIGNAL**

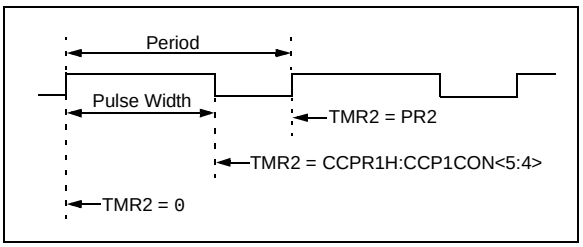
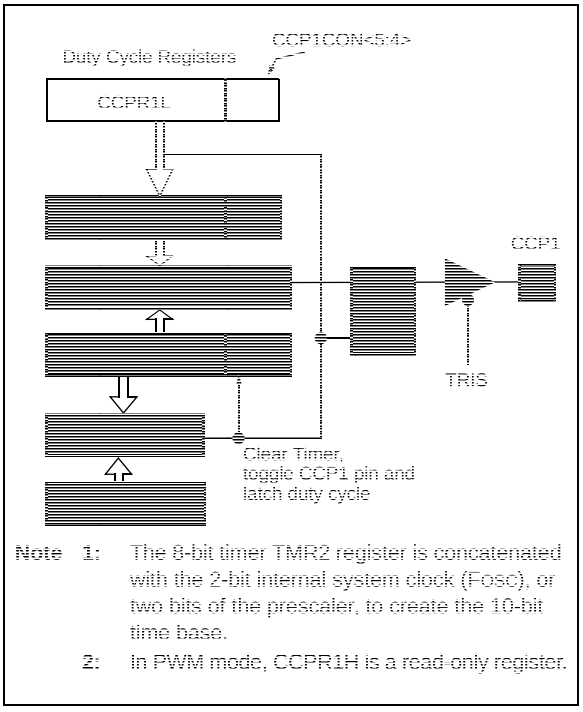



**FIGURE 10-4: SIMPLIFIED PWM BLOCK DIAGRAM**




**Note 1:** The 8-bit timer TMR2 register is concatenated with the 2-bit internal system clock (FOSC), or two bits of the prescaler, to create the 10-bit time base.

**2:** In PWM mode, CCPR1H is a read-only register.

## 11.0 COMPLEMENTARY OUTPUT GENERATOR (COG) MODULE

The primary purpose of the Complementary Output Generator (COG) is to convert a single output PWM signal into a two output complementary PWM signal. The COG can also convert two separate input events into a single or complementary PWM output.

The COG PWM frequency and duty cycle are determined by a rising event input and a falling event input. The rising event and falling event may be the same source. Sources may be synchronous or asynchronous to the COG_clock.

The rate at which the rising event occurs determines the PWM frequency. The time from the rising event input to the falling event input determines the duty cycle.

A selectable clock input is used to generate the phase delay, blanking and dead-band times.

A simplified block diagram of the COG is shown in Figure 11-1.

The COG module has the following features:

- Two modes of operation:
  - Synchronous PWM
  - Push-pull
- Selectable clock source
- Independently selectable rising event sources
- Independently selectable falling event sources
- Independently selectable edge or level event sensitivity
- Independent output enables
- Independent output polarity selection
- Phase delay with independent rising and falling delay times
- Dead-band control with:
  - Independent rising and falling event dead-band times
  - Synchronous and asynchronous timing
- Blanking control with independent rising and falling event blanking times
- Auto-shutdown control with:
  - Independently selectable shutdown sources
  - Auto-restart enable
  - Auto-shutdown pin override control (high, low, off, and High-Z)

## 11.1 Fundamental Operation

### 11.1.1 SYNCHRONOUS PWM MODE

In synchronous PWM mode, the COG generates a two output complementary PWM waveform from rising and falling event sources. In the simplest configuration, the rising and falling event sources have the same signal, which is a PWM signal with the desired period and duty cycle. The COG converts this single PWM input into a dual complementary PWM output. The frequency and duty cycle of the dual PWM output match those of the single input PWM signal. The off-to-on transition of each output can be delayed from the on-to-off transition of the other output, thereby creating a time immediately after the PWM transition where neither output is driven. This is referred to as dead time and is covered in **Section 11.5 “Dead-Band Control”**.

A typical operating waveform, with dead band, generated from a single CCP1 input is shown in Figure 11-4.

### 11.1.2 PUSH-PULL MODE

In Push-Pull mode, the COG generates a single PWM output that alternates every PWM period, between the two COG output pins. The output drive activates with the rising input event and terminates with the falling event input. Each rising event starts a new period and causes the output to switch to the COG pin not used in the previous period.

A typical push-pull waveform generated from a single CCP1 input is shown in Figure 11-6.

Push-Pull mode is selected by setting the GxMD bit of the COGxCON0 register.

### 11.1.3 ALL MODES

In addition to generating a complementary output from a single PWM input, the COG can also generate PWM waveforms from a periodic rising event and a separate falling event. In this case, the falling event is usually derived from analog feedback within the external PWM driver circuit. In this configuration, high-power switching transients may trigger a false falling event that needs to be blanked out. The COG can be configured to blank falling (and rising) event inputs for a period of time immediately following the rising (and falling) event drive output. This is referred to as input blanking and is described in **Section 11.6 “Blanking Control”**.

It may be necessary to guard against the possibility of circuit faults. In this case, the active drive must be terminated before the Fault condition causes damage. This is referred to as auto-shutdown and is described in **Section 11.8 “Auto-shutdown Control”**.

A feedback falling event arriving too late or not at all can be terminated with auto-shutdown or by enabling one of the Hardware Limit Timer (HLT) event inputs. See **Section 9.0 “Hardware Limit Timer (HLT) Module”** for more information about the HLT.

The COG can be configured to operate in phase delayed conjunction with another PWM. The active drive cycle is delayed from the rising event by a phase delay timer. Phase delay is covered in more detail in **Section 11.7 “Phase Delay”**. A typical operating waveform, with phase delay and dead band, generated from a single CCP1 input, is shown in Figure 11-5.

**REGISTER 11-3: COGxRIS: COG RISING EVENT INPUT SELECTION REGISTER**

| U-0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| — | GxRIHLT2 | GxRIHLT1 | GxRIT2M | GxRIFLT | GxRICCP1 | GxRIC2 | GxRIC1 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | q = Value depends on condition |

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **GxRIHLT2:** COGx Rising Event Input Source 6 Enable bit
1 = HLTimer2 output is enabled as a rising event input
0 = HLTimer2 has no effect on the rising event

bit 5 **GxRIHLT1:** COGx Rising Event Input Source 5 Enable bit
1 = HLTimer1 output is enabled as a rising event input
0 = HLTimer1 has no effect on the rising event

bit 4 **GxRIT2M:** COGx Rising Event Input Source 4 Enable bit
1 = Timer2 match with PR2 is enabled as a rising event input
0 = Timer2 match with PR2 has no effect on the rising event

bit 3 **GxRIFLT:** COGx Rising Event Input Source 3 Enable bit
1 = COGxFLT pin is enabled as a rising event input
0 = COGxFLT pin has no effect on the rising event

bit 2 **GxRICCP1:** COGx Rising Event Input Source 2 Enable bit
1 = CCP1 output is enabled as a rising event input
0 = CCP1 has no effect on the rising event

bit 1 **GxRIC2:** COGx Rising Event Input Source 1 Enable bit
1 = Comparator 2 output is enabled as a rising event input
0 = Comparator 2 output has no effect on the rising event

bit 0 **GxRIC1:** COGx Rising Event Input Source 0 Enable bit
1 = Comparator 1 output is enabled as a rising event input
0 = Comparator 1 output has no effect on the rising event

**REGISTER 11-7: COGxASD0: COG AUTO-SHUTDOWN CONTROL REGISTER 0**

| R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| GxASDE | GxARSEN | GxASD1L<1:0> | | GxASD0L<1:0> | | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | q = Value depends on condition |

bit 7 **GxASDE:** Auto-Shutdown Event Status bit
1 = COG is in the shutdown state
0 = COG is either not in the shutdown state or will exit the shutdown state on the next rising event

bit 6 **GxARSEN:** Auto-Restart Enable bit
1 = Auto-restart is enabled
0 = Auto-restart is disabled

bit 5-4 **GxASD1L<1:0>:** COGxOUT1 Auto-Shutdown Override Level Select bits
11 = COGxOUT1 is tri-stated when shutdown is active
10 = The inactive state of the pin, including polarity, is placed on COGxOUT1 when shutdown is active
01 = A logic ‘1’ is placed on COGxOUT1 when shutdown is active
00 = A logic ‘0’ is placed on COGxOUT1 when shutdown is active

bit 3-2 **GxASD0L<1:0>:** COGxOUT0 Auto-Shutdown Override Level Select bits
11 = COGxOUT0 is tri-stated when shutdown is active
10 = The inactive state of the pin, including polarity, is placed on COGxOUT0 when shutdown is active
01 = A logic ‘1’ is placed on COGxOUT0when shutdown is active
00 = A logic ‘0’ is placed on COGxOUT0when shutdown is active

bit 1-0 **Unimplemented:** Read as ‘0’

## 12.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESL and ADRESH).

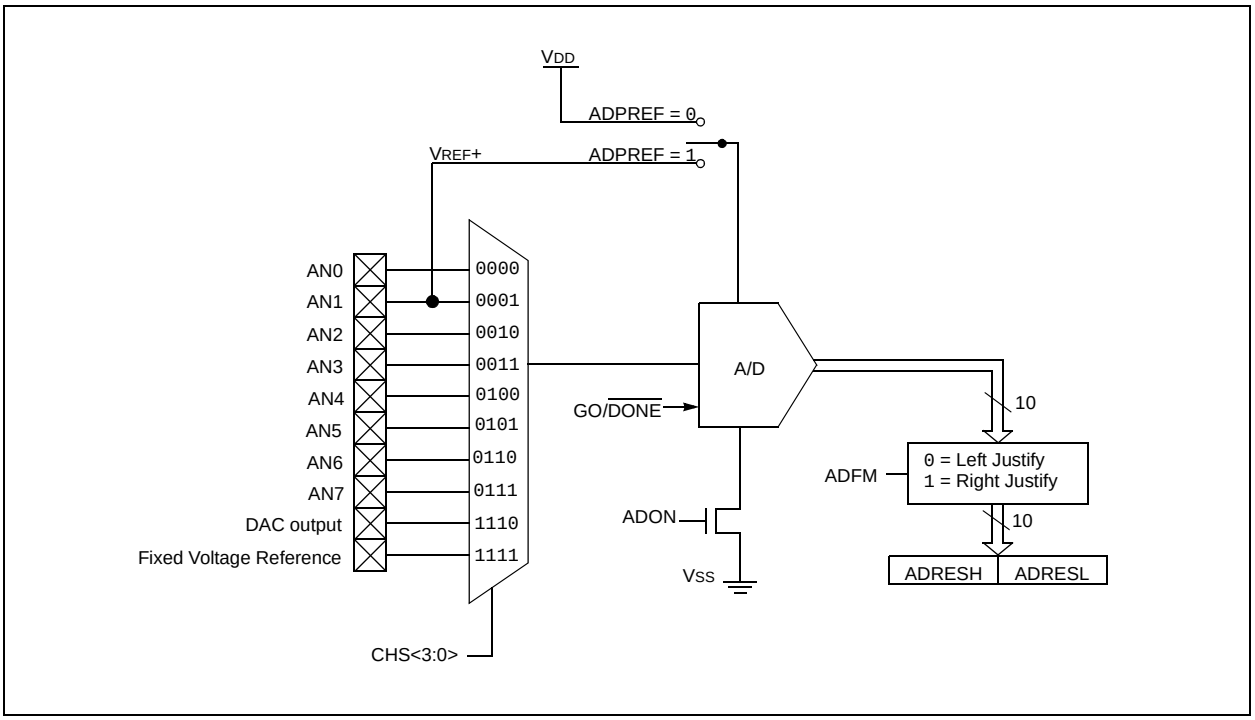
The ADC voltage reference is software selectable to either VDD or a voltage applied to the external reference pins.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake up the device from Sleep.

Figure 12-1 shows the block diagram of the ADC.

| **Note:** | The ADRESL and ADRESH registers are read-only. |
|---|---|

**FIGURE 12-1: ADC BLOCK DIAGRAM**



### 12.2.6 A/D CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure Port:
   - Disable pin output driver (See TRIS register)
   - Configure pin as analog
2. Configure the ADC module:
   - Select ADC conversion clock
   - Configure voltage reference
   - Select ADC input channel
   - Select result format
   - Turn on ADC module
3. Configure ADC interrupt (optional):
   - Clear ADC interrupt flag
   - Enable ADC interrupt
   - Enable peripheral interrupt
   - Enable global interrupt**(1)**
4. Wait the required acquisition time**(2)**.
5. Start conversion by setting the GO/$\overline{\text{DONE}}$ bit.
6. Wait for ADC conversion to complete by one of the following:
   - Polling the GO/$\overline{\text{DONE}}$ bit
   - Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC Result
8. Clear the ADC interrupt flag (required if interrupt is enabled).

**Note 1:** The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

**2:** See **Section 12.4 "A/D Acquisition Requirements"**.

**EXAMPLE 12-1: A/D CONVERSION**

```
;This code block configures the ADC
;for polling, Vdd reference, Frc clock
;and RA0 input.
;
;Conversion start & polling for completion
; are included.
;
  BANKSEL  TRISA       ;
  BSF      TRISA,0     ;Set RA0 to input
  BANKSEL  ADCON1      ;
  MOVLW    B'01110000' ;ADC Frc clock,
  IORWF    ADCON1      ; and RA0 as analog
  BANKSEL  ADCON0      ;
  MOVLW    B'10000001' ;Right justify,
  MOVWF    ADCON0      ;Vdd Vref, AN0, On
  CALL     SampleTime  ;Acquisiton delay
  BSF      ADCON0,GO   ;Start conversion
TEST AGAIN
  BTFSC    ADCON0,GO   ;Is conversion done?
  GOTO     TEST AGAIN  ;No, test again
  BANKSEL  ADRESH      ;
  MOVF     ADRESH,W    ;Read upper 2 bits
  MOVWF    RESULTHI    ;Store in GPR space
  BANKSEL  ADRESL      ;
  MOVF     ADRESL,W    ;Read lower 8 bits
  MOVWF    RESULTLO    ;Store in GPR space
```

## 14.5 Operation During Sleep

When the device wakes up from Sleep through an interrupt or a Watchdog Timer time-out, the contents of the DACxCON0 register are not affected. To minimize current consumption in Sleep mode, the voltage reference should be disabled.

## 14.6 Effects of a Reset

A device Reset affects the following:

- DAC is disabled
- DAC output voltage is removed from the DACxOUT pin
- The DACR<8:0> range select bits are cleared

| RETFIE | Return from Interrupt |
|---|---|
| Syntax: | [ *label* ] RETFIE |
| Operands: | None |
| Operation: | TOS → PC,<br>1 → GIE |
| Status Affected: | None |
| Description: | Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a 2-cycle instruction. |
| Words: | 1 |
| Cycles: | 2 |
| Example: | `RETFIE`<br>After Interrupt<br>PC = TOS<br>GIE = 1 |

| RETLW | Return with literal in W |
|---|---|
| Syntax: | [ *label* ] RETLW k |
| Operands: | 0 ≤ k ≤ 255 |
| Operation: | k → (W);<br>TOS → PC |
| Status Affected: | None |
| Description: | The W register is loaded with the 8-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction. |
| Words: | 1 |
| Cycles: | 2 |
| Example: | `CALL TABLE;W contains`<br>`;table offset`<br>`;value`<br>`GOTO DONE`<br>`TABLE`<br>•<br>•<br>`ADDWF PC ;W = offset`<br>`RETLW k1 ;Begin table`<br>`RETLW k2 ;`<br>•<br>•<br>•<br>`RETLW kn ;End of table`<br>`DONE`<br>Before Instruction<br>W = 0x07<br>After Instruction<br>W = value of k8 |

| RETURN | Return from Subroutine |
|---|---|
| Syntax: | [ *label* ] RETURN |
| Operands: | None |
| Operation: | TOS → PC |
| Status Affected: | None |
| Description: | Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruction. |

## 23.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified $V_{DD}$ range). This is for **information only** and devices are ensured to operate properly only within the specified range.

| | |
|---|---|
| **Note:** | The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range. |

**"Typical" represents the mean of the distribution at 25°C. "MAXIMUM", "Max.", "MINIMUM" or "Min." represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.**

**FIGURE 23-5: IDD TYPICAL, EC OSCILLATOR, HIGH-POWER MODE, PIC16HV753 ONLY**

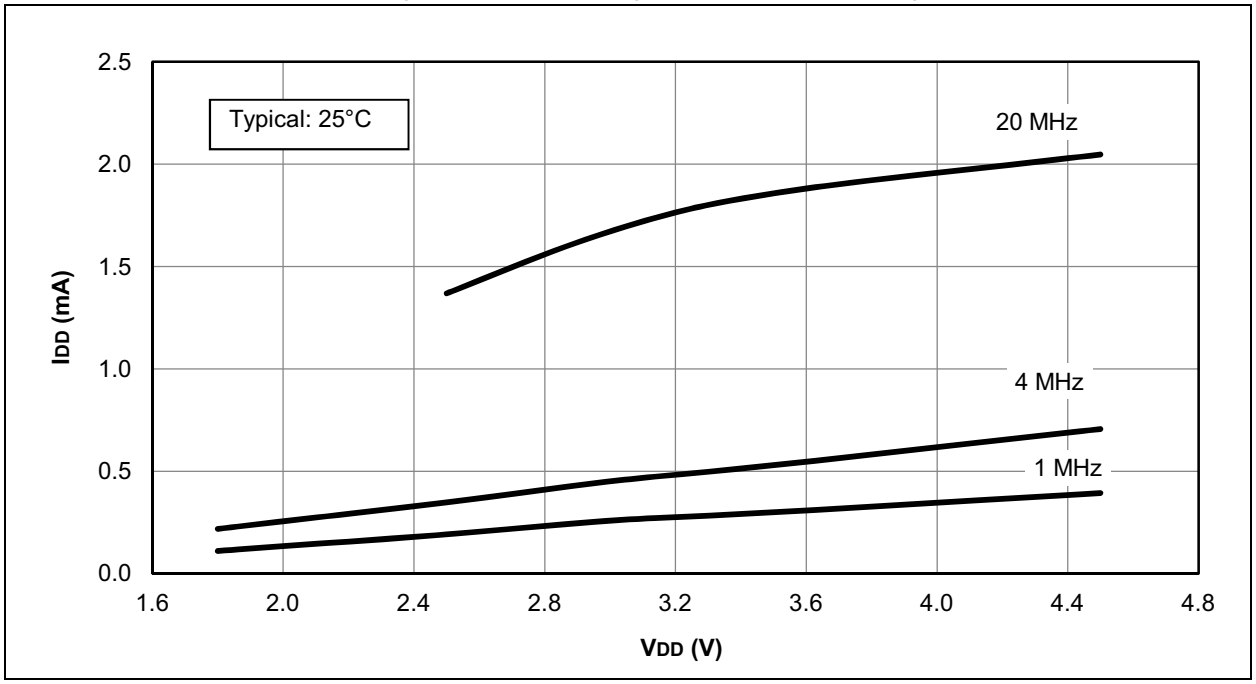



**FIGURE 23-6: IDD MAXIMUM, EC OSCILLATOR, HIGH-POWER MODE, PIC16HV753 ONLY**

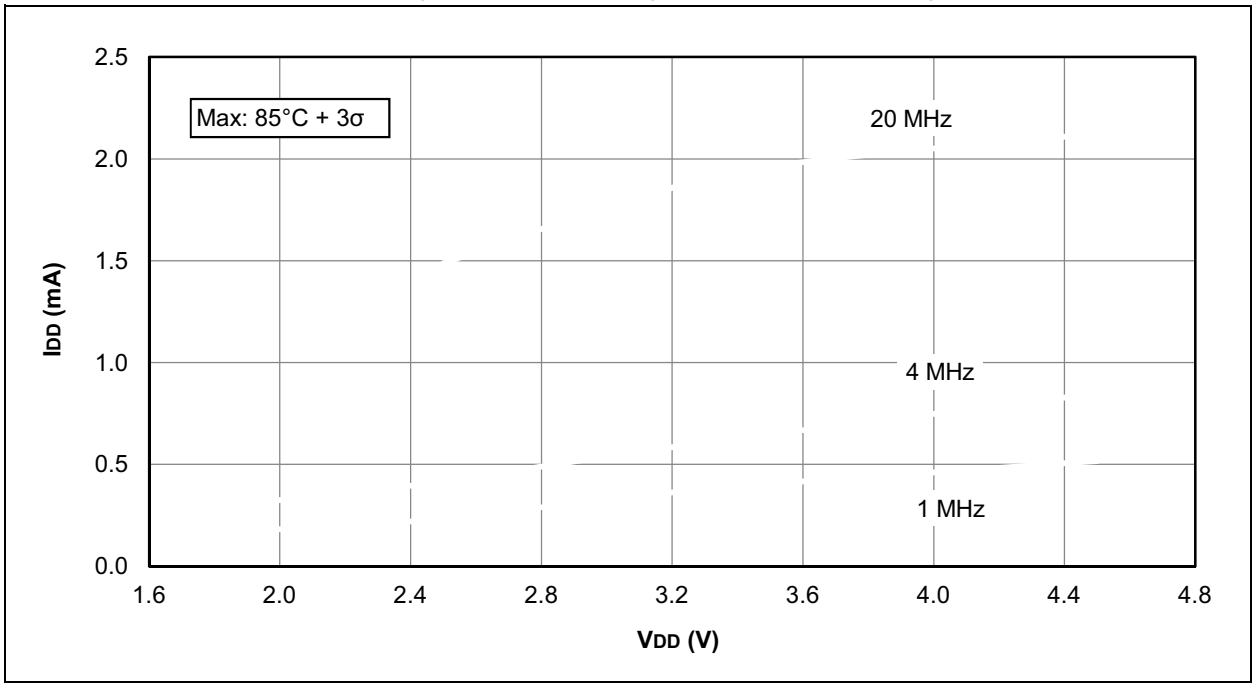


**FIGURE 23-16: IPD, WATCHDOG TIMER (WDT), PIC16HV753 ONLY**

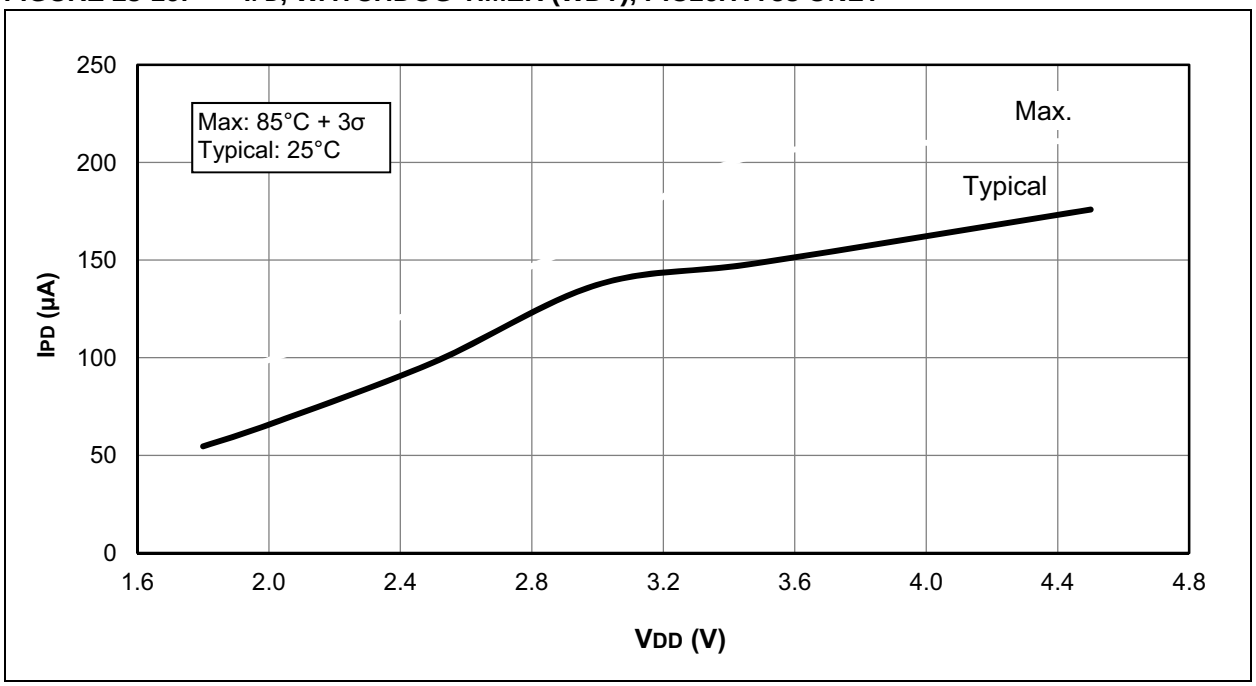
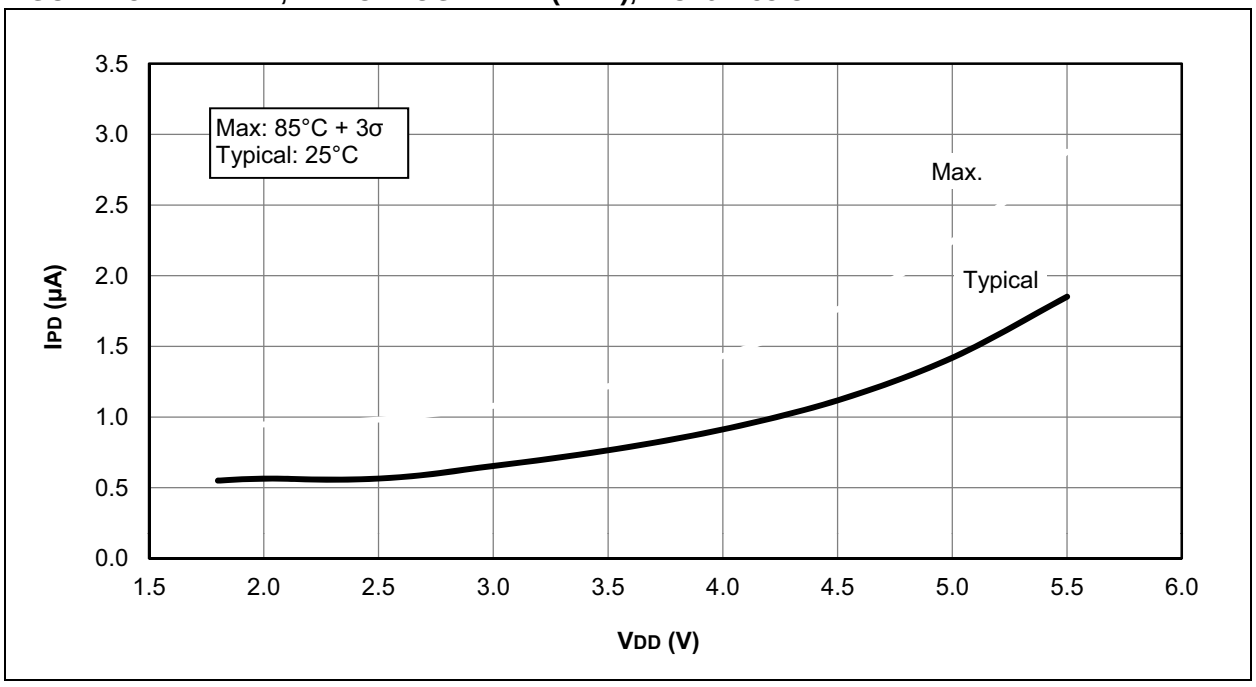
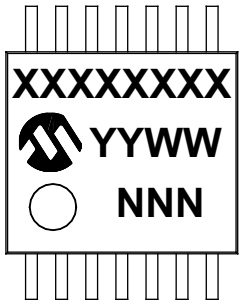



**FIGURE 23-17: IPD, WATCHDOG TIMER (WDT), PIC16F753 ONLY**

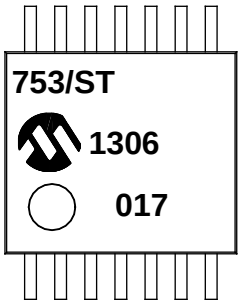


### 24.2 Package Marking Information

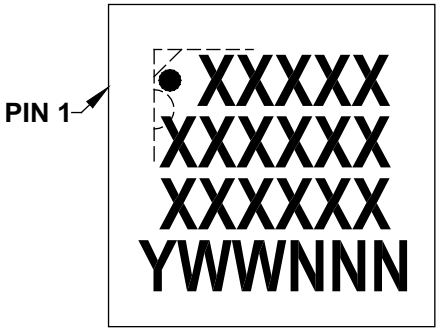
14-Lead TSSOP (4.4 mm)



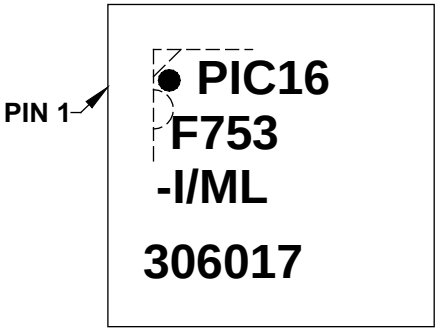

Example




16-Lead QFN (4x4x0.9 mm)




Example

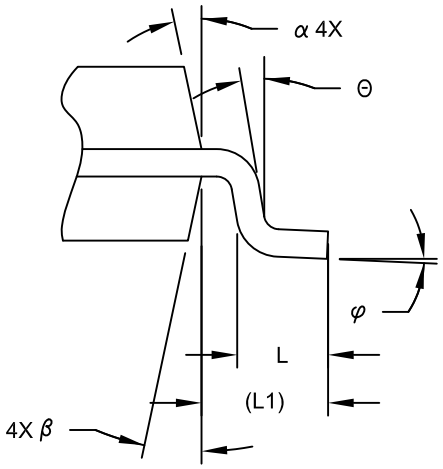


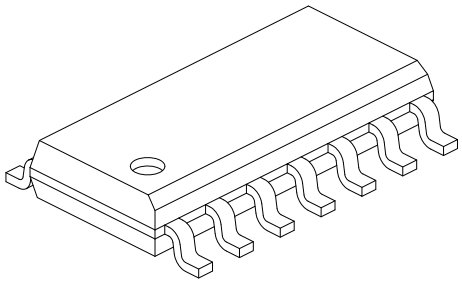

| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

### 14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



**VIEW C**

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 14 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | - | - | 1.75 |
| Molded Package Thickness | A2 | 1.25 | - | - |
| Standoff § | A1 | 0.10 | - | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 8.65 BSC | |
| Chamfer (Optional) | h | 0.25 | - | 0.50 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Lead Angle | Θ | 0° | - | - |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.10 | - | 0.25 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | 15° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

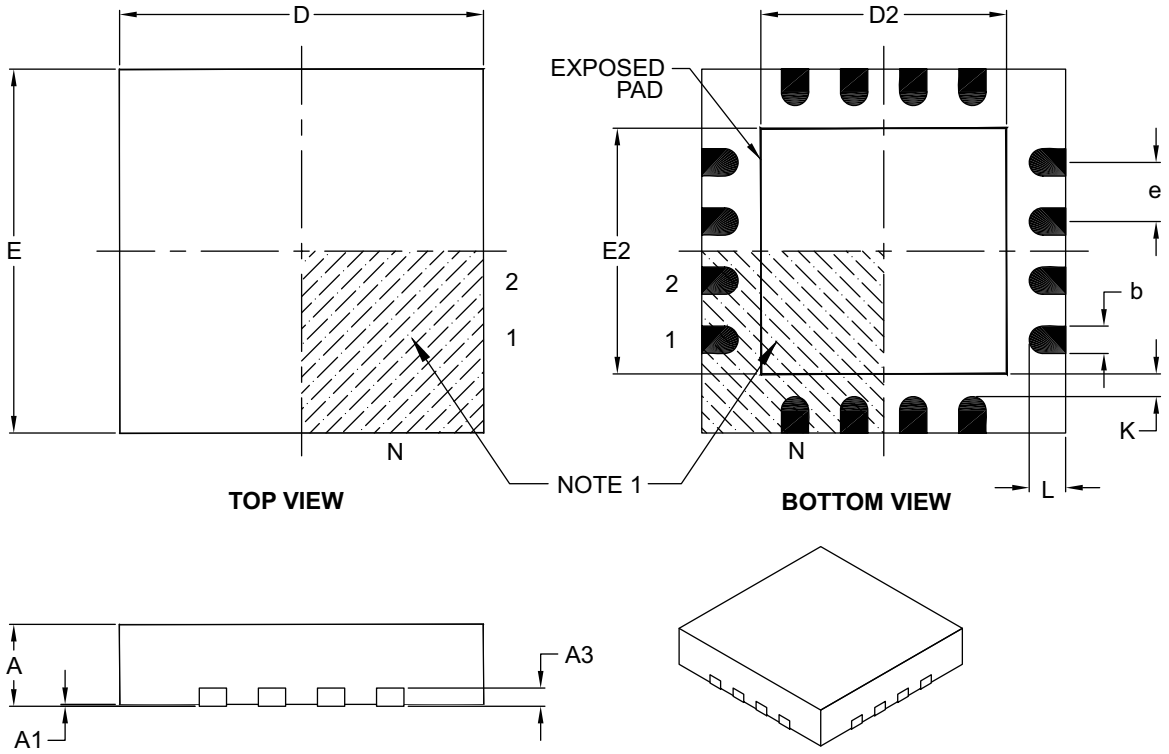
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

### 16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 16 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 4.00 BSC | |
| Exposed Pad Width | E2 | 2.50 | 2.65 | 2.80 |
| Overall Length | D | | 4.00 BSC | |
| Exposed Pad Length | D2 | 2.50 | 2.65 | 2.80 |
| Contact Width | b | 0.25 | 0.30 | 0.35 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B