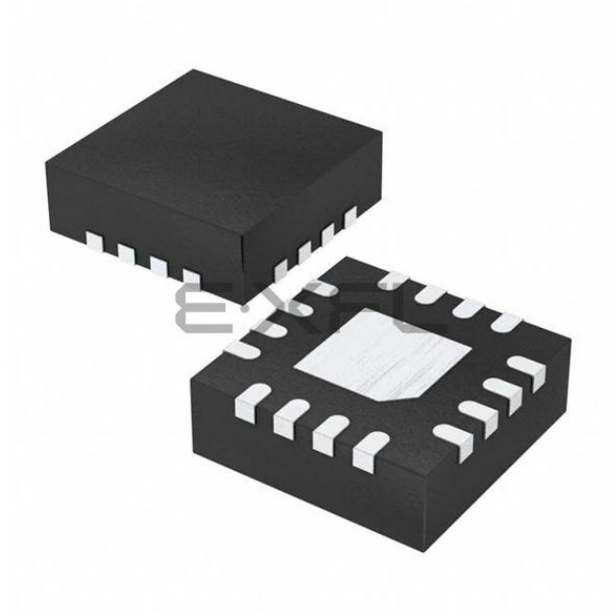

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b; D/A 1x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VQFN Exposed Pad
Supplier Device Package	16-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f753-i-ml

TABLE 2-1: PIC16F753/HV753 SPECIAL REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR	Value on all other Resets
Bank 0											
00h	INDF	INDF<7:0>								xxxx xxxx	xxxx xxxx
01h	TMR0	TMR0<7:0>								xxxx xxxx	uuuu uuuu
02h	PCL	PCL<7:0>								0000 0000	0000 0000
03h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	FSR<7:0>								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--uu uuuu
06h	—	Unimplemented								—	—
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	--uu uuuu
08h	IOCAF	—	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	--00 0000	--00 0000
09h	IOCCF	—	—	IOCCF5	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0	--00 0000	--00 0000
0Ah	PCLATH	—	—	—	PCLATH<4:0>					---0 0000	---0 0000
0Bh	INTCON	GIE	PEIE	T0IE	INTE	IOCIE	T0IF	INTF	IOCIF	0000 0000	0000 0000
0Ch	PIR1	TMR1GIF	ADIF	—	—	HLTMR2IF	HLTMR1IF	TMR2IF	TMR1IF	00--0000	00--0000
0Dh	PIR2	—	—	C2IF	C1IF	—	COG1IF	—	CCP1IF	--00 -0-0	--00 -0-0
0Eh	—	Unimplemented								—	—
0Fh	TMR1L	TMR1L<7:0>								xxxx xxxx	uuuu uuuu
10h	TMR1H	TMR1H<7:0>								xxxx xxxx	uuuu uuuu
11h	T1CON	TMR1CS<1:0>		T1CKPS<1:0>		T1OSCEN	$\overline{T1SYNC}$	—	TMR1ON	0000 00-0	0000 00-0
12h	T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{DONE}$	T1GVAL	T1GSS<1:0>		0000 0x00	0000 0x00
13h	CCPR1L	CCPR1L<7:0>								xxxx xxxx	uuuu uuuu
14h	CCPR1H	CCPR1H<7:0>								xxxx xxxx	uuuu uuuu
15h	CCP1CON	—	—	DC1B<1:0>		CCP1M<3:0>				--00 0000	--00 0000
16h	—	Unimplemented								—	—
17h	—	Unimplemented								—	—
18h	—	Unimplemented								—	—
19h	—	Unimplemented								—	—
1Ah	—	Unimplemented								—	—
1Bh	—	Unimplemented								—	—
1Ch	ADRESL	Least Significant two bits of the left shifted result or eight bits of the right shifted result								xxxx xxxx	uuuu uuuu
1Dh	ADRESH	Most Significant eight bits of the left shifted A/D result or two bits of the right shifted result								xxxx xxxx	uuuu uuuu
1Eh	ADCON0	ADFM	—	CHS<3:0>				GO/$\overline{DONE}$	ADON	0-00 0000	0-00 0000
1Fh	ADCON1	—	ADCS<2:0>			—	—	—	ADPREF1	-000 ---0	-000 ---0

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition shaded = unimplemented.

TABLE 2-3: PIC16F753/HV753 SPECIAL REGISTERS SUMMARY BANK 2

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR	Value on all other Resets
Bank 2											
100h	INDF	INDF<7:0>								xxxx xxxx	xxxx xxxx
101h	TMR0	TMR0<7:0>								xxxx xxxx	uuuu uuuu
102h	PCL	PCL<7:0>								0000 0000	0000 0000
103h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
104h	FSR	FSR<7:0>								xxxx xxxx	uuuu uuuu
105h	LATA	—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0	--xx -xxx	--uu -uuu
106h	—	Unimplemented								—	—
107h	LATC	—	—	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	--xx xxxx	--uu uuuu
108h	IOCAN	—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	--00 0000	--00 0000
109h	IOCCN	—	—	IOCCN5	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0	--00 0000	--00 0000
10Ah	PCLATH	—	—	—	PCLATH<4:0>					---0 0000	---0 0000
10Bh	INTCON	GIE	PEIE	T0IE	INTE	IOCIE	T0IF	INTF	IOCIF	0000 0000	0000 0000
10Ch	WPUA	—	—	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	--11 1111	--11 1111
10Dh	WPUC	—	—	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	--11 1111	--11 1111
10Eh	SLRCONC	—	—	SLRC5	SLRC4	—	—	—	—	--00 ----	--00 ----
10Fh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$	---- --qq	---- --uu
110h	TMR2	TMR2<7:0>								0000 0000	0000 0000
111h	PR2	PR2<7:0>								1111 1111	1111 1111
112h	T2CON	—	T2OUTPS<3:0>				TMR2ON	T2CKPS<1:0>		-000 0000	-000 0000
113h	HLTMR1	Holding Register for the 8-bit Hardware Limit Timer1 Count								0000 0000	0000 0000
114h	HLTPR1	HLTMR1 Module Period Register								1111 1111	1111 1111
115h	HLT1CON0	—	H1OUTPS<3:0>				H1ON	H1CKPS<1:0>		-000 0000	-000 0000
116h	HLT1CON1	H1FES	H1RES	—	H1ERS<2:0>			H1FEREN	H1REREN	11-0 0000	11-0 0000
117h	HLTMR2	Holding Register for the 8-bit Hardware Limit Timer2 Count								0000 0000	0000 0000
118h	HLTPR2	HLTMR2 Module Period Register								1111 1111	1111 1111
119h	HLT2CON0	—	H2OUTPS<3:0>				H2ON	H2CKPS<1:0>		-000 0000	-000 0000
11Ah	HLT2CON1	H2FES	H2RES	—	H2ERS<2:0>			H2FEREN	H2REREN	11-0 0000	11-0 0000
11Bh	—	Unimplemented								—	—
11Ch	—	Unimplemented								—	—
11Dh	—	Unimplemented								—	—
11Eh	SLPCCON0	SC1EN	—	—	SC1POL	SC1TSS<1:0>		—	SC1INS	0-00 00-0	0-00 00-0
11Fh	SLPCCON1	—	—	—	SC1RNG	SC1ISET<3:0>				---0 0000	---0 0000

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition shaded = unimplemented.

TABLE 3-1: SUMMARY OF REGISTERS ASSOCIATED WITH FLASH PROGRAM MEMORY

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PMCON1	—	—	—	—	—	WREN	WR	RD	27
PMCON2	Program Memory Control Register 2								27
PMADRL	PMADRL<7:0>								26
PMADRH	—	—	—	—	—	—	PMADRH<1:0>		26
PMDATL	PMDATL<7:0>								26
PMDATH	—	—	PMDATH<5:0>						26
INTCON	GIE	PEIE	T0IE	INTE	IOCIE	T0IF	INTF	IOCIF	17

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Flash program memory module.
* Page provides register information.

TABLE 3-2: SUMMARY OF CONFIGURATION WORD WITH FLASH PROGRAM MEMORY

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG(1)	13:8	—	—	$\overline{\text{DEBUG}}$	$\overline{\text{CLKOUTEN}}$	WRT<1:0>		BOREN<1:0>		150
	7:0	—	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	—	—	FOSC0	

Legend: — = unimplemented location, read as '1'. Shaded cells are not used by Flash program memory.
Note 1: See Configuration Word register (Register 19-1) for operation of all register bits.

5.3 PORTA and TRISA Registers

PORTA is a 6-bit wide port with five bidirectional and one input-only pin. The corresponding data direction register is TRISA (Register 5-2). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., disable the output driver). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). The exception is RA3, which is input-only and its TRIS bit will always read as '1'. Example 5-1 shows how to initialize PORTA.

Reading the PORTA register (Register 5-2) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch. RA3 reads '0' when MCLRE = 1.

The TRISA register controls the direction of the PORTA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

Note:	The ANSEL register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0' and cannot generate an interrupt.

5.3.1 PORTA FUNCTIONS AND OUTPUT PRIORITIES

Each PORTA pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in Table 5-1.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the highest priority.

Analog input functions, such as comparator inputs, are not shown in the priority lists. These inputs are active when the peripheral is enabled and the input multiplexer for the pin is selected. The Analog mode, set with the ANSELA register, disables the digital input buffer thereby preventing excessive input current when the analog input voltage is between logic states. Digital output functions may control the pin when it is in Analog mode with the priority shown in Table 5-1.

TABLE 5-1: PORTA OUTPUT PRIORITY

Pin Name	Function Priority
RA0	ICSPDAT FVROUT DACOUT C1IN0+ RA0
RA1	FVRIN ICSPCLK V_{REF+} C1IN0- C2IN0- RA1
RA2	COG1FLT T0CKI C1OUT INT RA2
RA3	$\overline{MCLR}$ V_{PP} T1G RA3
RA4	CLKOUT T1G RA4
RA5	CLKIN T1CKI RA5

5.4 Additional Pin Functions

Every PORTA pin on the PIC16F753 has an interrupt-on-change option and a weak pull-up option. The next three sections describe these functions.

5.4.1 ANSELA REGISTER

The ANSELA register (Register 5-5) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELA bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

5.4.2 WEAK PULL-UPS

Each of the PORTA pins, except RA3, has an individually configurable internal weak pull-up. Control bits WPUx enable or disable each pull-up. Refer to Register 5-6. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the $\overline{\text{RAPU}}$ bit of the OPTION_REG register. A weak pull-up is automatically enabled for RA3 when configured as $\overline{\text{MCLR}}$ and disabled when RA3 is an I/O. There is no software control of the $\overline{\text{MCLR}}$ pull-up.

5.4.3 INTERRUPT-ON-CHANGE

Each PORTA pin is individually configurable as an interrupt-on-change pin. Control bits IOCA enable or disable the interrupt function for each pin. Refer to Register 5-7. The interrupt-on-change is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of PORTA. The 'mismatch' outputs of the last read are OR'd together to set the PORTA Change Interrupt Flag bit (IOCIF) in the INTCON register (Register 2-3).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, clears the interrupt by:

a) Any read of PORTA AND Clear flag bit IOCIF. This will end the mismatch condition;

   OR

b) Any write of PORTA AND Clear flag bit IOCIF will end the mismatch condition;

A mismatch condition will continue to set flag bit IOCIF. Reading PORTA will end the mismatch condition and allow flag bit IOCIF to be cleared. The latch holding the last read value is not affected by a $\overline{\text{MCLR}}$ nor BOR Reset. After these Resets, the IOCIF flag will continue to be set if a mismatch is present.

Note:	If a change on the I/O pin should occur when any PORTA operation is being executed, then the IOCIF interrupt flag may not get set.

7.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing counter which is accessed through the TMR1H:TMR1L register pair. Writes to TMR1H or TMR1L directly update the counter.

When used with an internal clock source, the module is a timer and increments on every instruction cycle. When used with an external clock source, the module can be used as either a timer or counter and increments on every selected edge of the external source.

Timer1 is enabled by configuring the TMR1ON and TMR1GE bits in the T1CON and T1GCON registers, respectively. Table 7-1 displays the Timer1 enable selections.

TABLE 7-1: TIMER1 ENABLE SELECTIONS

TMR1ON	TMR1GE	Timer1 Operation
0	0	Off
0	1	Off
1	0	Always On
1	1	Count Enabled

7.2 Clock Source Selection

The TMR1CS<1:0> bits of the T1CON register are used to select the clock source for Timer1. Table 7-2 displays the clock source selections.

TABLE 7-2: CLOCK SOURCE SELECTIONS

TMR1CS<1:0>	Clock Source
11	Temperature Sense Oscillator
10	External Clocking on T1CKI Pin
01	System Clock (FOSC)
00	Instruction Clock (FOSC/4)

7.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, the TMR1H:TMR1L register pair will increment on multiples of FOSC or FOSC/4 as determined by the Timer1 prescaler.

7.2.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1 module may work as a timer or a counter. When enabled to count, Timer1 is incremented on the rising edge of the external clock input T1CKI.

Note: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge (see Figure 7-2) after any one or more of the following conditions:

- Timer1 enabled after POR Reset
- Write to TMR1H or TMR1L
- Timer1 is disabled
- Timer1 is disabled (TMR1ON = 0) when T1CKI is high then Timer1 is enabled (TMR1ON = 1) when T1CKI is low.

7.2.3 WDT OSCILLATOR

When the Watchdog is selected, Timer 1 will use the LFINTOSC that is used to operate the Watchdog Timer. This is the same oscillator as the LFINTOSC used as the system clock. Selecting this option will enable the oscillator even when the LFINTOSC or the Watchdog are not in use. This oscillator will continue to operate when in Sleep mode.

9.1 HLT Operation

The clock input to the HLT module is the system instruction clock (FOSC/4). HLTMRx increments on each rising clock edge.

A 4-bit counter/prescaler on the clock input provides the following prescale options:

- Direct input
- Divide-by-4
- Divide-by-16
- Divide-by-64

The prescale options are selected by the prescaler control bits, HxCKPS<1:0> of the HLTxCON0 register.

The value of HLTMRx is compared to that of the Period register, HLTPRx, on each clock cycle. When the two values match, then the comparator generates a match signal as the HLTimerx output. This signal also resets the value of HLTMRx to 00h on the next clock rising edge and drives the output counter/postscaler (see **Section 9.2 "HLT Interrupt"**).

The HLTMRx and HLTPRx registers are both directly readable and writable. The HLTMRx register is cleared on any device Reset, whereas the HLTPRx register initializes to FFh. Both the prescaler and postscaler counters are cleared on any of the following events:

- A write to the HLTMRx register
- A write to the HLTxCON0 register
- Power-on Reset (POR)
- Brown-out Reset (BOR)
- $\overline{\text{MCLR}}$ Reset
- Watchdog Timer (WDT) Reset
- Stack Overflow Reset
- Stack Underflow Reset
- RESET Instruction

Note:	HLTMRx is not cleared when HLTxCON0 is written.

9.2 HLT Interrupt

The HLT can also generate an optional device interrupt. The HLTMRx output signal (HLTMRx-to-HLTPRx match) provides the input for the 4-bit counter/postscaler. The overflow output of the postscaler sets the HLTMRxIF bit of the PIR1 register. The interrupt is enabled by setting the HLTMRx Match Interrupt Enable bit, HLTMRxIE of the PIE1 register.

A range of 16 postscale options (from 1:1 through 1:16 inclusive) can be selected with the postscaler control bits, HxOUTPS<3:0>, of the HLTxCON0 register.

9.3 Peripheral Resets

Resets driven from the selected peripheral output prevents the HLTMRx from matching the HLTPRx register and generating an output. In this manner, the HLT can be used as a hardware time limit to other peripherals.

In this device, the primary purpose of the HLT is to limit the COG PWM duty cycle. Normally, the COG operation uses analog feedback to determine the PWM duty cycle. The same feedback signal is used as an HLT Reset input. The HLTPRx register is set to occur at the maximum allowed duty cycle. If the analog feedback to the COG exceeds the maximum time, then an HLTMRx-to-HLTPRx match will occur and generate the output needed to limit the COG drive output.

The HLTMRx can be reset by one of several selectable peripheral sources. Reset inputs include:

- CCP1 output
- Comparator 1 output
- Comparator 2 output
- COGxFLT pin
- COG1OUT0
- COG1OUT1

The external Reset input is selected with the HxERS<2:0> bits of the HLTxCON1 register. High and low Reset enables are selected with the HxREREN and HxFEREN bits, respectively. Setting the HxRES and HxFES bits makes the respective rising and falling Reset events edge sensitive. Reset inputs that are not edge sensitive are level sensitive.

HLTMRx Resets are synchronous with the HLT clock. In other words, HLTMRx is cleared on the rising edge of the HLT clock after the enabled Reset event occurs.

If an enabled external Reset occurs at the same time a write occurs to the TMR4A register, the write to the timer takes precedence and pending Resets are cleared.

9.4 HLTimerx Output

The unscaled output of HLTMRx is available only to the COG module, where it is used as a selectable limit to the maximum COG period.

9.5 HLT Operation During Sleep

The HLT cannot be operated while the processor is in Sleep mode. The contents of the HLTMRx register will remain unchanged while the processor is in Sleep mode.

10.2.5 COMPARE DURING SLEEP

The Compare mode is dependent upon the system clock (FOSC) for proper operation. Since FOSC is shut down during Sleep mode, the Compare mode will not function properly during Sleep.

TABLE 10-3: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CCP1CON	—	—	DC1B<1:0>		CCP1M<3:0>				80
CCPR1L	CCPR1L<7:0>								74
CCPR1H	CCPR1H<7:0>								74
INTCON	GIE	PEIE	T0IE	INTE	IOCIE	T0IF	INTF	IOCIF	17
PIE1	TMR1-GIE	ADIE	—	—	HLTMR2IE	HLTMR1IE	TMR2IE	TMR1IE	18
PIE2	—	—	C2IE	C1IE	—	COG1IE	—	CCP1IE	19
PIR1	TMR1-GIF	ADIF	—	—	HLTMR2IF	HLTMR1IF	TMR2IF	TMR1IF	20
PIR2	—	—	C2IF	C1IF	—	COG1IF	—	CCP1IF	21
T1CON	TMR1CS<1:0>		T1CKPS<1:0>		T1OSCEN	$\overline{\text{T1SYNC}}$	—	TMR1ON	65
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{DONE}}$	T1GVAL	T1GSS<1:0>		66
TMR1H	TMR1H<7:0>								57*
TMR1L	TMR1L<7:0>								57*
TRISA	—	—	TRISA5	TRISA4	TRISA3(1)	TRISA2	TRISA1	TRISA0	43

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by Compare mode.

* Page provides register information.

Note 1: TRISA3 always reads '1'.

When the phase delay count value is zero, phase delay is disabled and the phase delay counter output is true, thereby allowing the event signal to pass straight through to complementary output driver flop.

11.7.1 CUMULATIVE UNCERTAINTY

It is not possible to create more than one COG_clock of uncertainty by successive stages. Consider that the phase delay stage comes after the blanking stage, the dead-band stage comes after either the blanking or phase delay stages, and the blanking stage comes after the dead-band stage. When the preceding stage is enabled, the output of that stage is necessarily synchronous with the COG_clock, which removes any possibility of uncertainty in the succeeding stage.

EQUATION 11-1: PHASE, DEAD-BAND AND BLANKING TIME CALCULATION

$$T_{\text{min}} = \frac{\text{Count}}{F_{COG\_clock}}$$

$$T_{\text{max}} = \frac{\text{Count} + 1}{F_{COG\_\text{clock}}}$$

$$T_{\text{uncertainty}} = T_{\text{max}} - T_{\text{min}}$$

Also:

$$T_{\text{uncertainty}} = \frac{1}{F_{COG\_\text{clock}}}$$

Where:

T	Count
Rising Phase Delay	COGxPHR
Falling Phase Delay	COGxPHF
Rising Dead Band	COGxDBR
Falling Dead Band	COGxDBF
Rising Event Blanking	COGxBKR
Falling Event Blanking	COGxBKF

EQUATION 11-2: TIMER UNCERTAINTY

Given:

$$Count = Ah = 10d$$

$$F_{COG\_\text{Clock}} = 8\text{MHz}$$

Therefore:

$$T_{\text{uncertainty}} = \frac{1}{F_{COG\_\text{clock}}}$$

$$= \frac{1}{8MHz} = 125ns$$

Proof:

$$T_{\text{min}} = \frac{Count}{F_{COG\_\text{clock}}}$$

$$= 125ns \bullet 10d = 1.25\mu s$$

$$T_{\text{max}} = \frac{Count + 1}{F_{COG\_\text{clock}}}$$

$$= 125ns \bullet (10d + 1)$$

$$= 1.375\mu s$$

Therefore:

$$T_{\text{uncertainty}} = T_{\text{max}} - T_{\text{min}}$$

$$= 1.375\mu s - 1.25\mu s$$

$$= 125ns$$

REGISTER 11-4: COGxRSIM: COG RISING EVENT SOURCE INPUT MODE REGISTER

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	GxRMHLT2	GxRMHLT1	GxRMT2M	GxRMFLT	GxRMCCP1	GxRMC2	GxRMC1
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **Unimplemented:** Read as '0'

bit 6 **GxRMHLT2:** COGx Rising Event Input Source 6 Mode bit(1)
GxRIHLT2 = 1:
1 = HLTimer2 low-to-high transition will cause a rising event after rising event phase delay
0 = HLTimer2 high level will cause an immediate rising event
GxRIHLT2 = 0:
HLTimer2 has no effect on rising event

bit 5 **GxRMHLT1:** COGx Rising Event Input Source 5 Mode bit(1)
GxRIHLT1 = 1:
1 = HLTimer1 low-to-high transition will cause a rising event after rising event phase delay
0 = HLTimer1 high level will cause an immediate rising event
GxRIHLT1 = 0:
HLTimer1 has no effect on rising event

bit 4 **GxRMT2M:** COGx Rising Event Input Source 4 Mode bit(1)
GxRIT2M = 1:
1 = Timer2 match with PR2 low-to-high transition will cause a rising event after rising event phase delay
0 = Timer2 match with PR2 high level will cause an immediate rising event
GxRIT2M = 0:
Timer2 match with PR2 has no effect on rising event

bit 3 **GxRMFLT:** COGx Rising Event Input Source 3 Mode bit
GxRIFLT = 1:
1 = COGxFLT pin low-to-high transition will cause a rising event after rising event phase delay
0 = COGxFLT pin high level will cause an immediate rising event
GxRIFLT = 0:
COGxFLT pin has no effect on rising event

bit 2 **GxRMCCP1:** COGx Rising Event Input Source 2 Mode bit
GxRICCP1 = 1:
1 = CCP1 low-to-high transition will cause a rising event after rising event phase delay
0 = CCP1 high level will cause an immediate rising event
GxRICCP1 = 0:
CCP1 has no effect on rising event

bit 1 **GxRMC2:** COGx Rising Event Input Source 1 Mode bit
GxRIC2 = 1:
1 = Comparator 2 low-to-high transition will cause a rising event after rising event phase delay
0 = Comparator 2 high level will cause an immediate rising event
GxRIC2 = 0:
Comparator 2 has no effect on rising event

bit 0 **GxRMC1:** COGx Rising Event Input Source 0 Mode bit
GxRIC1 = 1:
1 = Comparator 1 low-to-high transition will cause a rising event after rising event phase delay
0 = Comparator 1 high level will cause an immediate rising event
GxRIC1 = 0:
Comparator 1 has no effect on rising event

Note 1: These sources are pulses and therefore the only benefit of Edge mode over Level mode is that they can be delayed by rising event phase delay.

REGISTER 11-5: COGxFIS: COG FALLING EVENT INPUT SELECTION REGISTER

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	GxFIHLT2	GxFIHLT1	GxFIT2M	GxFIFLT	GxFICCP1	GxFIC2	GxFIC1
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **GxFIHLT2:** COGx Falling Event Input Source 6 Enable bit
1 = HLTimer2 output is enabled as a falling event input
0 = HLTimer2 has no effect on the falling event

bit 5 **GxFIHLT1:** COGx Falling Event Input Source 5 Enable bit
1 = HLTimer1 output is enabled as a falling event input
0 = HLTimer1 has no effect on the falling event

bit 4 **GxFIT2M:** COGx Falling Event Input Source 4 Enable bit
1 = Timer2 match with PR2 is enabled as a falling event input
0 = Timer2 match with PR2 has no effect on the falling event

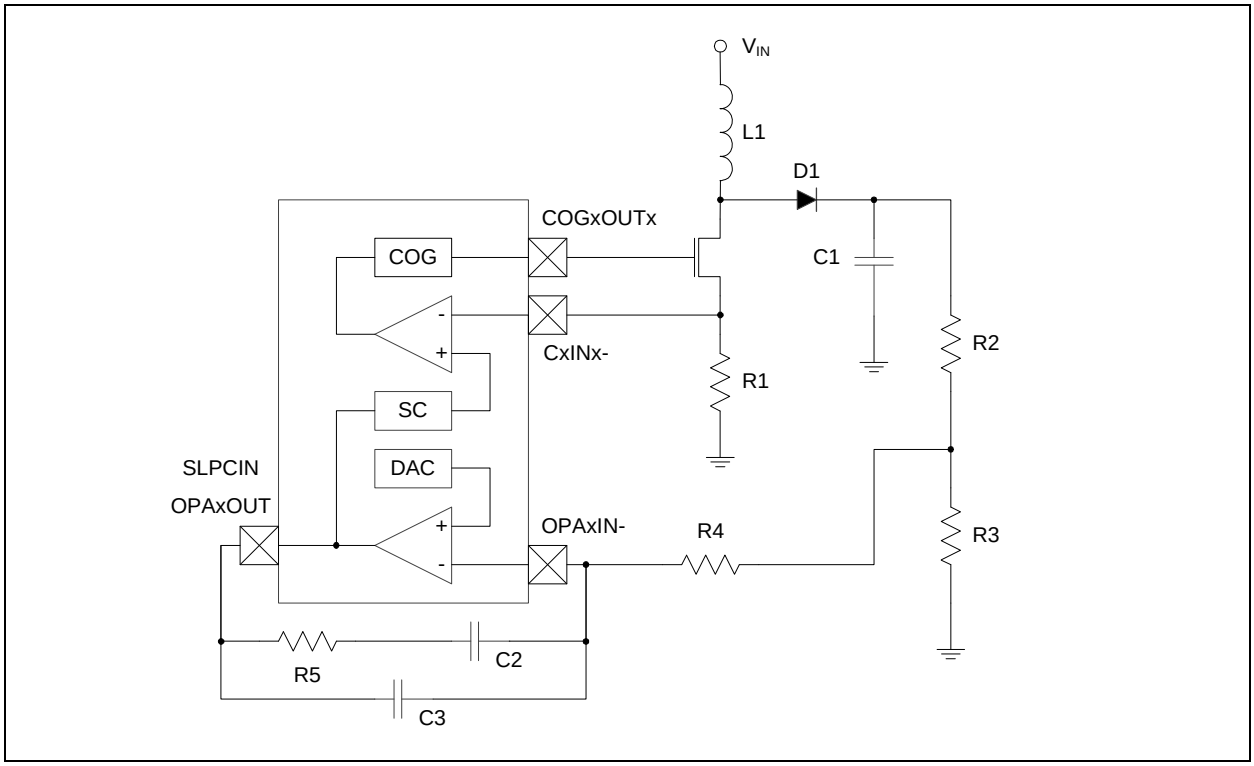
bit 3 **GxFIFLT:** COGx Falling Event Input Source 3 Enable bit
1 = COGxFLT pin is enabled as a falling event input
0 = COGxFLT pin has no effect on the falling event

bit 2 **GxFICCP1:** COGx Falling Event Input Source 2 Enable bit
1 = CCP1 output is enabled as a falling event input
0 = CCP1 has no effect on the falling event

bit 1 **GxFIC2:** COGx Falling Event Input Source 1 Enable bit
1 = Comparator 2 output is enabled as a falling event input
0 = Comparator 2 output has no effect on the falling event

bit 0 **GxFIC1:** COGx Falling Event Input Source 0 Enable bit
1 = Comparator 1 output is enabled as a falling event input
0 = Comparator 1 output has no effect on the falling event

FIGURE 17-3: EXAMPLE SLOPE COMPENSATION CIRCUIT



17.3 Inputs

The SC module connects to the following inputs:

- COG1
- COG2
- Comparator C1
- Comparator C2

17.4 Outputs

The SC module connects to the following outputs:

- Comparator C1
- Comparator C2
- Op amp

17.5 Operation During Sleep

The SC module is unaffected by Sleep.

17.6 Effects of a Reset

The SC module resets to a disabled condition.

DECFSZ	Decrement f, Skip if 0
Syntax:	[*label*] DECFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 → (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a 2-cycle instruction.

GOTO	Unconditional Branch
Syntax:	[*label*] GOTO k
Operands:	$0 \le k \le 2047$
Operation:	k → PC<10:0> PCLATH<4:3> → PC<12:11>
Status Affected:	None
Description:	GOTO is an unconditional branch. The 11-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a 2-cycle instruction.

INCF	Increment f
Syntax:	[*label*] INCF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 → (destination)
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

INCFSZ	Increment f, Skip if 0
Syntax:	[*label*] INCFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 → (destination), skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2-cycle instruction.

IORLW	Inclusive OR literal with W
Syntax:	[*label*] IORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .OR. k → (W)
Status Affected:	Z
Description:	The contents of the W register are OR'ed with the 8-bit literal 'k'. The result is placed in the W register.

IORWF	Inclusive OR W with f
Syntax:	[*label*] IORWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .OR. (f) → (destination)
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

TABLE 22-3: POWER-DOWN CURRENTS (I_{PD}) (CONTINUED)(1,2)

PIC16F753		Standard Operating Conditions (unless otherwise stated) Sleep mode						
PIC16HV753								
Param No.	Device Characteristics	Min.	Typ†	Max. 85°C	Max. 125°C	Units	Conditions	
							V_{DD}	Note
	Power-down Base Current (I_{PD})(2, 3)							
D025		—	0.10	0.41	3.51	µA	3.0	A/D Current(1), no conversion in progress
		—	0.12	0.55	4.41	µA	5.0	
D025		—	145	171	175	µA	3.0	
		—	185	226	231	µA	4.5	
D026		—	20	37	37	µA	2.0	DAC Current(1)
		—	30	46	46	µA	3.0	
		—	50	76	76	µA	5.0	
D026		—	85	155	155	µA	2.0	
		—	165	213	213	µA	3.0	
		—	215	284	284	µA	4.5	
D027		—	115	185	203	µA	2.0	FVR Current(1), FVRBUFEN = 1, FVROUT buffer enabled
		—	120	193	219	µA	3.0	
		—	125	196	224	µA	5.0	
D027		—	65	126	145	µA	2.0	
		—	136	171	182	µA	3.0	
		—	175	226	231	µA	4.5	
D028		—	1	2	4	µA	2.0	T1OSC Current, TMR1CS <1:0> = 11
		—	2	3	5	µA	3.0	
		—	9	20	21	µA	5.0	
D028		—	65	126	140	µA	2.0	
		—	136	172	180	µA	3.0	
		—	175	228	235	µA	4.5	
D029		—	140	258	265	µA	2.0	Op-Amp Current(1)
		—	155	326	340	µA	3.0	
		—	165	421	422	µA	5.0	
D029		—	140	260	265	µA	2.0	
		—	155	325	340	µA	3.0	
		—	165	400	410	µA	4.5	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral Δ current can be determined by subtracting the base I_{PD} current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{SS}.

3: Shunt regulator is always ON and always draws operating current.

TABLE 22-4: I/O PORTS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
		Capacitive Loading Specs on Output Pins					
D101*	COSC2	OSC2 pin	—	—	15	pF	In XT, HS, LP modes when external clock is used to drive OSC1
D101A*	CIO	All I/O pins	—	—	50	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Negative current is defined as current sourced by the pin.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: This specification applies to all weak pull-up pins, including the weak pull-up found on RA3/$\overline{MCLR}$. When RA3/$\overline{MCLR}$ is configured as $\overline{MCLR}$ Reset pin, the weak pull-up is always enabled.

TABLE 22-5: MEMORY PROGRAMMING SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
		Program Memory Programming Specifications					
D110	V_{IHH}	Voltage on $\overline{MCLR}$/V_{PP} pin	10.0	—	13.0	V	**(Note 2)**
D112	V_{BE}	V_{DD} for Bulk Erase	4.5	—	V_{DDMAX}	V	
D113	V_{PEW}	V_{DD} for Write or Row Erase	4.5	—	V_{DDMAX}	V	
D114	I_{PPPGM}	Current on $\overline{MCLR}$/V_{PP} during Erase/Write	—	300	1000	μA	
		Program Flash Memory					
D121	E_P	Cell Endurance	10K	100K	—	E/W	-40°C ≤ T_A ≤ +85°C **(Note 1)**
D121A	E_P	Cell Endurance	1K	10K	—	E/W	-40°C ≤ T_A ≤ +125°C **(Note 1)**
D122	V_{PRW}	V_{DD} for Read/Write	V_{DDMIN}	—	V_{DDMAX}	V	
D123	T_{IW}	Self-timed Write Cycle Time	—	2	2.5	ms	
D124	T_{RETD}	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D125	E_{HEFC}	High-Endurance Flash Cell	N/A	—	—	E/W	0°C to +60°C, Lower byte last 128 addresses

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Self-write and Block Erase.

2: Required only if single-supply programming is disabled.

FIGURE 22-8: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

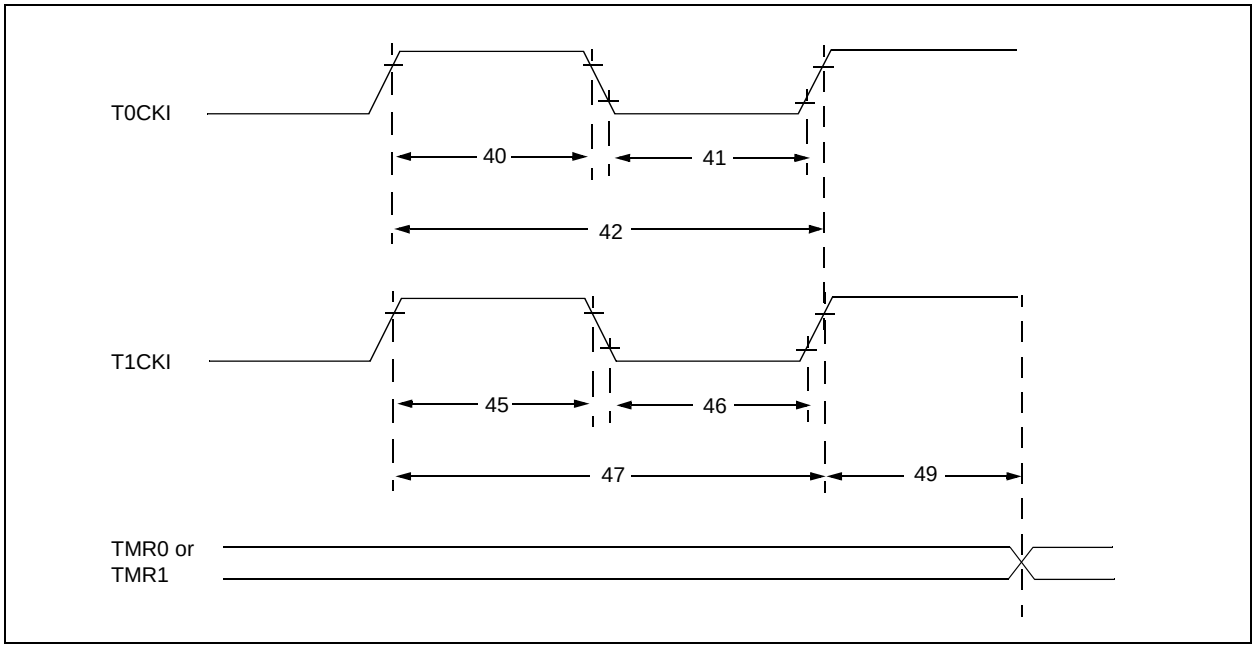


TABLE 22-11: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)								
Param No.	**Sym.**	**Characteristic**		**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
40*	TT0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	TT0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	TT0P	T0CKI Period		Greater of: 20 or TCY + 40 / N	—	—	ns	N = prescale value
45*	TT1H	T1CKI High Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
46*	TT1L	T1CKI Low Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
47*	TT1P	T1CKI Input Period	Synchronous	Greater of: 30 or TCY + 40 / N	—	—	ns	N = prescale value
			Asynchronous	60	—	—	ns	
49*	TCKEZT-MR1	Delay from External Clock Edge to Timer Increment		2 TOSC	—	7 TOSC	—	Timers in Sync mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 23-3: IDD TYPICAL, EC OSCILLATOR, MEDIUM-POWER MODE, PIC16F753 ONLY

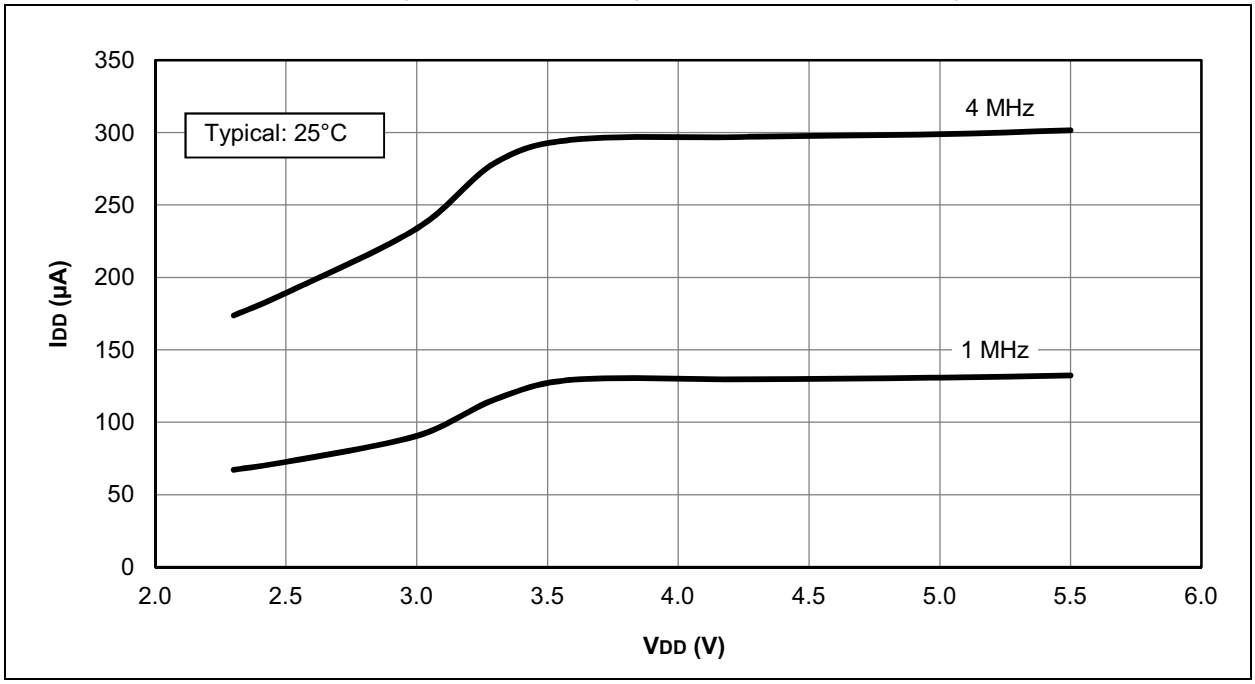


FIGURE 23-4: IDD MAXIMUM, EC OSCILLATOR, MEDIUM-POWER MODE, PIC16F753 ONLY

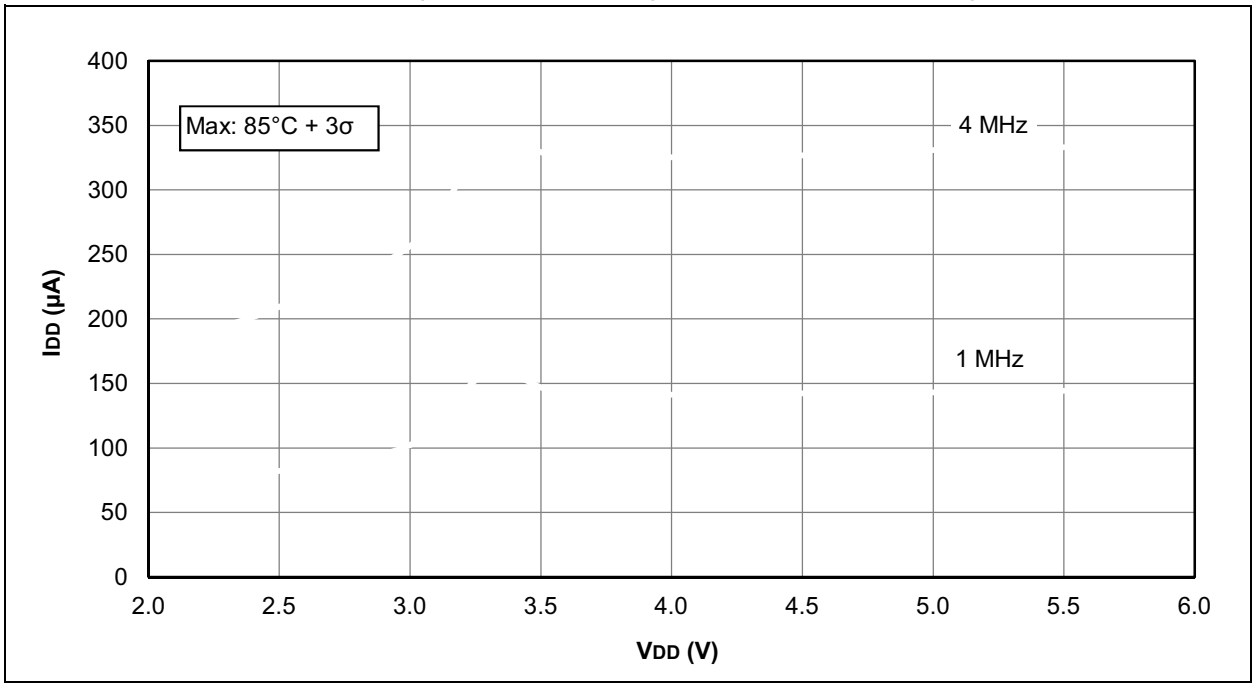


FIGURE 23-11: IDD TYPICAL, HFINTOSC, PIC16HV753 ONLY

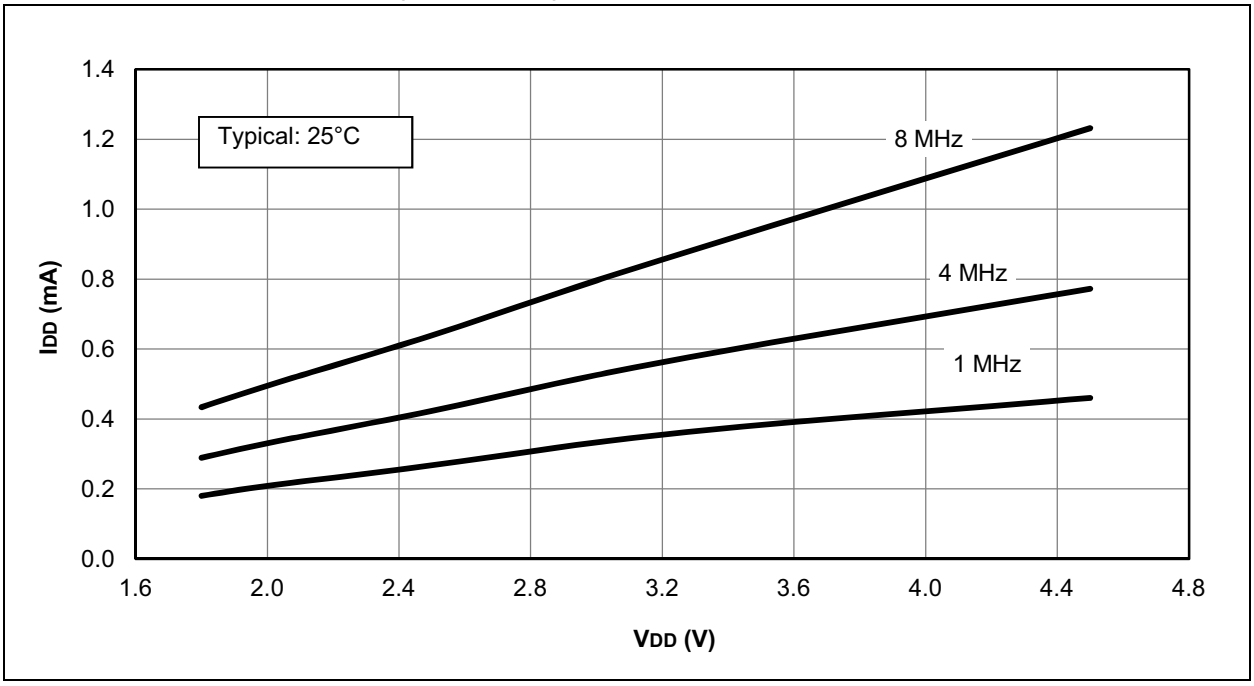


FIGURE 23-12: IDD MAXIMUM, HFINTOSC, PIC16HV753 ONLY

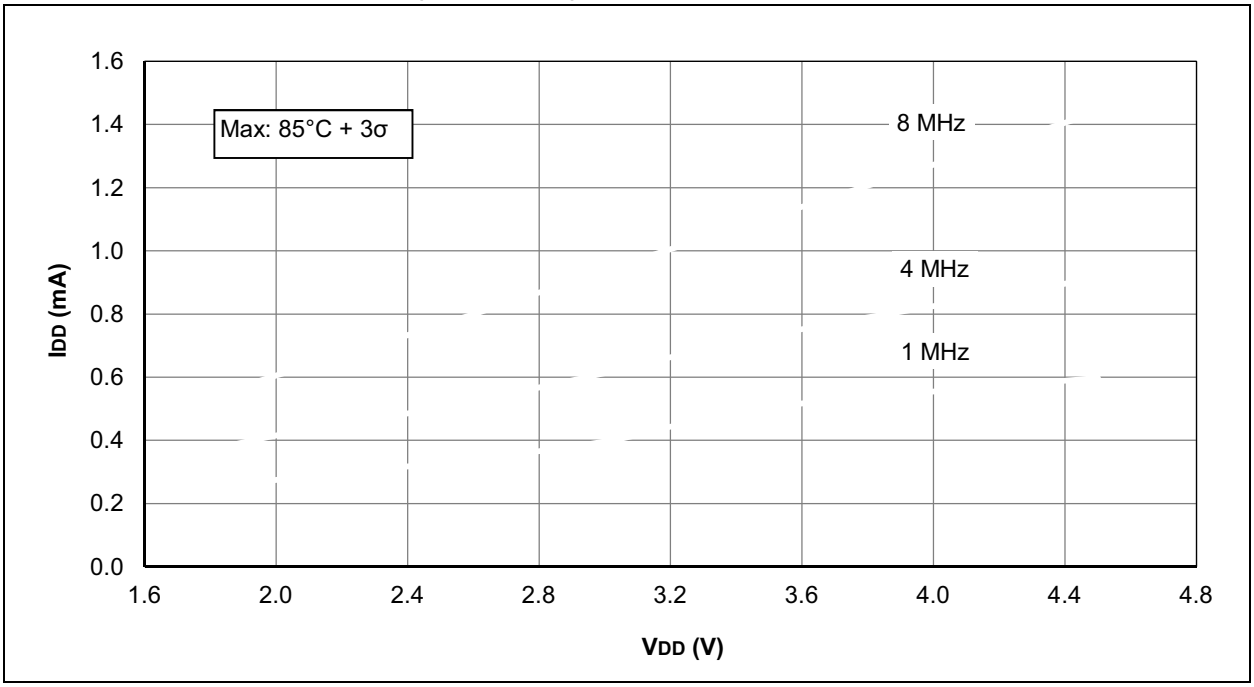


FIGURE 23-30: IPD, COMPARATOR, LOW-POWER MODE, PIC16HV753 ONLY

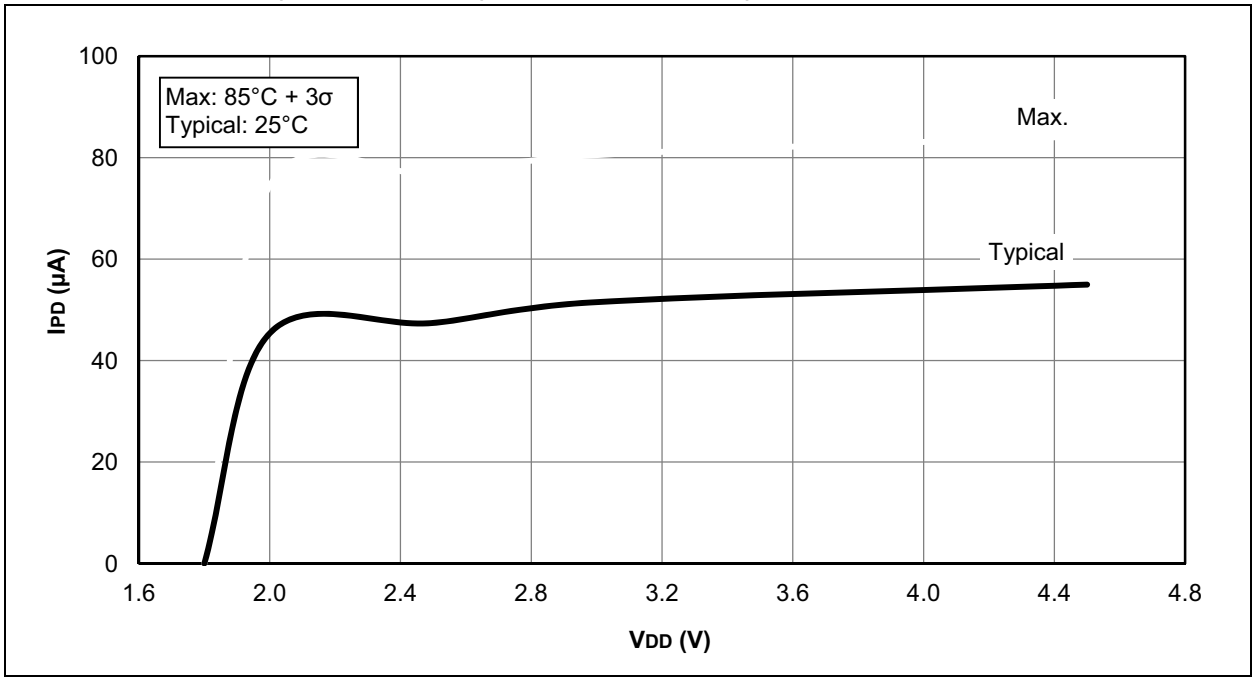
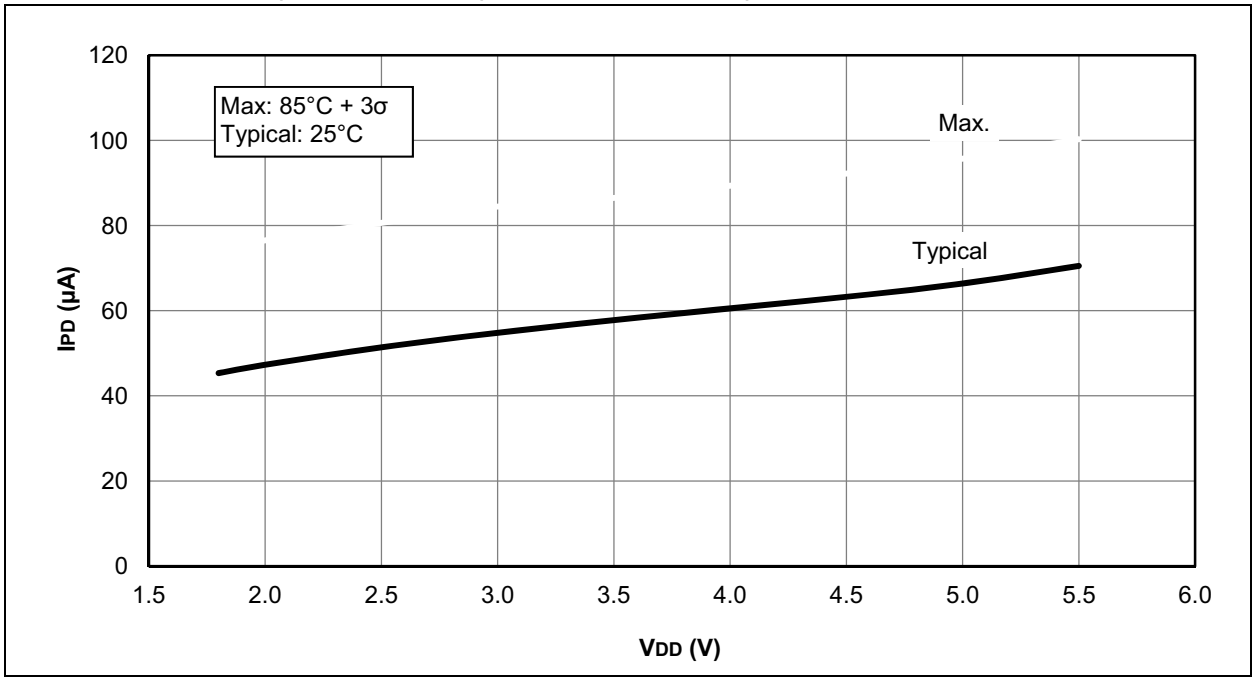
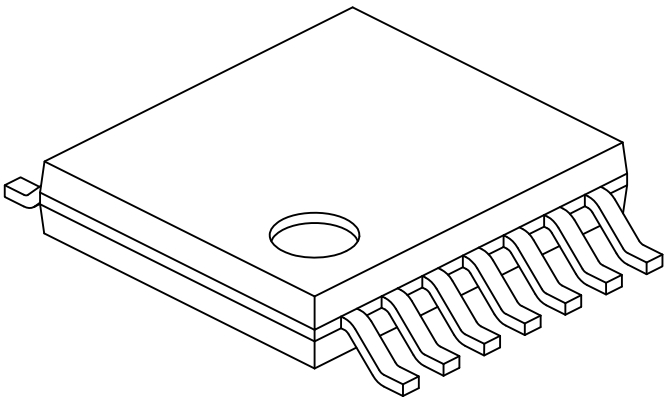


FIGURE 23-31: IPD, COMPARATOR, LOW-POWER MODE, PIC16F753 ONLY



14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)		1.00 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2