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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b; D/A 1x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f753-i-sl

2.3 Global SFRs

2.3.1 STATUS REGISTER

The STATUS register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- the Reset status
- the bank select bits for data memory (RAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS,` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `'000u u1uu'` (where u = unchanged).

It is recommended, therefore, that only `BCF, BSF, SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see **Section 18.0 "Instruction Set Summary"**.

REGISTER 2-1: STATUS: STATUS REGISTER

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)
1 = Bank 2, 3 (100h-1FFh)
0 = Bank 0, 1 (00h-FFh)

bit 6 **RP1:** Register Bank Select bit (used for direct addressing)
00 = Bank 0 (00h-7Fh)
01 = Bank 1 (80h-FFh)
10 = Bank 2 (100h-17Fh)
11 = Bank 3 (180h-1FFh)

bit 5 **RP0:** Register Bank Select bit (used for direct addressing)
1 = Bank 1 (80h-FFh)
0 = Bank 0 (00h-7Fh)

bit 4 **$\overline{TO}$:** Time-Out bit
1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-Down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{\text{Borrow}}$ bit(2) (`ADDWF, ADDLW, SUBLW, SUBWF` instructions), For $\overline{\text{Borrow}}$, the polarity is reversed.
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{\text{Borrow}}$ bit(2) (`ADDWF, ADDLW, SUBLW, SUBWF` instructions)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: The C and DC bits operate as a $\overline{\text{Borrow}}$ and $\overline{\text{Digit Borrow}}$ out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

2: For $\overline{\text{Borrow}}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF, RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

FIGURE 3-1: FLASH PROGRAM MEMORY READ CYCLE EXECUTION

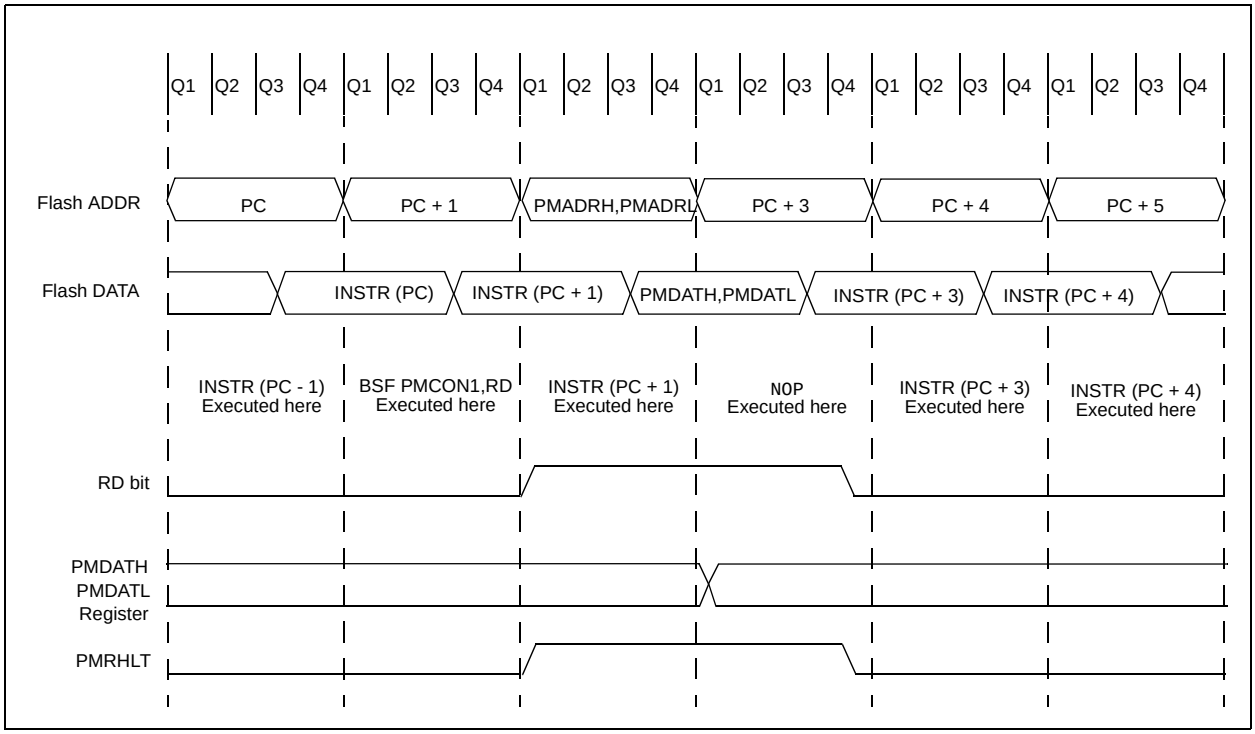


TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	ADFM	—	CHS<3:0>				GO/$\overline{\text{DONE}}$	ADON	109
ADCON1	—	ADCS<2:0>			—	—	—	ADPREF1	110
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	44
APFCON	—	—	—	T1GSEL	—	—	—	—	40
CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1ZLF	C1SP	C1HYS	C1SYNC	129
CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2ZLF	C2SP	C2HYS	C2SYNC	129
CM1CON1	C1INTP	C1INTN	C1PCH<2:0>			C1NCH<2:0>			130
CM2CON1	C2INTP	C2INTN	C2PCH<2:0>			C2NCH<2:0>			130
DAC1CON0	DACEN	DACFM	DACOE	—	DACPSS1	DACPSS0	—	—	120
IOCAF	—	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	45
IOCAN	—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	45
IOCAP	—	—	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	45
LATA	—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0	43
OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS<2:0>			16
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	43
TRISA	—	—	TRISA5	TRISA4	TRISA3(1)	TRISA2	TRISA1	TRISA0	43

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTA.
Note 1: TRISA3 always reads '1'.

FIGURE 7-5: TIMER1 GATE SINGLE-PULSE MODE

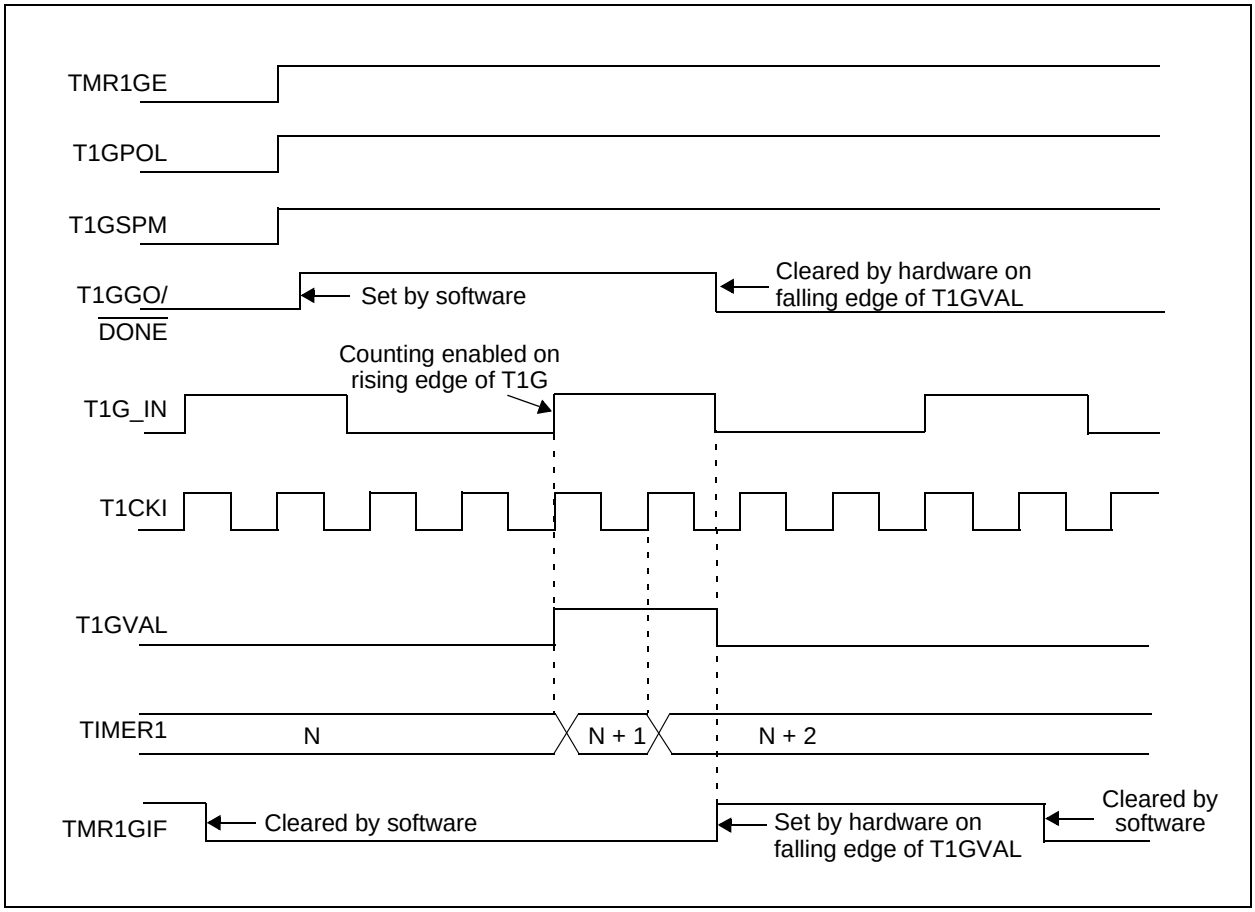
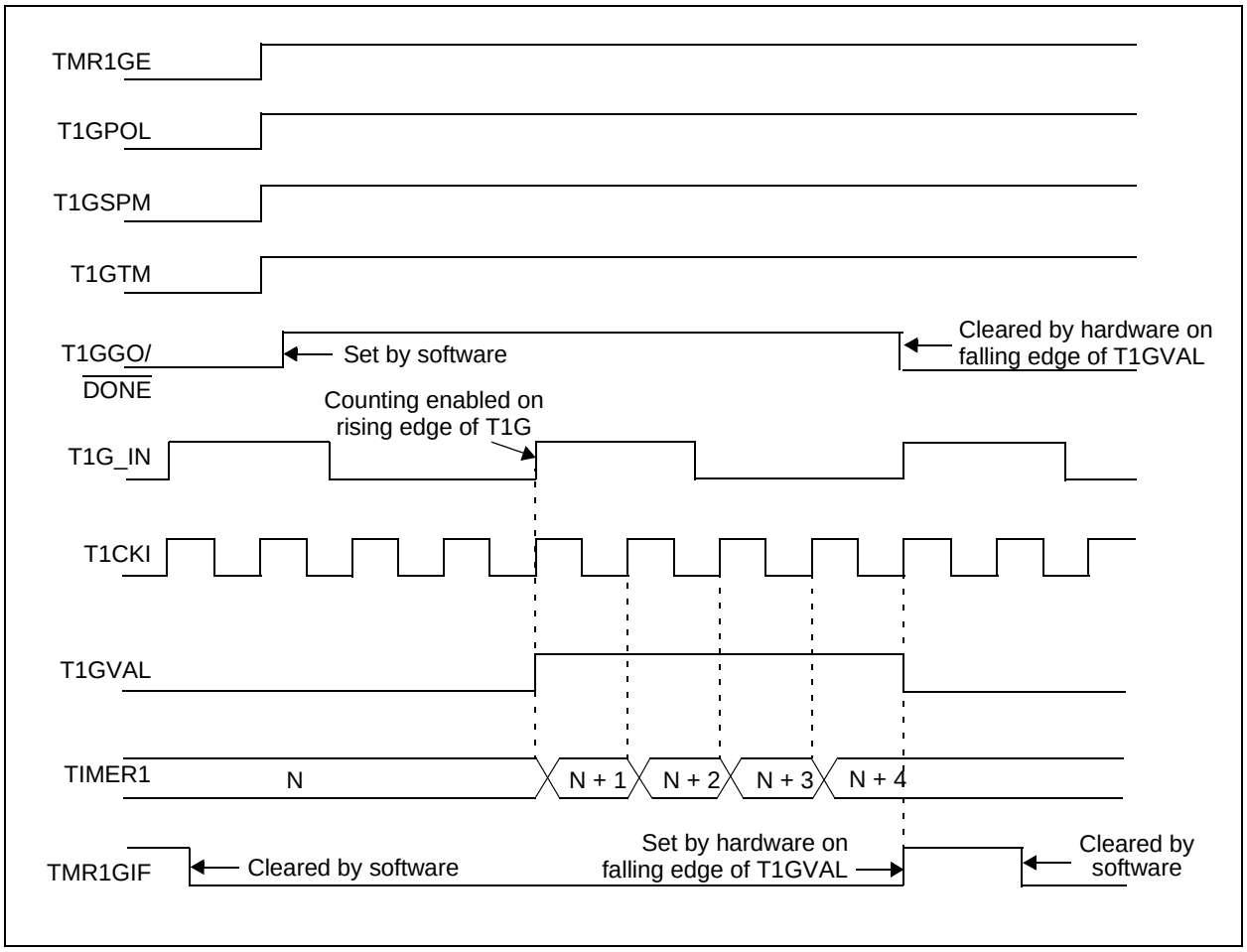


FIGURE 7-6: TIMER1 GATE SINGLE-PULSE AND TOGGLE COMBINED MODE



REGISTER 7-2: T1GCON: TIMER1 GATE CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-x	R/W-0	R/W-0
TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{DONE}}$	T1GVAL	T1GSS<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TMR1GE:** Timer1 Gate Enable bit

If TMR1ON = 0:
This bit is ignored
If TMR1ON = 1:
1 = Timer1 counting is controlled by the Timer1 gate function
0 = Timer1 counts regardless of Timer1 gate function

bit 6 **T1GPOL:** Timer1 Gate Polarity bit

1 = Timer1 gate is active-high (Timer1 counts when gate is high)
0 = Timer1 gate is active-low (Timer1 counts when gate is low)

bit 5 **T1GTM:** Timer1 Gate Toggle mode bit

1 = Timer1 Gate Toggle mode is enabled.
0 = Timer1 Gate Toggle mode is disabled and toggle flip-flop is cleared
Timer1 gate flip-flop toggles on every rising edge.

bit 4 **T1GSPM:** Timer1 Gate Single-Pulse mode bit

1 = Timer1 Gate Single-Pulse mode is enabled and is controlling Timer1 gate
0 = Timer1 Gate Single-Pulse mode is disabled

bit 3 **T1GGO/$\overline{\text{DONE}}$:** Timer1 Gate Single-Pulse Acquisition Status bit

1 = Timer1 gate single-pulse acquisition is ready, waiting for an edge
0 = Timer1 gate single-pulse acquisition has completed or has not been started
This bit is automatically cleared when T1GSPM is cleared.

bit 2 **T1GVAL:** Timer1 Gate Current State bit

Indicates the current state of the Timer1 gate that could be provided to TMR1H:TMR1L.
Unaffected by Timer1 Gate Enable (TMR1GE).

bit 1-0 **T1GSS<1:0>:** Timer1 Gate Source Select bits

11 = SYNCC2OUT
10 = SYNCC1OUT
01 = Timer0 overflow output
00 = Timer1 gate pin

9.0 HARDWARE LIMIT TIMER (HLT) MODULE

The Hardware Limit Timer (HLT) module is a version of the Timer2-type modules. In addition to all the Timer2-type features, the HLT can be reset on rising and falling events from selected peripheral outputs.

The HLT primary purpose is to act as a timed hardware limit to be used in conjunction with asynchronous analog feedback applications. The external Reset source synchronizes the HLTMRx to an analog application.

In normal operation, the external Reset source from the analog application should occur before the HLTMRx matches the HLTPRx. This resets HLTMRx for the next period and prevents the HLTimerx Output from going active.

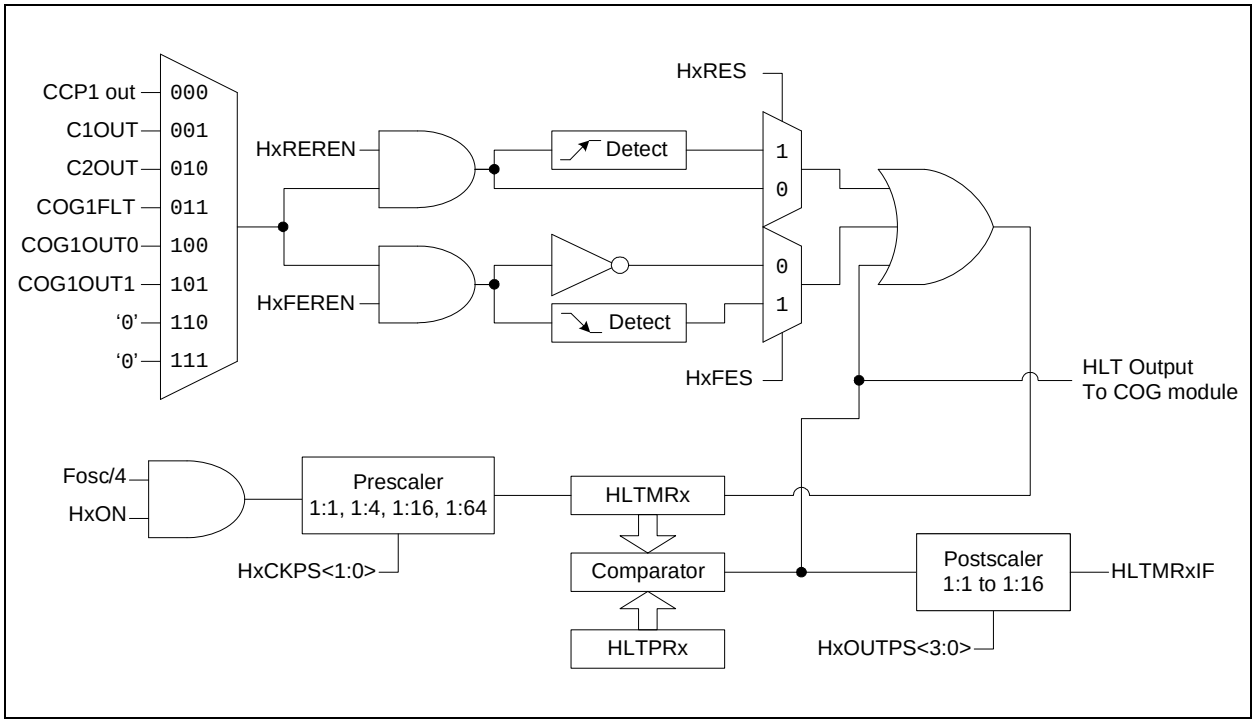
When the external Reset source fails to generate a signal within the expected time, (allowing the HLTMRx to match the HLTPRx), then the HLTimerx Output becomes active.

The HLT module incorporates the following features:

- 8-bit Read-Write Timer Register (HLTMRx)
- 8-bit Read-Write Period register (HLTPRx)
- Software programmable prescaler:
  - 1:1
  - 1:4
  - 1:16
  - 1:64
- Software programmable postscaler
  - 1:1 to 1:16, inclusive
- Interrupt on HLTMRx match with HLTPRx
- Eight selectable timer Reset inputs (two reserved)
- Reset on rising and falling event

Refer to Figure 9-1 for a block diagram of the HLT.

FIGURE 9-1: HLTMRx BLOCK DIAGRAM



10.2 Compare Mode

Compare mode makes use of the 16-bit Timer1 resource. The 16-bit value of the CCPR1H:CCPR1L register pair is constantly compared against the 16-bit value of the TMR1H:TMR1L register pair. When a match occurs, one of the following events can occur:

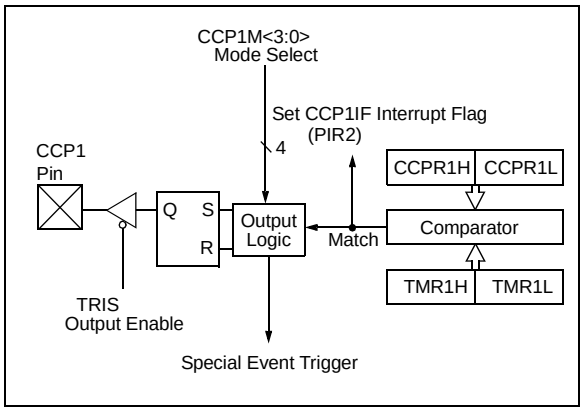
- Toggle the CCP1 output
- Set the CCP1 output
- Clear the CCP1 output
- Generate a Special Event Trigger
- Generate a Software Interrupt

The action on the pin is based on the value of the CCP1M<3:0> control bits of the CCP1CON register. At the same time, the interrupt flag CCP1IF bit is set.

All Compare modes can generate an interrupt.

Figure 10-2 shows a simplified diagram of the Compare operation.

FIGURE 10-2: COMPARE MODE OPERATION BLOCK DIAGRAM



10.2.1 CCP1 PIN CONFIGURATION

The user must configure the CCP1 pin as an output by clearing the associated TRIS bit.

Note:	Clearing the CCP1CON register will force the CCP1 compare output latch to the default low level. This is not the PORT I/O data latch.

10.2.2 TIMER1 MODE RESOURCE

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

See **Section 7.0 "Timer1 Module with Gate Control"** for more information on configuring Timer1.

Note:	Clocking Timer1 from the system clock (FOSC) should not be used in Compare mode. In order for Compare mode to recognize the trigger event on the CCP1 pin, TImer1 must be clocked from the instruction clock (FOSC/4) or from an external clock source.

10.2.3 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt mode is chosen (CCP1M<3:0> = 1010), the CCP1 module does not assert control of the CCP1 pin (see the CCP1CON register).

10.2.4 SPECIAL EVENT TRIGGER

When Special Event Trigger mode is chosen (CCP1M<3:0> = 1011), the CCP1 module does the following:

- Resets Timer1
- Starts an ADC conversion if ADC is enabled

The CCP1 module does not assert control of the CCP1 pin in this mode.

The Special Event Trigger output of the CCP1 occurs immediately upon a match between the TMR1H, TMR1L register pair and the CCPR1H, CCPR1L register pair. The TMR1H, TMR1L register pair is not reset until the next rising edge of the Timer1 clock. The Special Event Trigger output starts an A/D conversion (if the A/D module is enabled). This allows the CCPR1H, CCPR1L register pair to effectively provide a 16-bit programmable period register for Timer1.

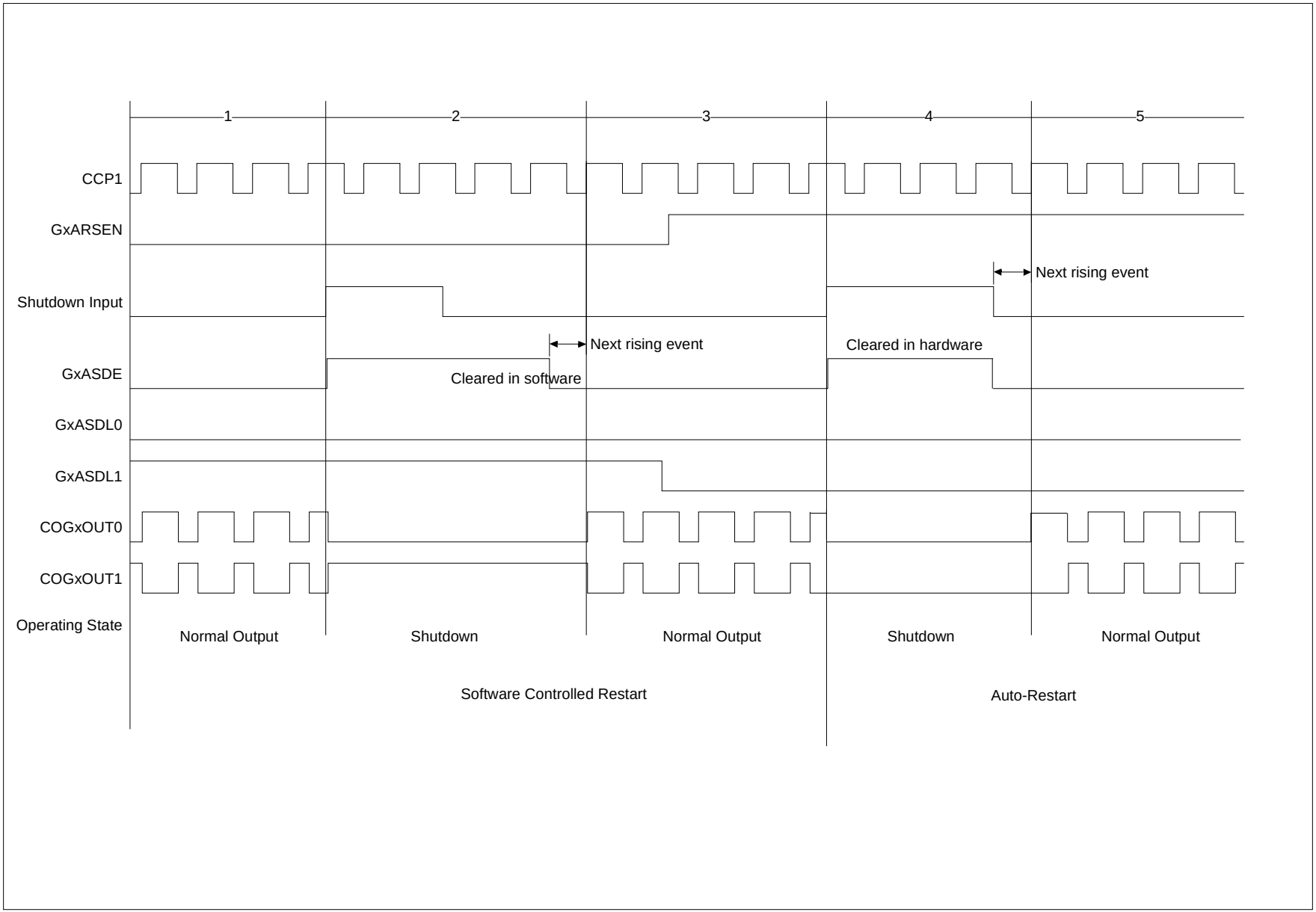
TABLE 10-2: SPECIAL EVENT TRIGGER

Device	CCP1
PIC16F753 PIC16HV753	CCP1

Refer to **Section 12.0 "Analog-to-Digital Converter (ADC) Module"** for more information.

Note 1:	The Special Event Trigger from the CCP module does not set interrupt flag bit TMR1IF of the PIR1 register.
2:	Removing the match condition by changing the contents of the CCPR1H and CCPR1L register pair, between the clock edge that generates the Special Event Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring.

FIGURE 11-8: AUTO-SHUTDOWN WAVEFORM – CCP1 AS RISING AND FALLING EVENT INPUT SOURCE



REGISTER 11-13: COGxPHR: COG RISING EDGE PHASE DELAY COUNT REGISTER

U-0	U-0	U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	—	GxPHR<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **GxPHR<3:0>:** Rising Edge Phase Delay Count Value bits
= Number of COGx clock periods to delay rising edge event

REGISTER 11-14: COGxPHF: COG FALLING EDGE PHASE DELAY COUNT REGISTER

U-0	U-0	U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	—	GxPHF<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **GxPHF<3:0>:** Falling Edge Phase Delay Count Value bits
= Number of COGx clock periods to delay falling edge event

15.0 COMPARATOR MODULE

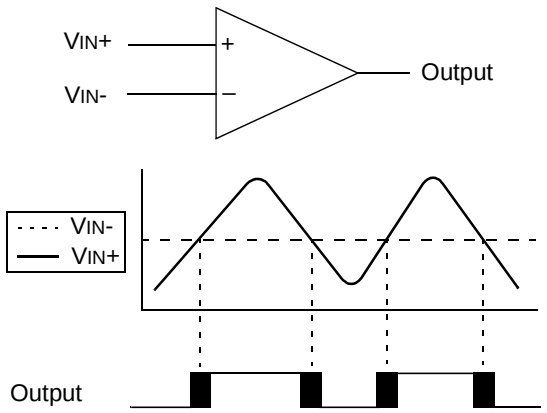
Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed-signal building blocks because they provide analog functionality independent of program execution. The analog comparator module includes the following features:

- Independent comparator control
- Programmable input selection
- Comparator output is available internally/externally
- Programmable output polarity
- Interrupt-on-change
- Wake-up from Sleep
- Programmable Speed/Power optimization
- PWM shutdown
- Programmable and Fixed Voltage Reference

15.1 Comparator Overview

A single comparator is shown in Figure 15-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

FIGURE 15-1: SINGLE COMPARATOR



Note: The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.

16.0 OPERATIONAL AMPLIFIER (OPA) MODULE

The Operational Amplifier (OPA) is a standard three-terminal device requiring external feedback to operate. The OPA module has the following features:

- External Connections to I/O Ports
- Selectable Unity Gain Bandwidth Product Option
- Low-Leakage Inputs
- Factory-Calibrated Input Offset Voltage

16.1 OPAxCON0 Register

The OPAxCON0 register, shown in Register 16-1, controls the OPA module.

The OPA module is enabled by setting the OPAxEN bit of the OPAxCON register. When enabled, the OPA forces the output driver of the OPAxOUT pin into tri-state to prevent contention between the driver and the OPA output.

The OPAxUGM bit of the OPAxCON register enables the Unity Gain Bandwidth mode (voltage follower) of the amplifier. In Unity Gain mode, the OPAxNCH<1:0> inputs are disabled. The default mode is normal three-terminal operation.

Note:	When the OPA module is enabled, the OPAxOUT pin is driven by the op amp output, not by the PORT digital driver. Refer to **Section 22.0 "Electrical Specifications"** for the op amp output drive capability.

16.2 Effects of a Reset

A device Reset forces all registers to their Reset state. This disables the OPA module.

16.3 OPA Module Performance

Common AC and DC performance specifications for the OPA module:

- Common Mode Voltage Range
- Leakage Current
- Input Offset Voltage
- Open Loop Gain
- Gain Bandwidth Product

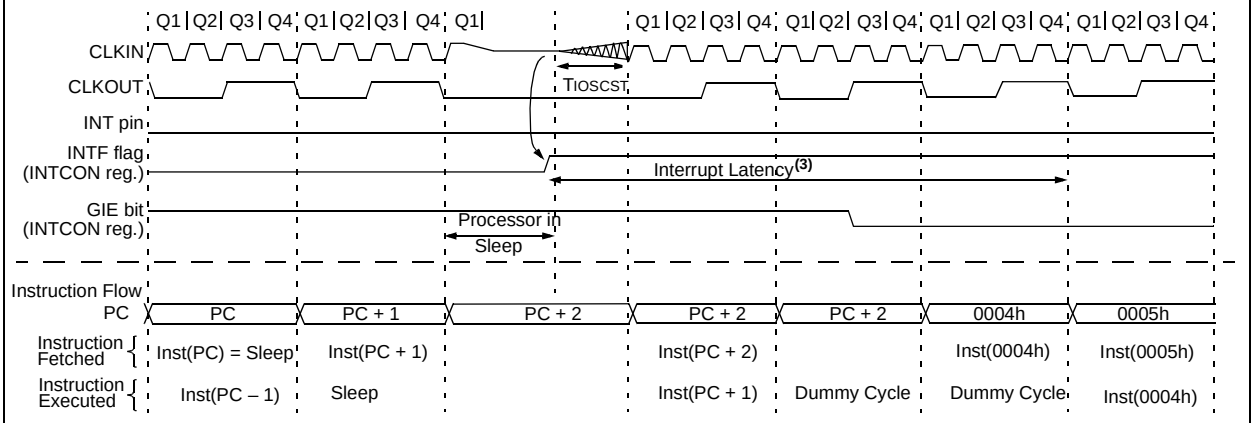
Common mode voltage range is the specified voltage range for the OPAx+ and OPAx- inputs, for which the OPA module will perform within its specifications. The OPA module is designed to operate with input voltages between V_{SS} and V_{DD}. Behavior for Common mode voltages greater than V_{DD} or below V_{SS} is not guaranteed.

Leakage current is a measure of the small source or sink currents on the OPAx+ and OPAx- inputs. To minimize the effect of leakage currents, the effective impedances connected to the OPAx+ and OPAx- inputs should be kept as small as possible and equal. Input offset voltage is a measure of the voltage difference between the OPAx+ and OPAx- inputs in a closed loop circuit with the OPA in its linear region. The offset voltage will appear as a DC offset in the output equal to the input offset voltage, multiplied by the gain of the circuit.

The input offset voltage is also affected by the Common mode voltage. The OPA is factory-calibrated to minimize the input offset voltage of the module. Open loop gain is the ratio of the output voltage to the differential input voltage (OPAx+) - (OPAx-). The gain is greatest at DC and falls off with frequency.

Gain Bandwidth Product or GBWP is the frequency at which the open loop gain falls off to 0 dB. The lower GBWP is optimized for systems requiring low-frequency response and low-power consumption.

FIGURE 19-10: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: HFINTOSC Oscillator mode assumed.

2: GIE = '1' assumed. In this case after wake-up, the processor jumps to 0004h. If GIE = '0', execution will continue in-line.

19.8 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP™ for verification purposes.

Note:	The entire Flash program memory will be erased when the code protection is turned off. See the *PIC16F753/HV753 Flash Memory Programming Specification* (DS41686) for more information.

19.9 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable during Program/Verify mode. Only the Least Significant seven bits of the ID locations are reported when using MPLAB® IDE.

22.2 DC Characteristics

TABLE 22-1: SUPPLY VOLTAGE

PIC16F753			Standard Operating Conditions (unless otherwise stated)				
PIC16HV753							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**					
			VDDMIN		VDDMAX		
			2.0	—	5.5	V	FOSC ≤ 8 MHz
			3.0	—	5.5	V	FOSC ≤ 10 MHz
			4.5	—	5.5	V	FOSC≤ 20 MHz
D001			2.0	—	5.0	V	FOSC ≤ 8 MHz(2)
			3.0	—	5.0	V	FOSC ≤ 10 MHz(2)
			4.5	—	5.0	V	FOSC ≤ 20 MHz(2)
D002*	VDR	**RAM Data Retention Voltage(1)**					
			1.5	—	—	V	Device in Sleep mode
D002			1.5	—	—	V	Device in Sleep mode
D003*	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal					
			—	1.6	—	V	
D003			—	1.6	—	V	
D004*	SVDD	**VDD Rise Rate** to ensure VDD Rise Rate internal Power-on Reset signal					
			0.05	—	—	V/ms	See Table for details.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: On the PIC16HV753, VDD is regulated by a Shunt Regulator and is dependent on series resistor (connected between the unregulated supply voltage and the VDD pin) to limit the current to 50 mA. See **Section 20.0 "Shunt Regulator (PIC16HV753 Only)"** for design requirements.

TABLE 22-6: THERMAL CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)					
Param No.	**Sym.**	**Characteristic**	**Typ.**	**Units**	**Conditions**
TH01	θ_{JA}	Thermal Resistance Junction to Ambient	84.6	°C/W	8-pin PDIP package
			149.5	°C/W	8-pin SOIC package
			60	°C/W	8-pin DFN 3x3mm package
TH02	θ_{JC}	Thermal Resistance Junction to Case	41.2	°C/W	8-pin PDIP package
			39.9	°C/W	8-pin SOIC package
			9	°C/W	8-pin DFN 3x3mm package
TH03	T_{JMAX}	Maximum Junction Temperature	150	°C	
TH04	PD	Power Dissipation	—	W	$PD = P_{INTERNAL} + P_{I/O}$
TH05	$P_{INTERNAL}$	Internal Power Dissipation	—	W	$P_{INTERNAL} = I_{DD} \times V_{DD}$ (1)
TH06	$P_{I/O}$	I/O Power Dissipation	—	W	$P_{I/O} = \Sigma (I_{OL} * V_{OL}) + \Sigma (I_{OH} * (V_{DD} - V_{OH}))$
TH07	P_{DER}	Derated Power	—	W	$P_{DER} = PD_{MAX} (T_J - T_A)/\theta_{JA}$ (2)

Note 1: I_{DD} is current to run the chip alone without driving any load on the output pins.

2: T_A = Ambient temperature; T_J = Junction Temperature

FIGURE 23-18: IPD, FIXED VOLTAGE REFERENCE (FVR), PIC16HV753 ONLY

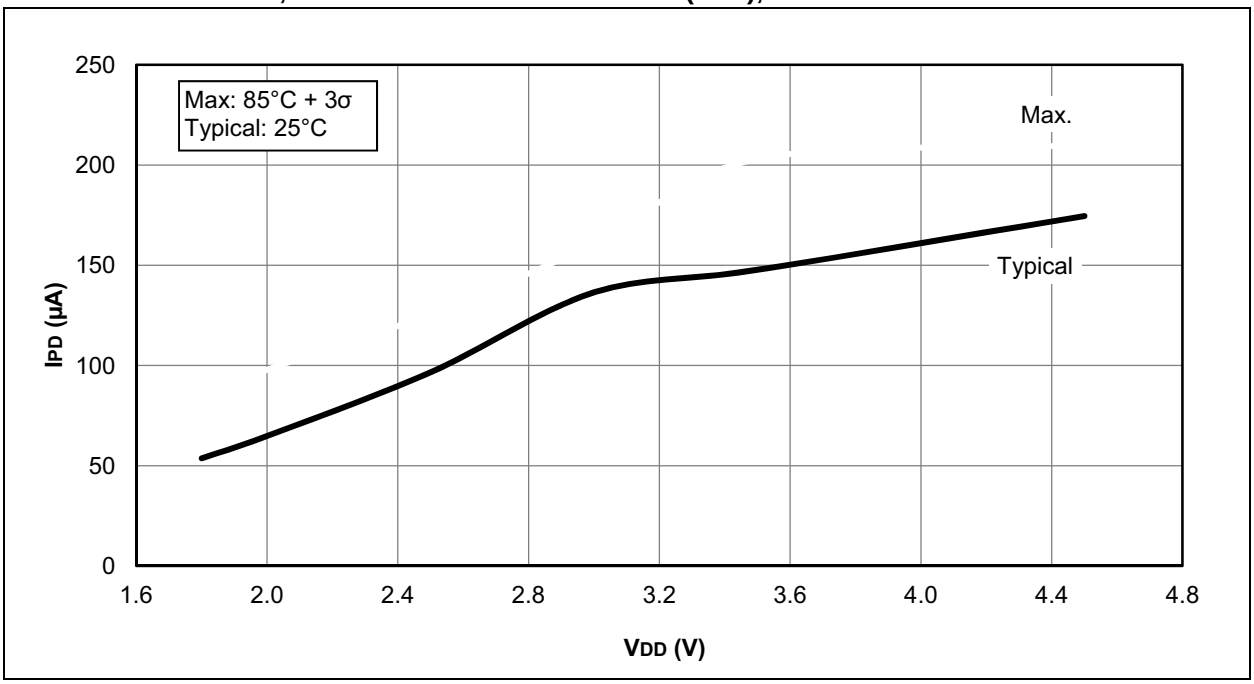


FIGURE 23-19: IPD, FIXED VOLTAGE REFERENCE (FVR), PIC16F753 ONLY

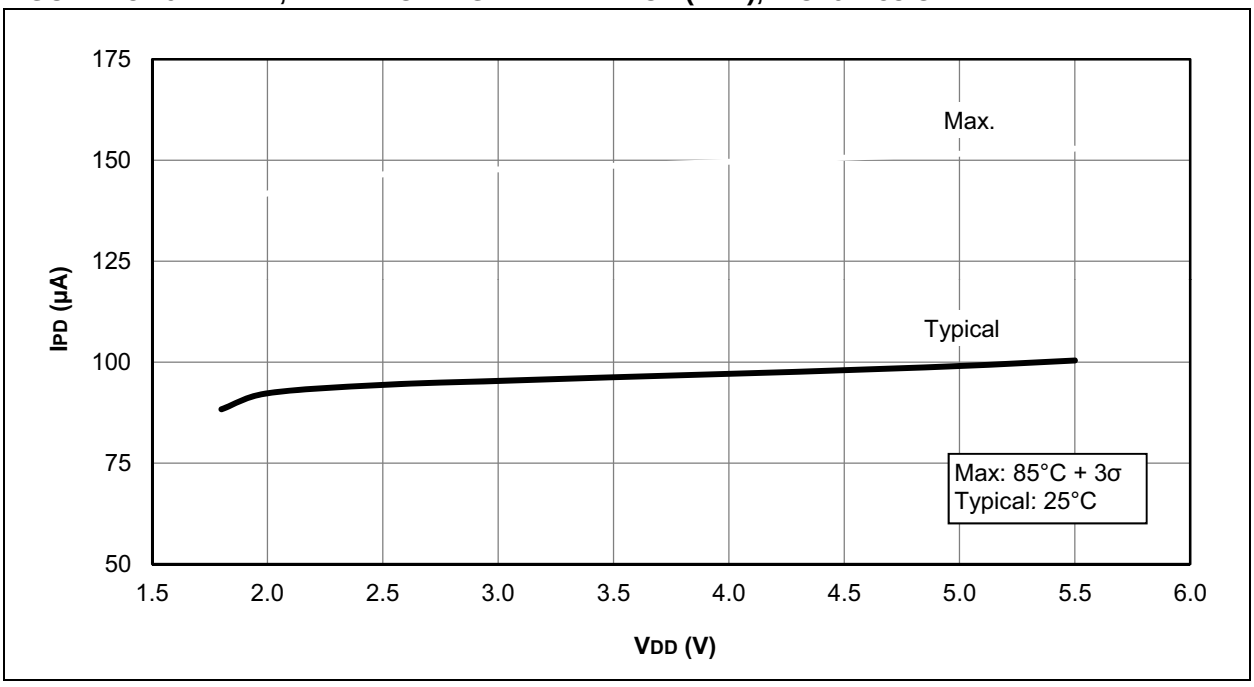


FIGURE 23-24: IPD, TIMER1 OSCILLATOR, FOSC = 32 kHz, PIC16HV753 ONLY

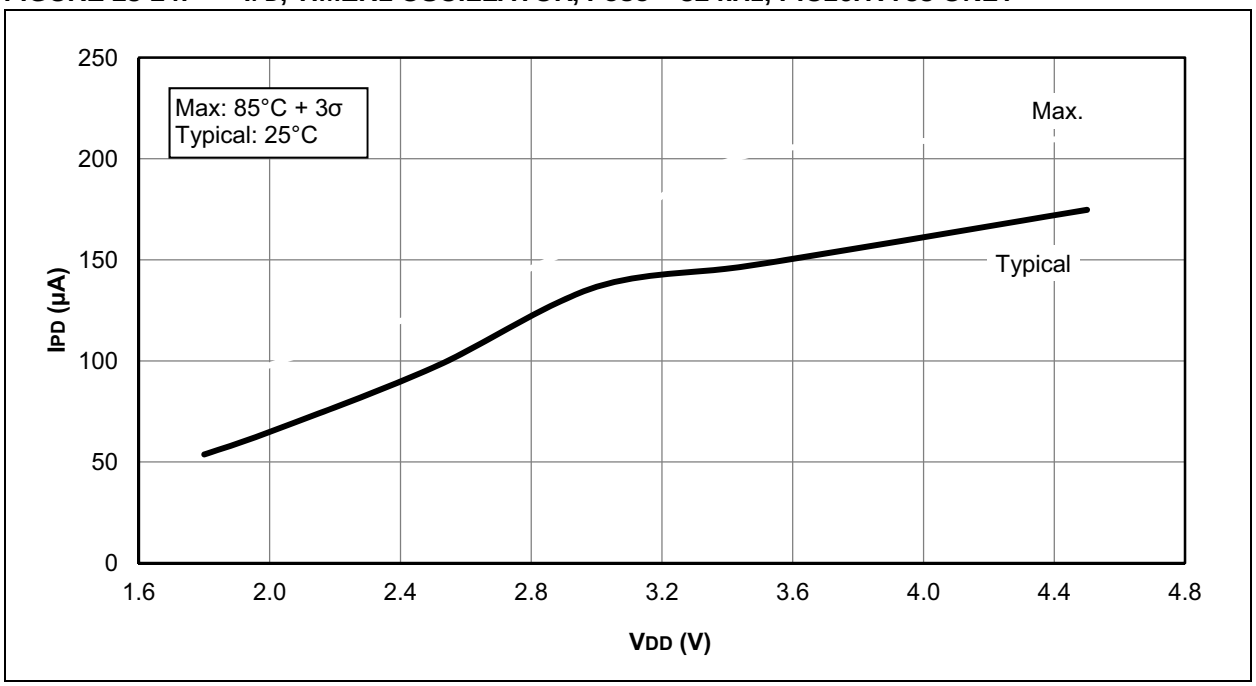


FIGURE 23-25: IPD, TIMER1 OSCILLATOR, FOSC = 32 kHz, PIC16F753 ONLY

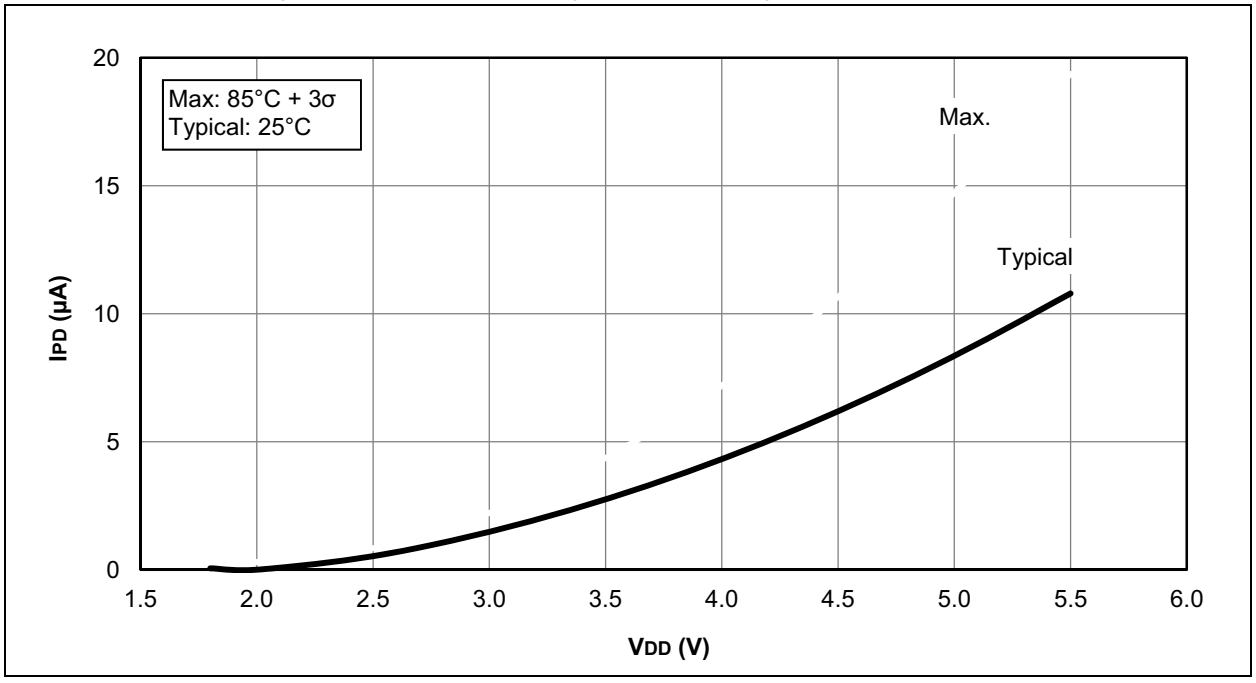


FIGURE 23-28: IPD, ADC NO CONVERSION IN PROGRESS, PIC16HV753 ONLY

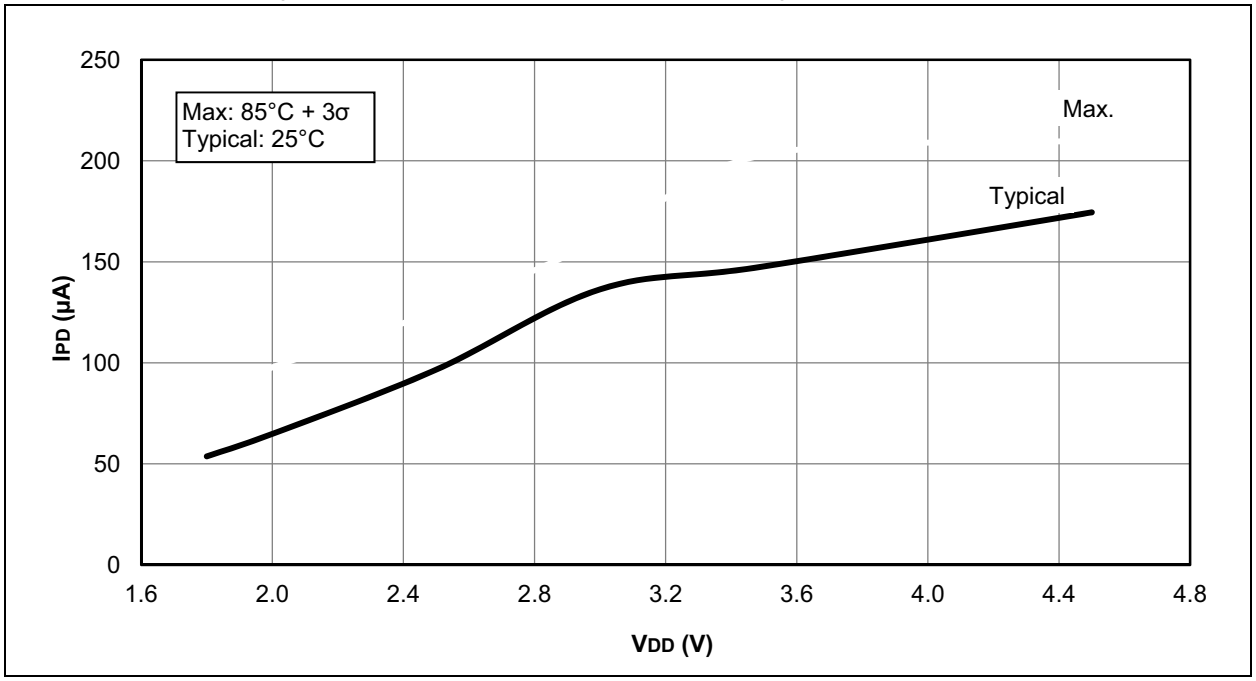
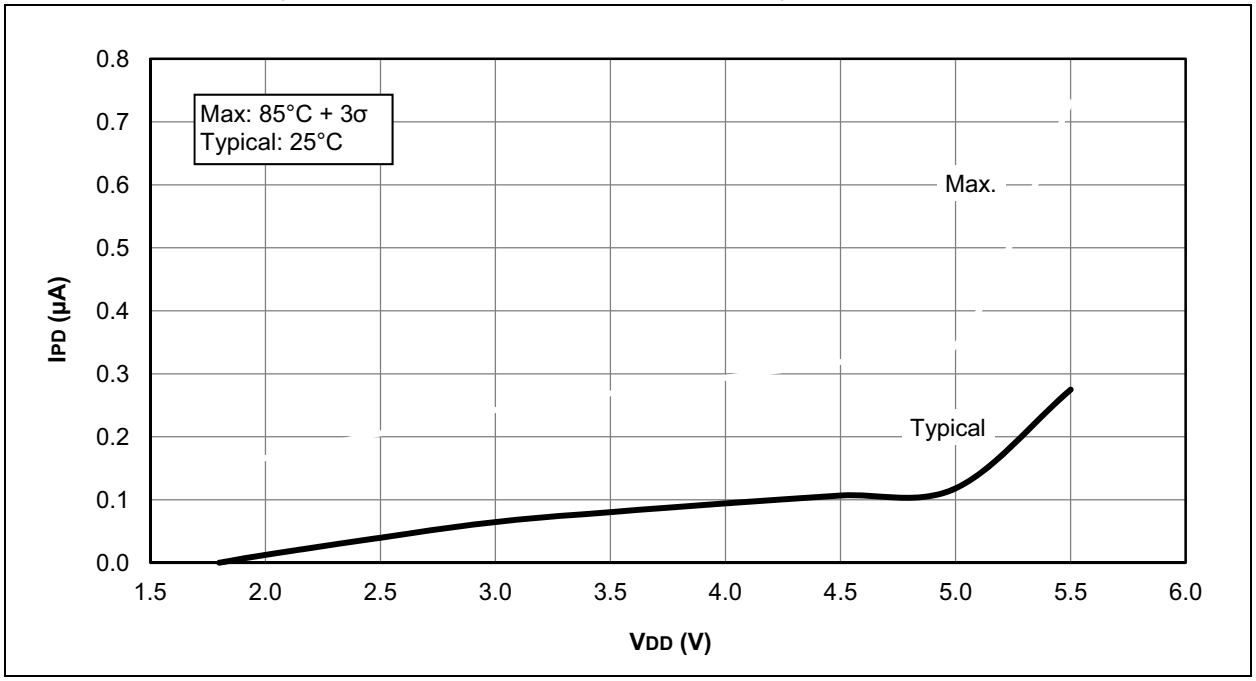
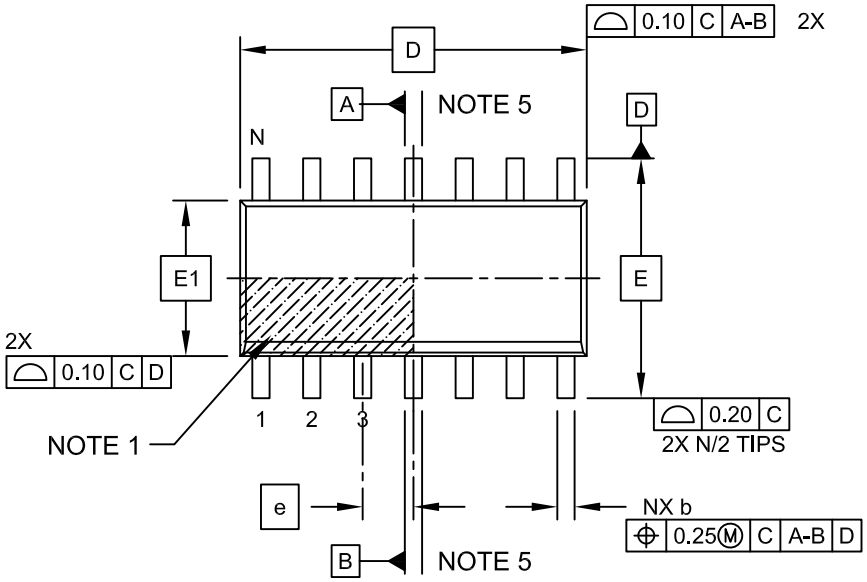


FIGURE 23-29: IPD, ADC NO CONVERSION IN PROGRESS, PIC16F753 ONLY

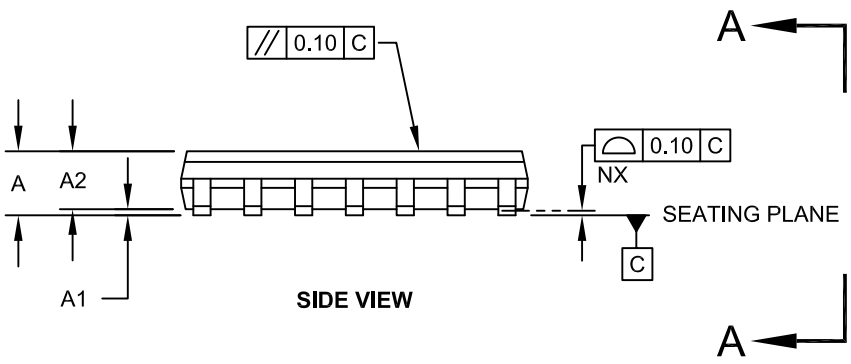


14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

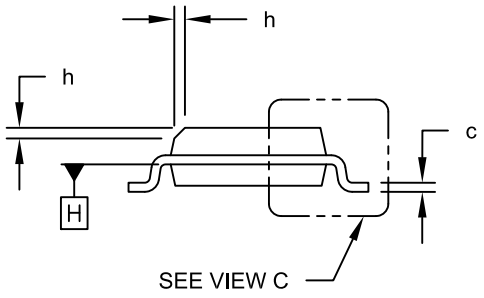
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A-A

Microchip Technology Drawing No. C04-065C Sheet 1 of 2

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