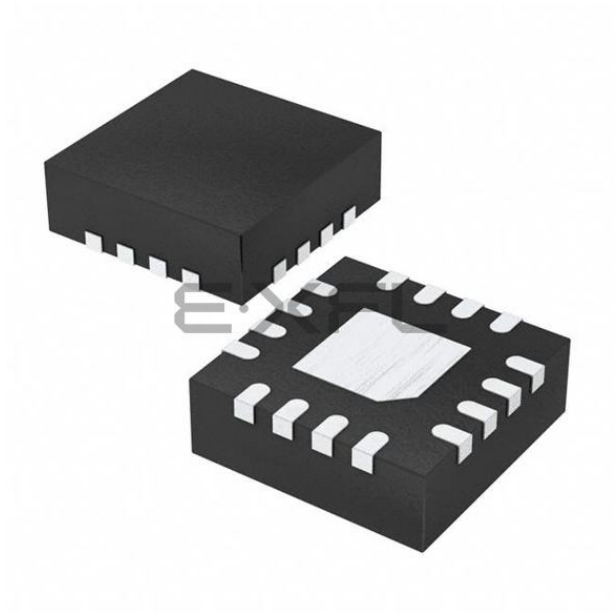


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b; D/A 1x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VQFN Exposed Pad
Supplier Device Package	16-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f753t-i-ml

- Complementary Output Generator (COG):
  - Complementary Waveforms from selectable sources
  - Two I/O (50 mA) for direct MOSFET drive
  - Rising and/or Falling edge dead-band control
  - Phase control, Blanking control
  - Auto-shutdown
  - Slope Compensation Circuit for use with SMPS power supplies

TABLE 1: PIC16F753/HV753 FAMILY TYPES

Device	Data Sheet Index	Program Memory Flash (words)	Self-Read/Write Flash Memory	Data SRAM (bytes)	I/Os(2)	10-bit ADC (ch)	Comparators	Timers (8/16-bit)	CCP	Complementary Output Generator (COG)	DAC	Op Amp	Shunt Regulator	Debug(1)	XLP
PIC12F752	(1)	1K	Y	64	6	4	2	3/1	1	Y	5-bit	N	N	H	Y
PIC12HV752	(1)	1K	Y	64	6	4	2	3/1	1	Y	5-bit	N	Y	H	Y
PIC16F753	(2)	2K	Y	128	12	8	2	3/1	1	Y	9-bit	Y	N	I/H	Y
PIC16HV753	(2)	2K	Y	128	12	8	2	3/1	1	Y	9-bit	Y	Y	I/H	Y

Note 1: I - Debugging, Integrated on Chip; H - Debugging, Requires Debug Header.

2: One pin is input-only.

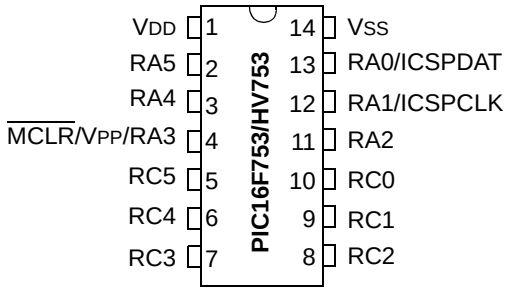
Data Sheet Index: (Unshaded devices are described in this document.)

1: DS40001576 PIC12F752/HV752 Data Sheet, 8-Pin Flash-Based, 8-Bit CMOS Microcontrollers.

2: DS40001709 PIC16F753/HV753 Data Sheet, 14/16-Pin Flash-based, 8-Bit CMOS Microcontrollers.

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

FIGURE 1: 14-PIN PDIP, SOIC, TSSOP DIAGRAM



Note: See Table 2 for location of all peripheral functions.

4.0 OSCILLATOR MODULE

4.1 Overview

The oscillator module has a variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 4-1 illustrates a block diagram of the oscillator module.

The oscillator module can be configured in one of two clock modes.

1. EC (external clock)
2. INTOSC (internal oscillator)

Clock Source modes are configured by the FOSC bit in the Configuration Word register (CONFIG).

The internal oscillator module provides the following selectable system clock modes:

- 8 MHz (HFINTOSC)
- 4 MHz (HFINTOSC Postscaler)
- 1 MHz (HFINTOSC Postscaler)
- 31 kHz (LFINTOSC)

FIGURE 4-1: PIC® MCU CLOCK SOURCE BLOCK DIAGRAM

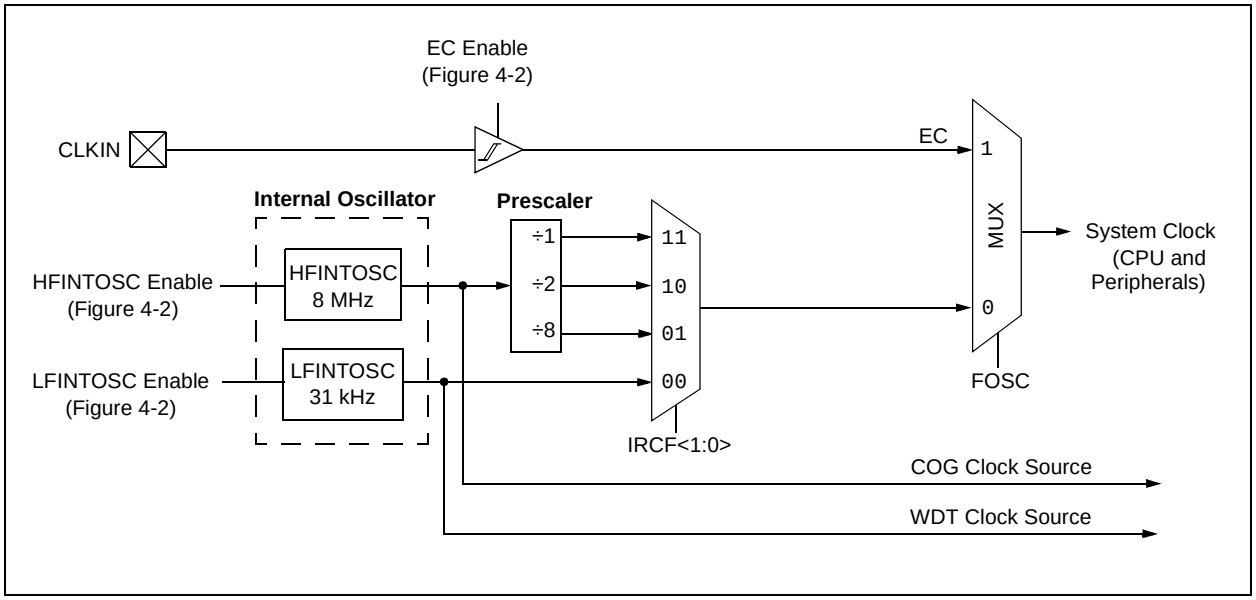
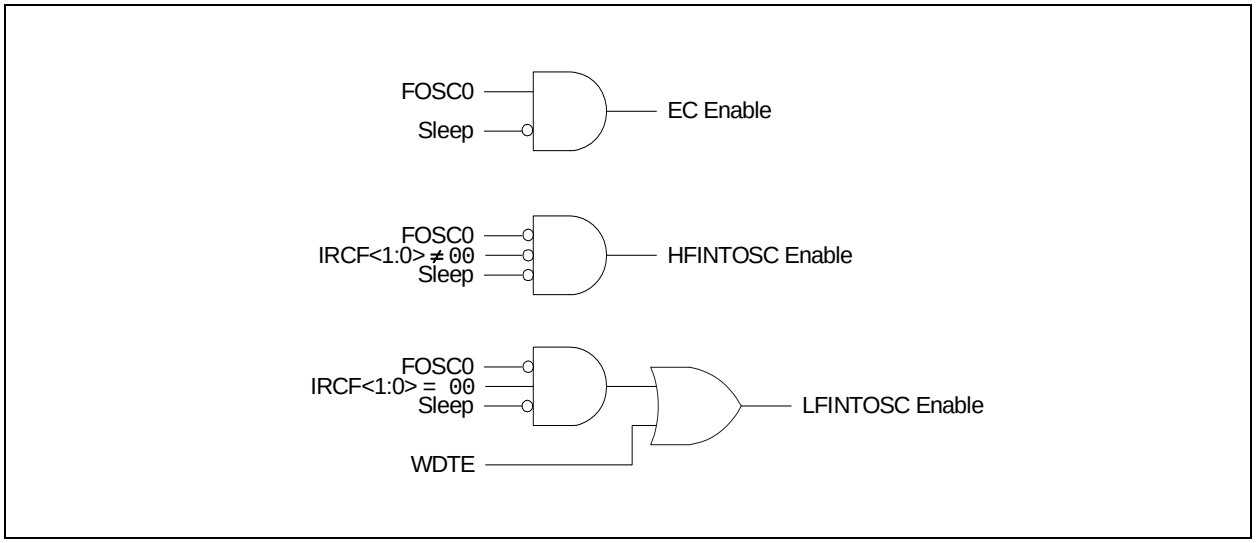


FIGURE 4-2: OSCILLATOR ENABLE



5.5 Register Definitions: PORTA Control

REGISTER 5-2: PORTA: PORTA REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R-x/x	R/W-x/u	R/W-x/u	R/W-x/u
—	—	RA5	RA4	RA3	RA2	RA1	RA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RA<5:0>**: PORTA I/O Value bits(1)
1 = Port pin is ≥ V_{IH}
0 = Port pin is ≤ V_{IL}

Note 1: Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.

REGISTER 5-3: TRISA: PORTA TRI-STATE REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	R-1/1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	TRISA5	TRISA4	TRISA3(1)	TRISA2	TRISA1	TRISA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **TRISA<5:0>:** PORTA Tri-State Control bits(1)
1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

Note 1: TRISA3 always reads '1'.

REGISTER 5-4: LATA: PORTA DATA LATCH REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	U-0	R/W-x/u	R/W-x/u	R/W-x/u
—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **LATA<5:4>**: PORTA Output Latch Value bits(1)

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **LATA<2:0>**: PORTA Output Latch Value bits(1)

Note 1: Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.

REGISTER 5-15: WPUC: WEAK PULL-UP PORTC REGISTER

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **WPUC<5:0>:** Weak Pull-up Control bits**(1,2,3)**
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: Global $\overline{\text{RAPU}}$ must be enabled for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is in Output mode (TRISC = 0).
3: The RC3 pull-up is enabled when configured as $\overline{\text{MCLR}}$ in the Configuration Word, otherwise it is disabled as an input and reads as ‘0’.

REGISTER 5-16: IOCCP: INTERRUPT-ON-CHANGE POSITIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IOCCP5	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-0 **IOCCP<5:0>:** Interrupt-on-Change Positive Edge Enable bits
1 = Interrupt-on-Change enabled on the pin for a positive going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 5-17: IOCCN: INTERRUPT-ON-CHANGE NEGATIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IOCCN5	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented**: Read as '0'

bit 5-0 **IOCCN<5:0>:** Interrupt-on-Change Negative Edge Enable bits

1 = Interrupt-on-Change enabled on the pin for a negative going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.

0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 5-18: IOCCF: INTERRUPT-ON-CHANGE FLAG REGISTER

U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
—	—	IOCCF5	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

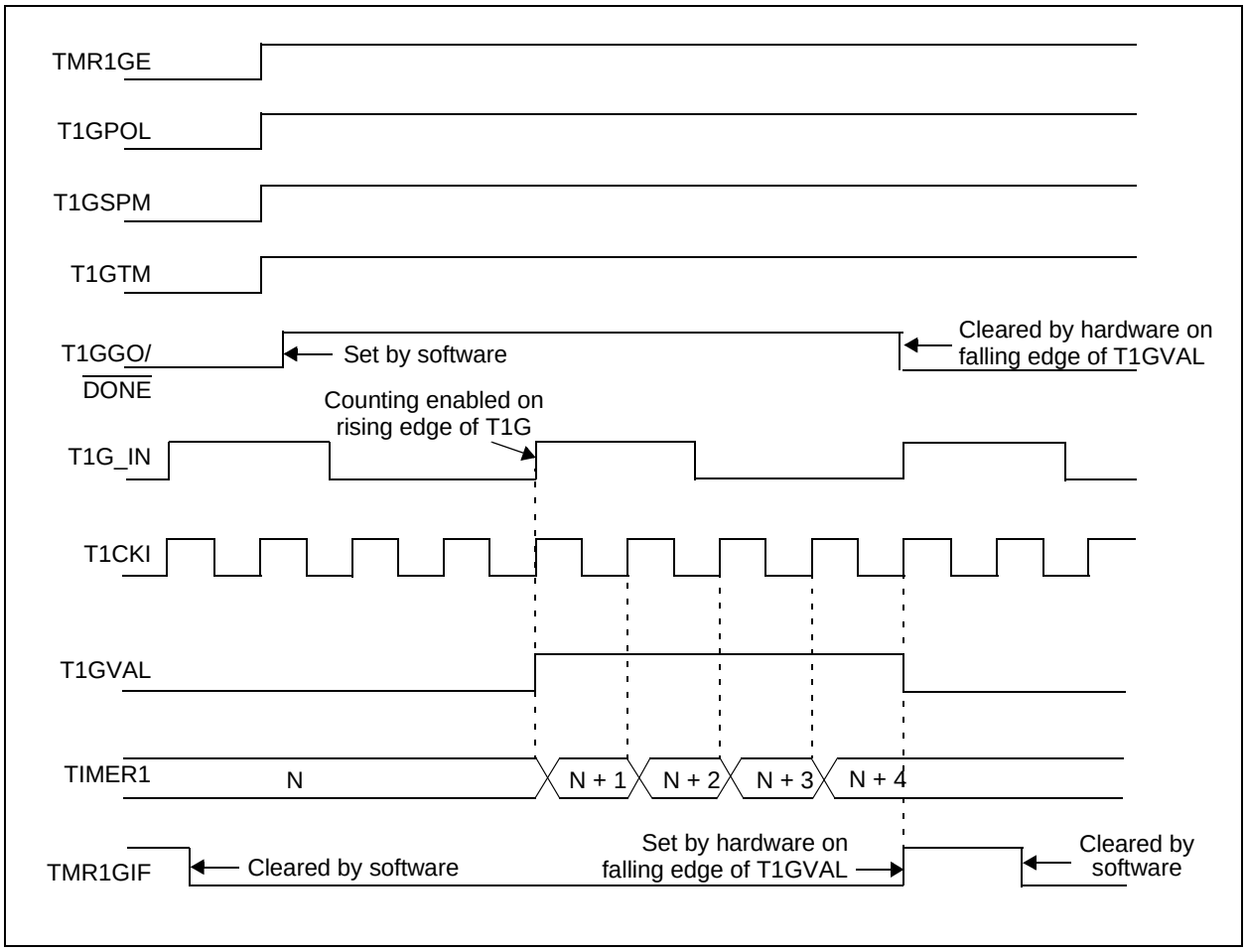
bit 7-6 **Unimplemented**: Read as '0'

bit 5-0 **IOCCF<5:0>:** Interrupt-on-Change Flag bits

1 = An enabled change was detected on the associated pin.
Set when IOCCPx = 1 and a rising edge was detected on RBx, or when IOCCNx = 1 and a falling edge was detected on RCx.

0 = No change was detected, or the user cleared the detected change.

FIGURE 7-6: TIMER1 GATE SINGLE-PULSE AND TOGGLE COMBINED MODE



10.0 CAPTURE/COMPARE/PWM MODULES

The Capture/Compare/PWM module is a peripheral which allows the user to time and control different events, and to generate Pulse-Width Modulation (PWM) signals. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate Pulse-Width Modulated signals of varying frequency and duty cycle.

10.1 Capture Mode

Capture mode makes use of the 16-bit Timer1 resource. When an event occurs on the CCP1 pin, the 16-bit CCPR1H:CCPR1L register pair captures and stores the 16-bit value of the TMR1H:TMR1L register pair, respectively. An event is defined as one of the following and is configured by the CCP1M<3:0> bits of the CCP1CON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

When a capture is made, the Interrupt Request Flag bit CCP1IF of the PIR2 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPR1H, CCPR1L register pair is read, the old captured value is overwritten by the new captured value.

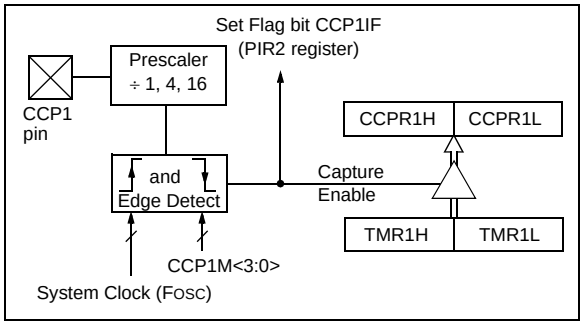
Figure 10-1 shows a simplified diagram of the Capture operation.

10.1.1 CCP1 PIN CONFIGURATION

In Capture mode, the CCP1 pin should be configured as an input by setting the associated TRIS control bit.

Note:	If the CCP1 pin is configured as an output, a write to the port can cause a capture condition.

FIGURE 10-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



10.1.2 TIMER1 MODE RESOURCE

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP1 module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

See **Section 7.0 "Timer1 Module with Gate Control"** for more information on configuring Timer1.

10.1.3 SOFTWARE INTERRUPT MODE

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCP1IE interrupt enable bit of the PIE2 register clear to avoid false interrupts. Additionally, the user should clear the CCP1IF interrupt flag bit of the PIR2 register following any change in Operating mode.

Note:	Clocking Timer1 from the system clock (FOSC) should not be used in Capture mode. In order for Capture mode to recognize the trigger event on the CCP1 pin, Timer1 must be clocked from the instruction clock (FOSC/4) or from an external clock source.

10.1.4 CCP1 PRESCALER

There are four prescaler settings specified by the CCP1M<3:0> bits of the CCP1CON register. Whenever the CCP1 module is turned off, or the CCP1 module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCP1CON register before changing the prescaler. Example 10-1 demonstrates the code to perform this function.

EXAMPLE 10-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
BANKSEL CCP1CON     ;Set Bank bits to point
                    ;to CCP1CON
CLRF    CCP1CON     ;Turn CCP1 module off
MOVLW   NEW_CAPT_PS;Load the W reg with
                    ;the new prescaler
                    ;move value and CCP1 ON
MOVWF   CCP1CON     ;Load CCP1CON with this
                    ;value
```

REGISTER 11-8: COGxASD1: COG AUTO-SHUTDOWN CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	GxASDSHLT2	GxASDSHLT1	GxASDSC2	GxASDSC1	GxASDSFLT
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **GxASDSHLT2:** COGx Auto-Shutdown Source Enable bit 4
1 = COGx is shutdown when HLTMR2 equals HLTPR2
0 = HLTimer 2 has no effect on shutdown

bit 3 **GxASDSHLT1:** COGx Auto-Shutdown Source Enable bit 3
1 = COGx is shutdown when HLTMR1 equals HLTPR1
0 = HLTimer 1 has no effect on shutdown

bit 2 **GxASDSC2:** COGx Auto-Shutdown Source Enable bit 2
1 = COGx is shutdown when Comparator 2 output is low
0 = Comparator 2 output has no effect on shutdown

bit 1 **GxASDSC1:** COGx Auto-Shutdown Source Enable bit 1
1 = COGx is shutdown when Comparator 1 output is low
0 = Comparator 1 output has no effect on shutdown

bit 0 **GxASDSFLT:** COGx Auto-Shutdown Source Enable bit 0
1 = COGx is shutdown when COGxFLT pin is low
0 = COGxFLT pin has no effect on shutdown

13.0 FIXED VOLTAGE REFERENCE (FVR)

The Fixed Voltage Reference (FVR) is a stable voltage reference, independent of VDD, with 1.2V output level. The output of the FVR can be configured to supply a reference voltage to the following:

- ADC input channel
- Comparator 1 positive input (C1VP)
- Comparator 2 positive input (C2VP)
- FVR_out pin
- Shunt regulator

On the PIC16F753, the FVR is enabled by setting the FVREN bit of the FVRCON register. The FVR is always enabled on the PIC16HV753 device.

13.1 Fixed Voltage Reference Output

The FVR output can be applied to the FVROUT pin by setting the FVRBUFSS and FVRBUFEN bits of the FVRCON register. The FVRBUFSS bit selects the op amp, FVR or DAC output reference to the FVROUT pin buffer. The FVRBUFEN bit enables the output buffer to the FVROUT pin.

Enabling the FVROUT pin automatically overrides any digital input or output functions of the pin. Reading the FVROUT pin when it has been configured for a reference voltage output will always return a '0'.

13.2 FVR Stabilization Period

When the Fixed Voltage Reference module is enabled, it requires time for the reference circuit to stabilize. Once the circuit stabilizes and is ready for use, the FVRRDY bit of the FVRCON register will be set. See **Section 22.0 "Electrical Specifications"** for the minimum delay requirement.

13.3 Operation During Sleep

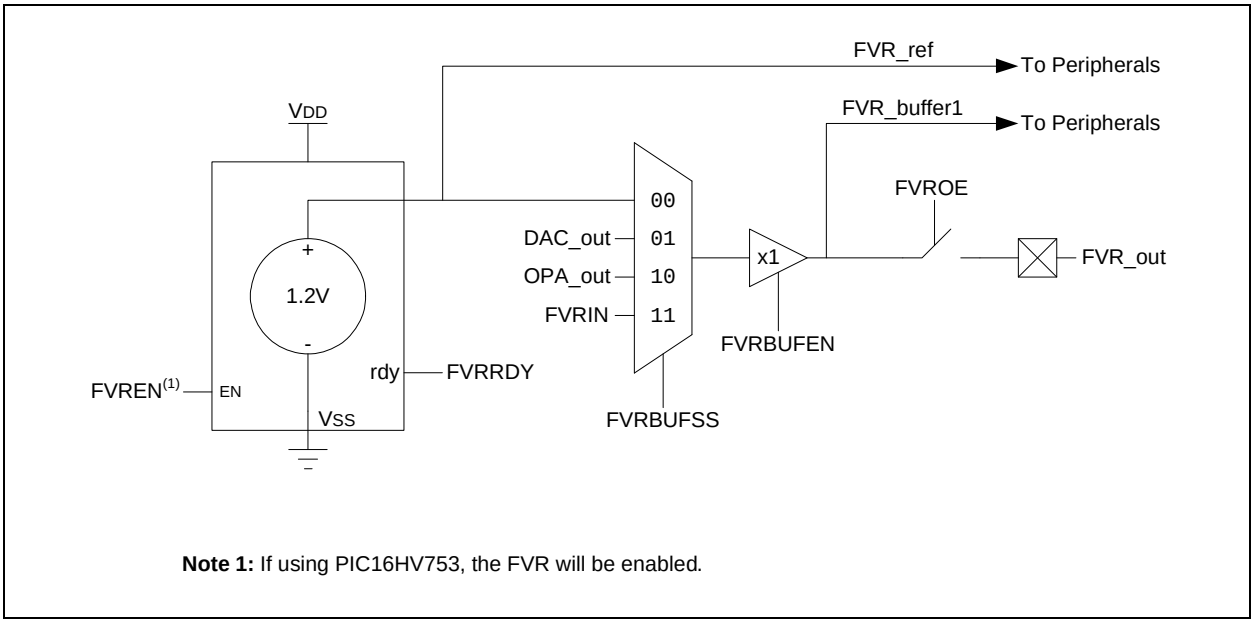
When the device wakes up from Sleep through an interrupt or a Watchdog Timer time-out, the contents of the FVRCON register are not affected. To minimize current consumption in Sleep mode, the FVR voltage reference should be disabled.

13.4 Effects of a Reset

A device Reset clears the FVRCON register. As a result:

- The FVR module is disabled
- The FVR voltage output is disabled on the FVROUT pin

FIGURE 13-1: VOLTAGE REFERENCE BLOCK DIAGRAM



Note 1: If using PIC16HV753, the FVR will be enabled.

FIGURE 14-1: DIGITAL-TO-ANALOG CONVERTER BLOCK DIAGRAM

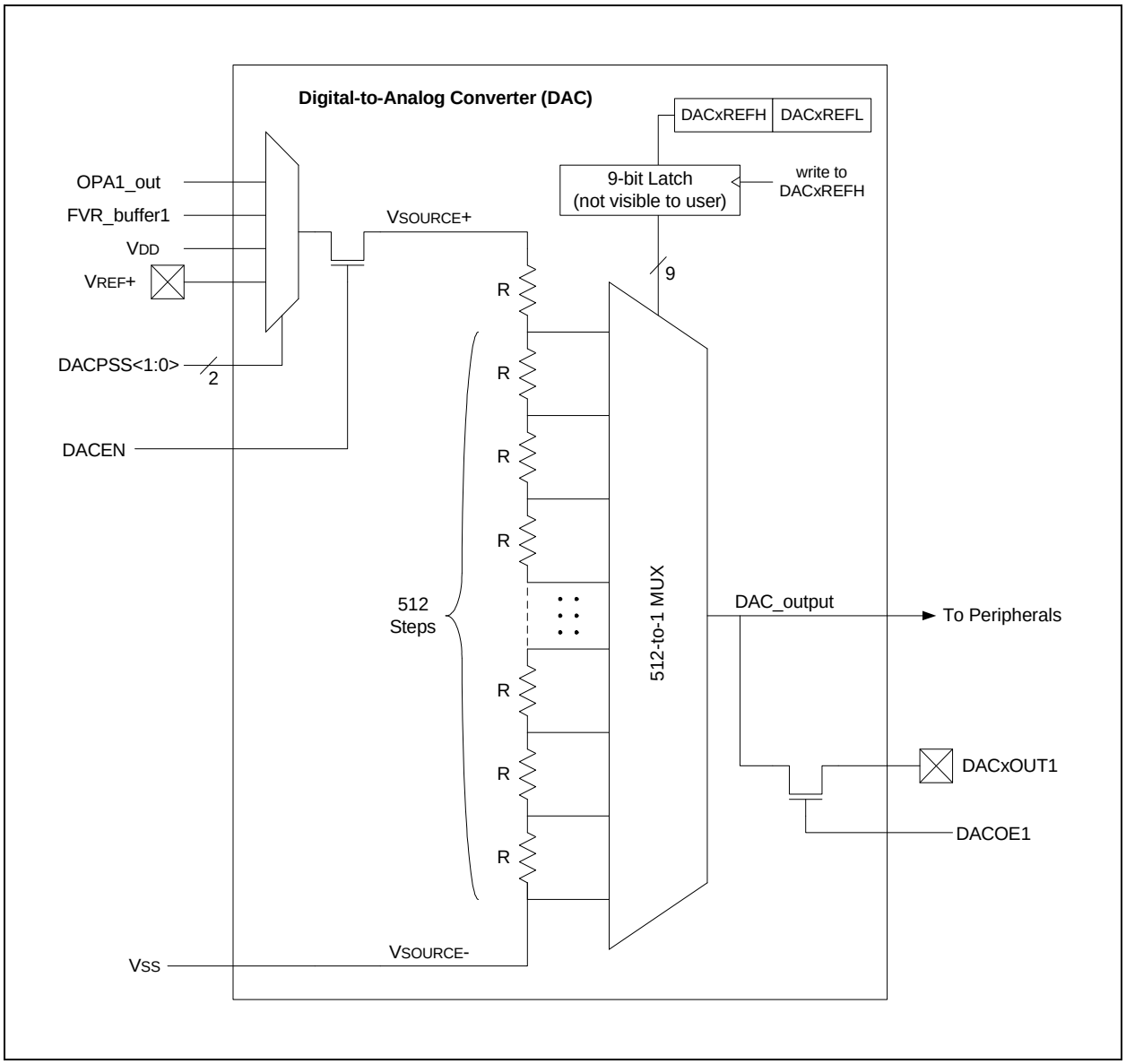


FIGURE 14-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE

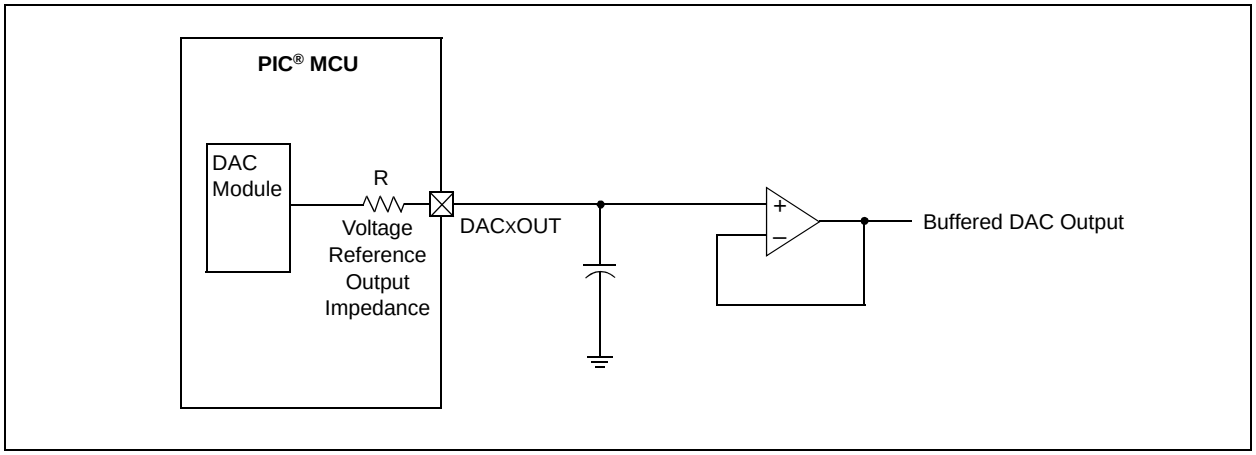


TABLE 15-2: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1ZLF	C1SP	C1HYS	C1SYNC	129
CM1CON1	C1INTP	C1INTN	C1PCH<2:0>			C1NCH<2:0>			130
CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2ZLF	C2SP	C2HYS	C2SYNC	129
CM2CON1	C2INTP	C2INTN	C2PCH<2:0>			C2NCH<2:0>			130
CMOUT	—	—	—	—	—	—	MCOUT2	MCOUT1	130
DAC1CON0	DACEN	DACFM	DACOE	—	DACPSS1	DACPSS0	—	—	120
DAC1REFL	Least Significant bit of the left shifted result or eight bits of the right shifted DAC setting								122
FVR1CON0	FVREN	FVRRDY	FVROE	FVRBUFSS1	FVRBUFSS0	—	—	FVRBUFEN	116
INTCON	GIE	PEIE	T0IE	INTE	IOCIE	T0IF	INTF	IOCIF	17
PIE2	—	—	C2IE	C1IE	—	COG1IE	—	CCP1IE	19
PIR2	—	—	C2IF	C1IF	—	COG1IF	—	CCP1IF	21
TRISA	—	—	TRISA5	TRISA4	TRISA3(1)	TRISA2	TRISA1	TRISA0	43
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	44

Legend: — = unimplemented location, read as '0'. Shaded cells are unused by the comparator module.
Note 1: TRISA3 always reads '1'.

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - (W) → (destination)

Status Affected: C, DC, Z

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

C = 0	W > f
C = 1	W ≤ f
DC = 0	W<3:0> > f<3:0>
DC = 1	W<3:0> ≤ f<3:0>

SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f<3:0>) → (destination<7:4>),
(f<7:4>) → (destination<3:0>)

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

XORLW **Exclusive OR literal with W**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Description: The contents of the W register are XOR'ed with the 8-bit literal 'k'. The result is placed in the W register.

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (destination)

Status Affected: Z

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

TABLE 19-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT RESET

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$	22
STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	15

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition. Shaded cells are not used by BOR.

19.3.5 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows:

- PWRT time-out is invoked after POR has expired.
- OST is activated after the PWRT time-out has expired.

The total time-out will vary based on oscillator configuration and $\overline{PWRTE}$ bit status. For example, in EC mode with $\overline{PWRTE}$ bit erased (PWRT disabled), there will be no time-out at all. Figure 19-4, Figure 19-5 and Figure 19-6 depict time-out sequences.

Since the time-outs occur from the POR pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then, bringing $\overline{MCLR}$ high will begin execution immediately (see Figure 19-5). This is useful for testing purposes or to synchronize more than one PIC16F753/HV753 device operating in parallel.

Table shows the Reset conditions for some special registers, while Table 19-4 shows the Reset conditions for all the registers.

19.3.6 POWER CONTROL (PCON) REGISTER

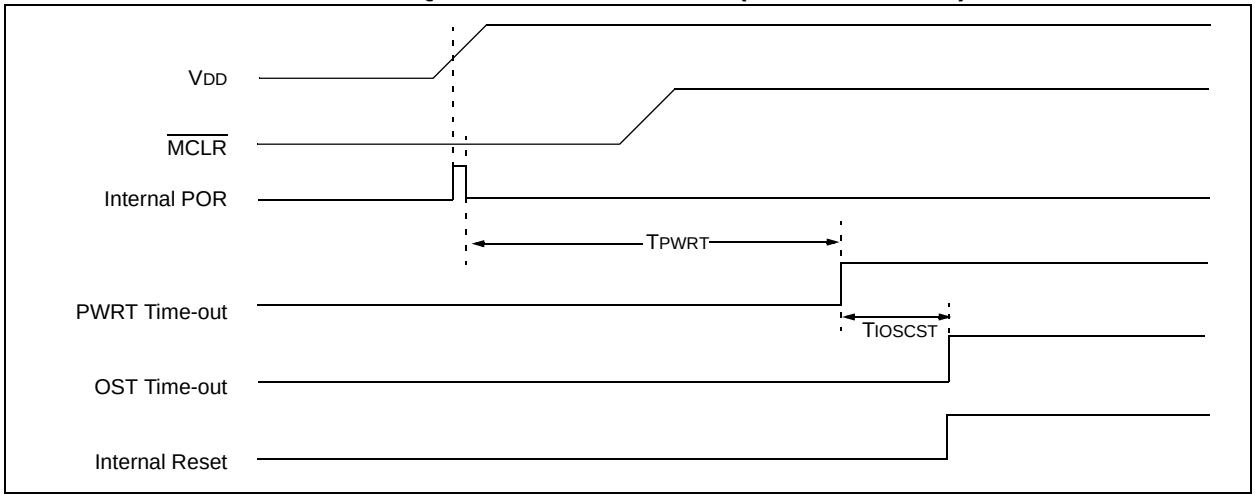
The Power Control register PCON (address 8Eh) has two Status bits to indicate what type of Reset occurred last.

Bit 0 is $\overline{BOR}$ (Brown-out). $\overline{BOR}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if $\overline{BOR}$ = 0, indicating that a Brown-out has occurred. The $\overline{BOR}$ Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (BOREN<1:0> = 00 in the Configuration Word register).

Bit 1 is $\overline{POR}$ (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent Reset, if $\overline{POR}$ is '0', it will indicate that a Power-on Reset has occurred (i.e., V_{DD} may have gone too low).

For more information, see **Section 19.3.4 "Brown-out Reset (BOR)"**.

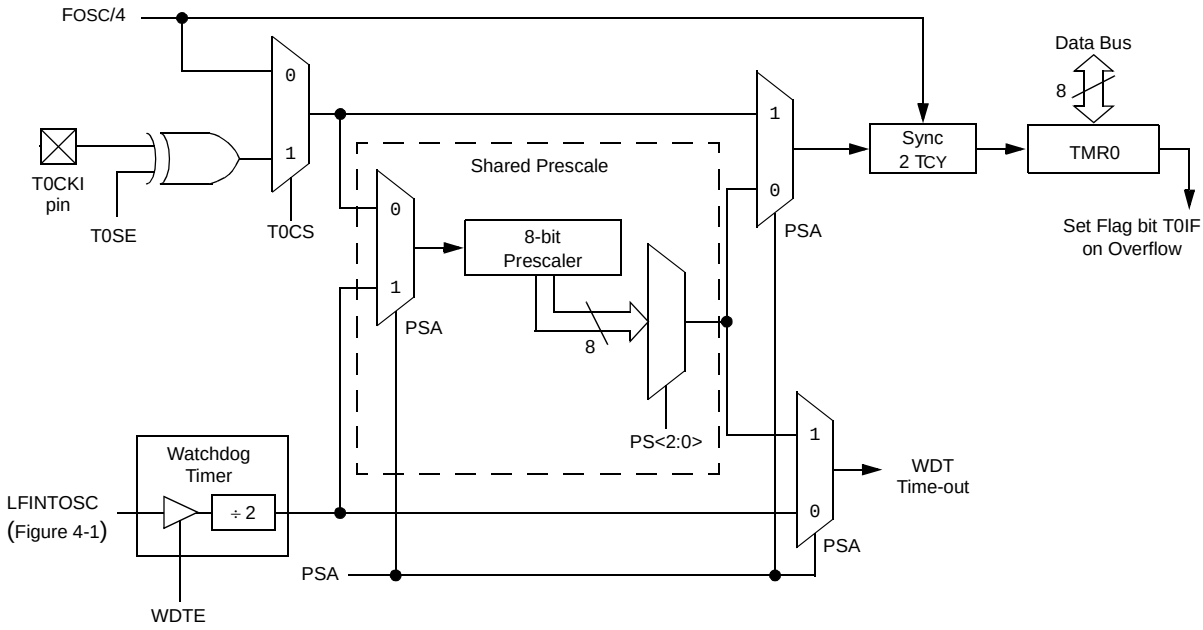
FIGURE 19-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{MCLR}$): CASE 1



19.6.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst-case conditions (i.e., VDD = Min., Temperature = Max., Max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

FIGURE 19-9: WATCHDOG TIMER WITH SHARED PRESCALE BLOCK DIAGRAM



Note 1: T0SE, T0CS, PSA, PS<2:0> are bits in the OPTION_REG register.

2: WDTE bit is in the Configuration Word register.

TABLE 19-7: WDT STATUS

Conditions	WDT
WDTE = 0	Cleared
CLRWDT Command	
Exit Sleep	

TABLE 19-8: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS<2:0>			56

Legend: Shaded cells are not used by the Watchdog Timer.

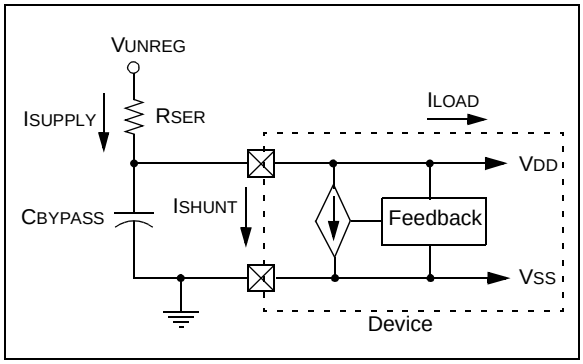
20.0 SHUNT REGULATOR (PIC16HV753 ONLY)

The PIC16HV753 devices include a permanent internal 5 volt (nominal) shunt regulator in parallel with the VDD pin. This eliminates the need for an external voltage regulator in systems sourced by an unregulated supply. All external devices connected directly to the VDD pin will share the regulated supply voltage and contribute to the total VDD supply current (ILOAD).

20.1 Regulator Operation

A shunt regulator generates a specific supply voltage by creating a voltage drop across a pass resistor RSER. The voltage at the VDD pin of the microcontroller is monitored and compared to an internal voltage reference. The current through the resistor is then adjusted, based on the result of the comparison, to produce a voltage drop equal to the difference between the supply voltage VUNREG and the VDD of the microcontroller. See Figure 20-1 for voltage regulator schematic.

FIGURE 20-1: SHUNT REGULATOR



An external current limiting resistor, RSER, located between the unregulated supply, VUNREG, and the VDD pin, drops the difference in voltage between VUNREG and VDD. RSER must be between RMAX and RMIN as defined by Equation 20-1.

EQUATION 20-1: RSER LIMITING RESISTOR

$$R_{MAX} = \frac{(VU_{MIN} - 5V)}{1.05 \bullet (1\ mA + I_{LOAD})}$$

$$R_{MIN} = \frac{(VU_{MAX} - 5V)}{0.95 \bullet (50\ mA)}$$

Where:

RMAX = maximum value of RSER (ohms)

RMIN = minimum value of RSER (ohms)

VUMIN = minimum value of VUNREG

VUMAX = maximum value of VUNREG

VDD = regulated voltage (5V nominal)

ILOAD = maximum expected load current in mA including I/O pin currents and external circuits connected to VDD.

1.05 = compensation for +5% tolerance of RSER

0.95 = compensation for -5% tolerance of RSER

20.2 Regulator Considerations

The supply voltage VUNREG and load current are not constant. Therefore, the current range of the regulator is limited. Selecting a value for RSER must take these three factors into consideration.

Since the regulator uses the band gap voltage as the regulated voltage reference, this voltage reference is permanently enabled in the PIC16HV753 devices.

The shunt regulator will still consume current when below operating voltage range for the shunt regulator.

20.3 Design Considerations

For more information on using the shunt regulator and managing current load, see Application Note *AN1035*, *Designing with HV Microcontrollers* (DS01035).

21.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

21.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

21.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

21.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

FIGURE 23-3: IDD TYPICAL, EC OSCILLATOR, MEDIUM-POWER MODE, PIC16F753 ONLY

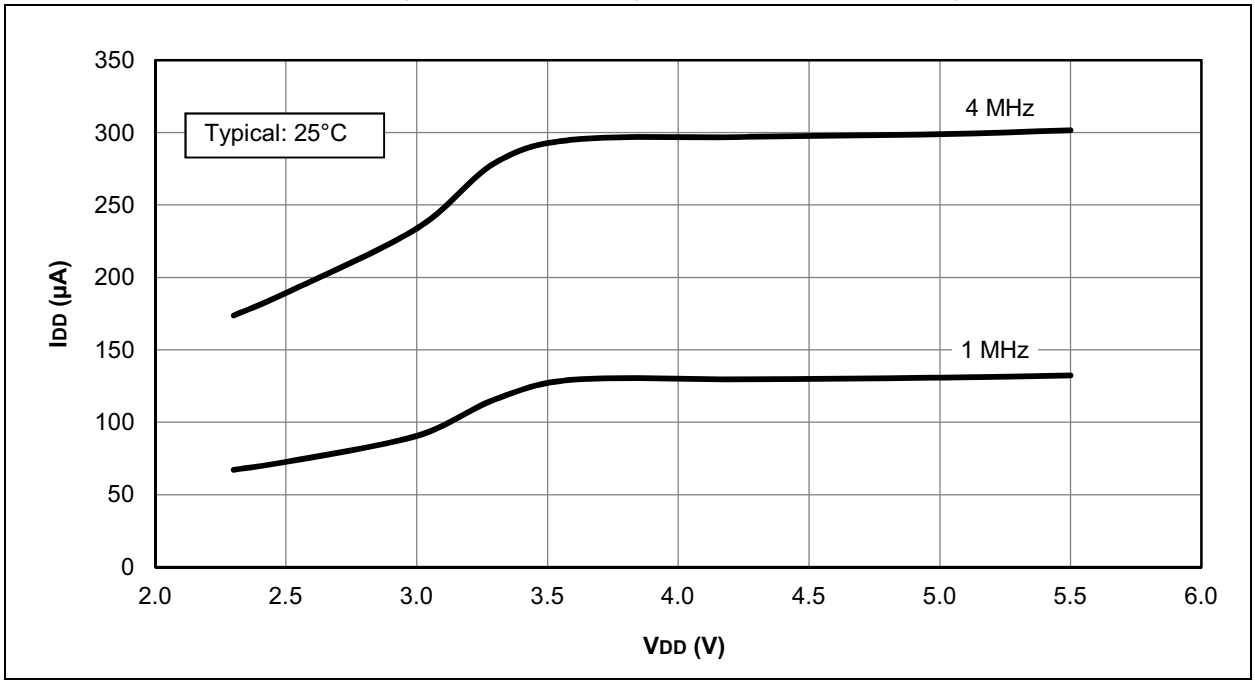


FIGURE 23-4: IDD MAXIMUM, EC OSCILLATOR, MEDIUM-POWER MODE, PIC16F753 ONLY

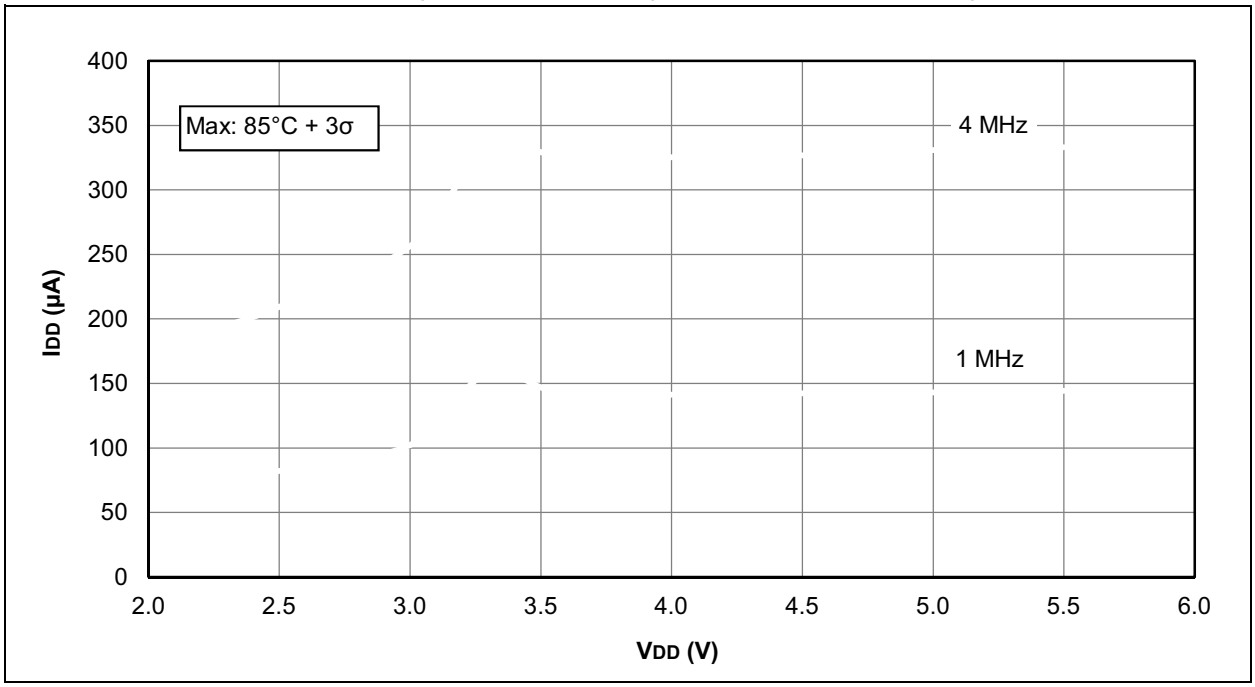


FIGURE 23-22: I_{PD}, DAC, PIC16HV753 ONLY

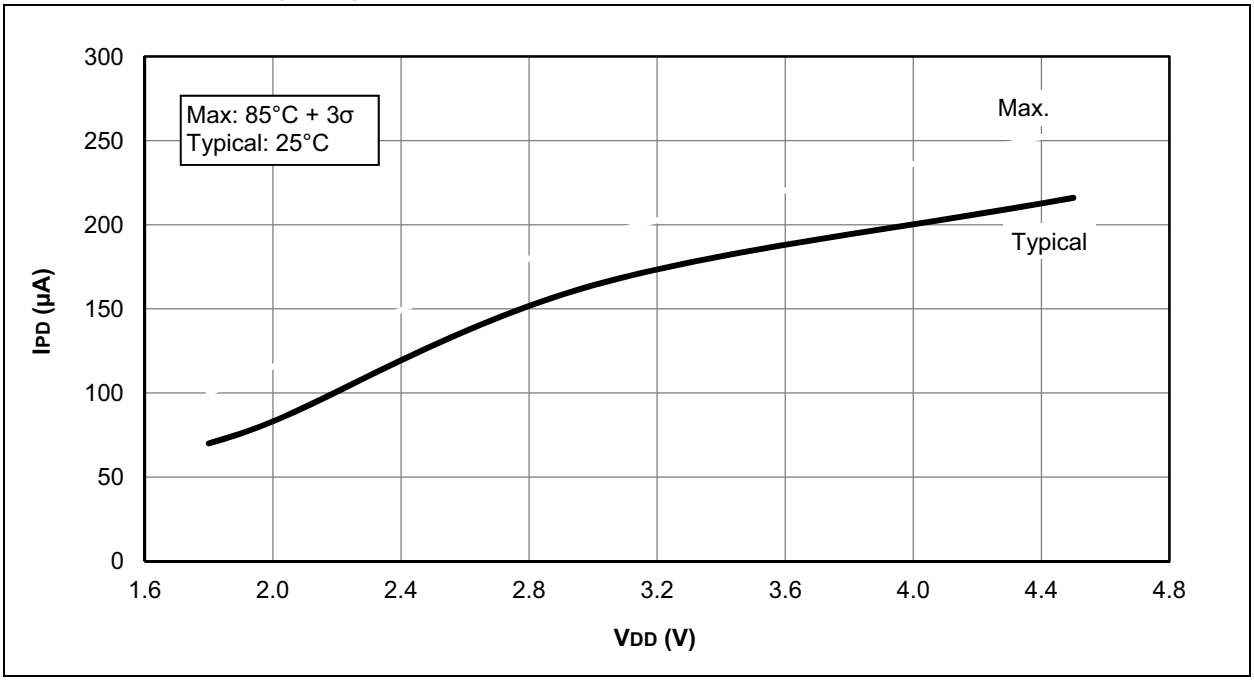


FIGURE 23-23: I_{PD}, DAC, PIC16F753 ONLY

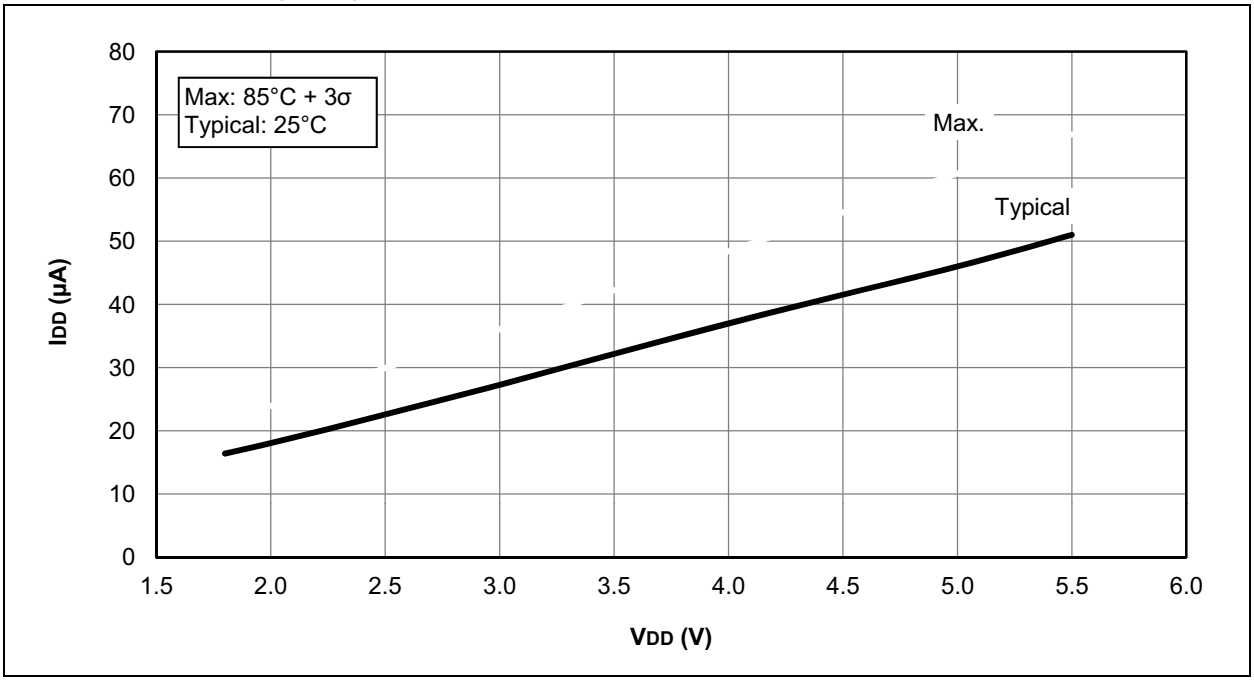


FIGURE 23-26: IPD, OP AMP, PIC16HV753 ONLY

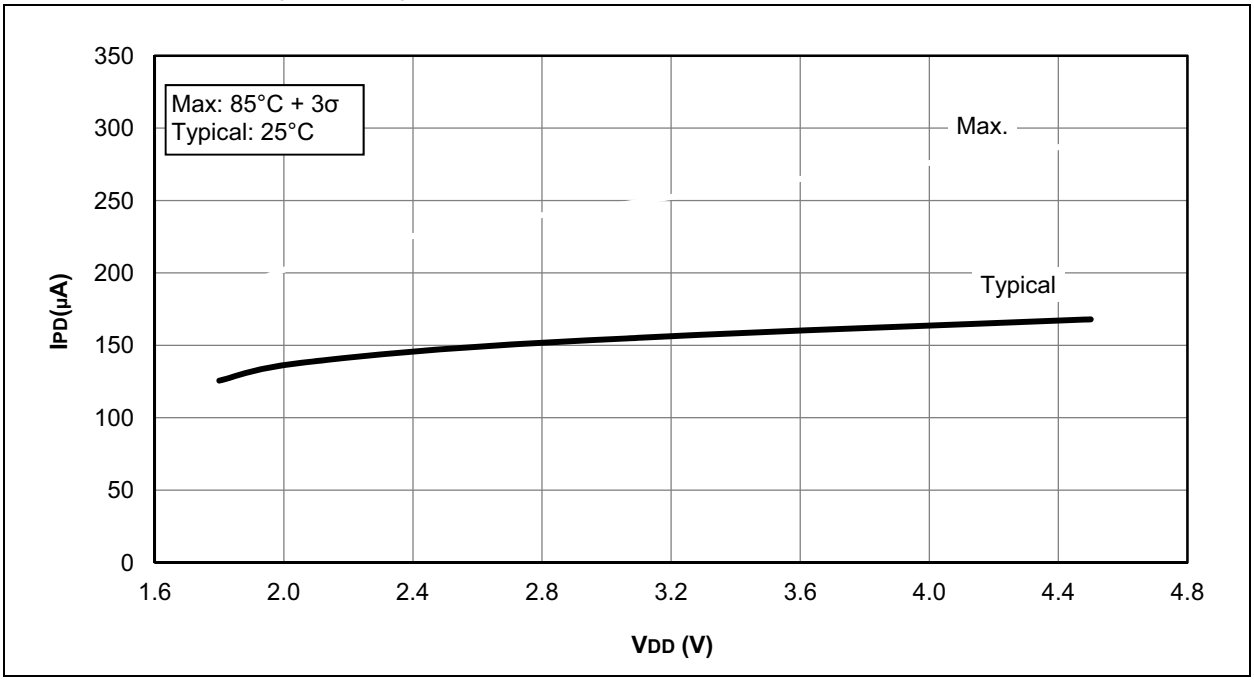
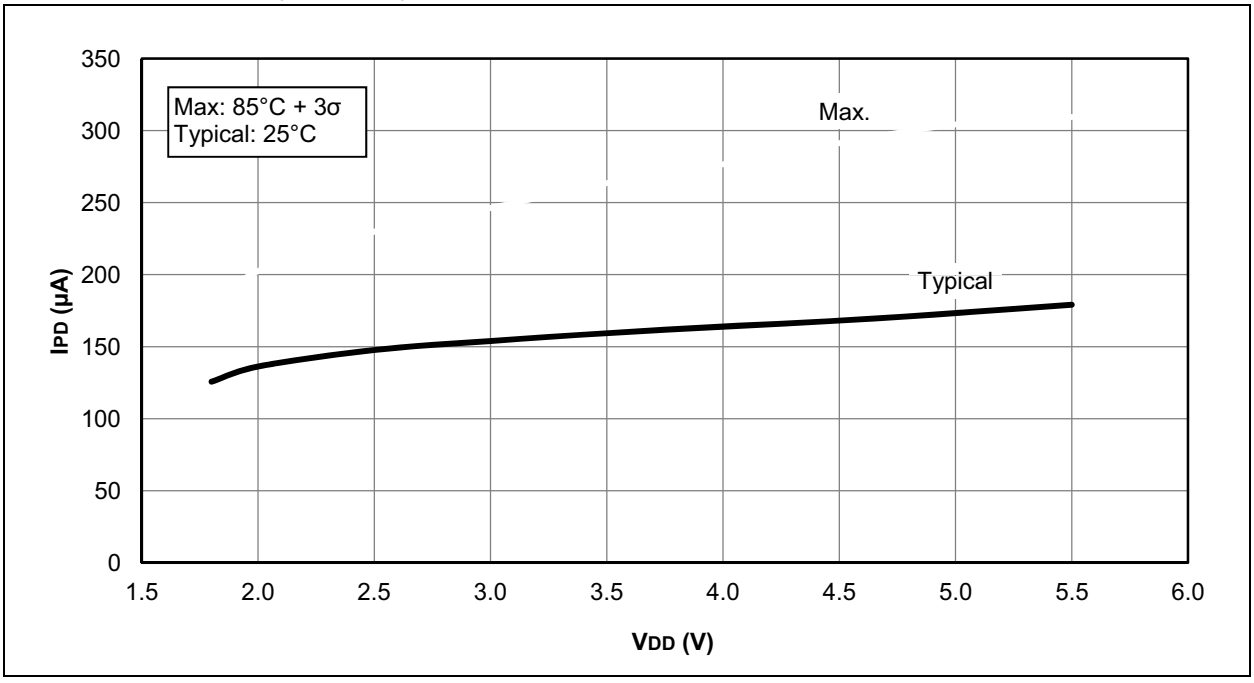
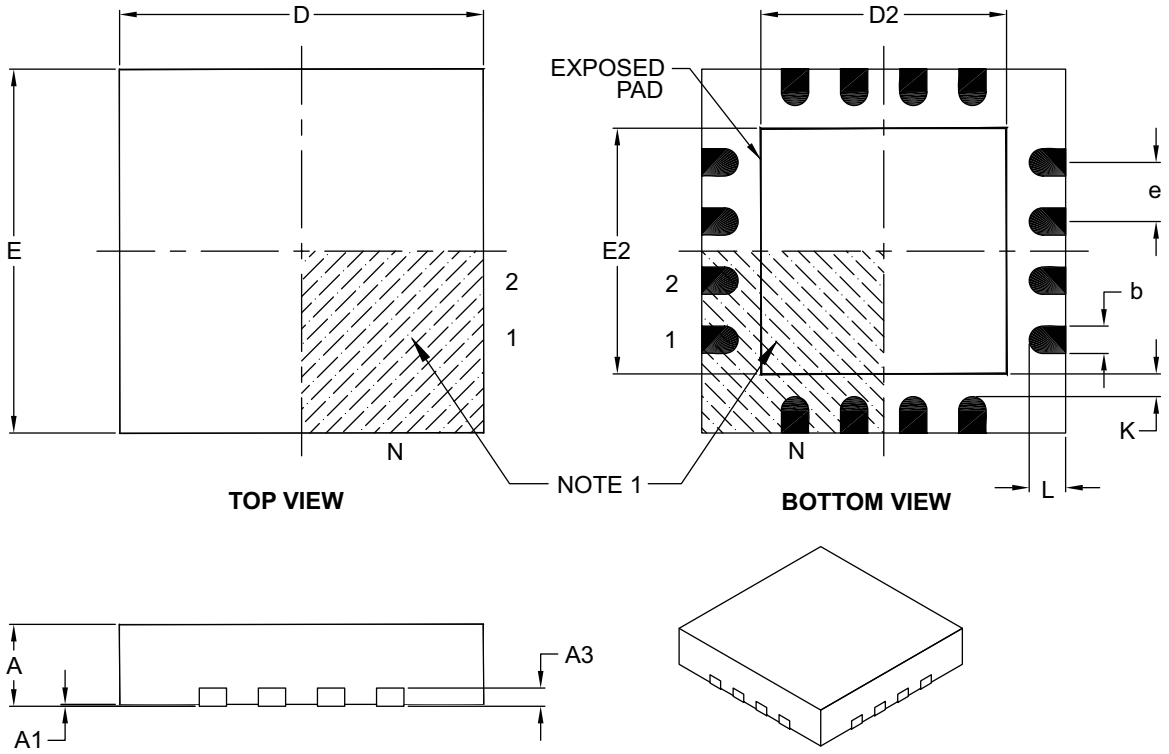


FIGURE 23-27: IPD, OP AMP, PIC16F753 ONLY



16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.65	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.65	2.80
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B