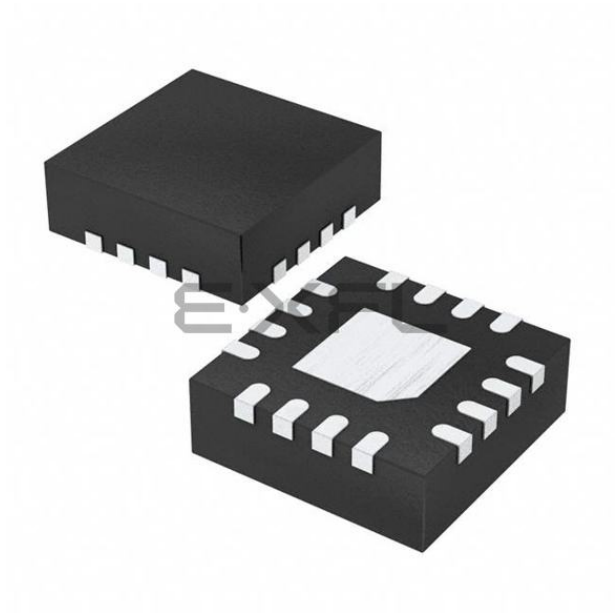

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 8x10b; D/A 1x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VQFN Exposed Pad
Supplier Device Package	16-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16hv753-e-ml

2.3.6 PIR1 REGISTER

The PIR1 register contains the Peripheral Interrupt flag bits, as shown in Register 2-6.

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-6: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR1GIF	ADIF	—	—	HLTMR2IF	HLTMR1IF	TMR2IF	TMR1IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TMR1GIF:** TMR1 Gate Interrupt Flag bit
1 = Timer1 gate interrupt is pending
0 = Timer1 gate interrupt is not pending

bit 6 **ADIF:** ADC Interrupt Flag bit
1 = ADC conversion complete
0 = ADC conversion has not completed or has not been started

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **HLTMR2IF:** HLT2 to HLTPR2 Match Interrupt Flag bit
1 = HLT2 to HLTPR2 match occurred (must be cleared in software)
0 = HLT2 to HLTPR2 match did not occur

bit 2 **HLTMR1IF:** HLT1 to HLTPR1 Match Interrupt Flag bit
1 = HLT1 to HLTPR1 match occurred (must be cleared in software)
0 = HLT1 to HLTPR1 match did not occur

bit 1 **TMR2IF:** Timer2 to PR2 Match Interrupt Flag bit
1 = Timer2 to PR2 match occurred (must be cleared in software)
0 = Timer2 to PR2 match did not occur

bit 0 **TMR1IF:** Timer1 Interrupt Flag bit
1 = Timer1 rolled over (must be cleared in software)
0 = Timer1 has not rolled over

3.0 FLASH PROGRAM MEMORY SELF-READ/SELF-WRITE CONTROL

The Flash program memory is readable and writable during normal operation (full V_{DD} range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers (see Registers 3-1 to 3-5). There are six SFRs used to read and write this memory:

- PMCON1
- PMCON2
- PMDATL
- PMDATH
- PMADRL
- PMADRH

When interfacing the program memory block, the PMDATL and PMDATH registers form a two-byte word which holds the 14-bit data for read/write, and the PMADRL and PMADRH registers form a two-byte word which holds the 10-bit address of the Flash location being accessed. These devices have 1K words of program Flash with an address range from 0000h to 03FFh.

The program memory allows a single-word read and a four-word write. A four-word write automatically erases the row of the location and writes the new data (erase before write).

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the voltage range of the device for byte or word operations.

When the device is code-protected, the CPU may continue to read and write the Flash program memory.

Depending on the settings of the Flash Program Memory Enable (WRT<1:0>) bits, the device may or may not be able to write certain blocks of the program memory; however, reads of the program memory are allowed.

When the Flash program memory Code Protection ($\overline{CP}$) bit in the Configuration Word register is enabled, the program memory is code-protected, and the device programmer (ICSP™) cannot access data or program memory.

3.1 PMADRH and PMADRL Registers

The PMADRH and PMADRL registers can address up to a maximum of 1K words of program memory.

When selecting a program address value, the Most Significant Byte (MSB) of the address is written to the PMADRH register and the Least Significant Byte (LSB) is written to the PMADRL register.

3.2 PMCON1 and PMCON2 Registers

PMCON1 is the control register for the data program memory accesses.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear.

PMCON2 is not a physical register. Reading PMCON2 will read all '0's. The PMCON2 register is used exclusively in the Flash memory write sequence.

4.2 Clock Source Modes

Clock Source modes can be classified as external or internal:

- The External Clock mode relies on an external clock for the clock source. For example, a clock module or clock output from another circuit.
- Internal clock sources are contained internally within the oscillator module. The oscillator module has four selectable clock frequencies:
  - 8 MHz
  - 4 MHz
  - 1 MHz
  - 31 kHz

The system clock can be selected between external or internal clock sources via the FOSC0 bit of the Configuration Word register (CONFIG).

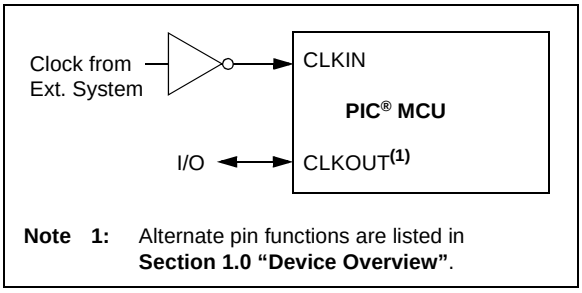
4.2.1 EC MODE

The External Clock (EC) mode allows an externally generated logic as the system clock source. The EC clock mode is selected when the FOSC0 bit of the Configuration Word is set.

When operating in this mode, an external clock source must be connected to the CLKIN input. The CLKOUT is available for either general purpose I/O or system clock output. Figure 4-3 shows the pin connections for EC mode.

Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 4-3: EXTERNAL CLOCK (EC) MODE OPERATION



Note 1: Alternate pin functions are listed in **Section 1.0 "Device Overview"**.

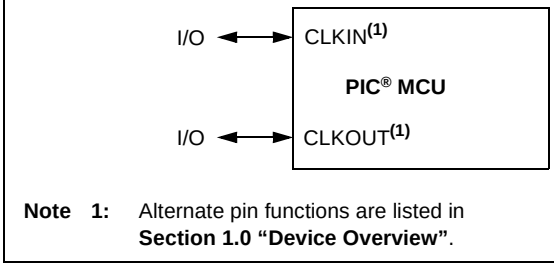
4.2.2 INTERNAL CLOCK MODE

Internal Clock mode configures the internal oscillators as the system clock source. The Internal Clock mode is selected when the FOSC0 bit of the Configuration Word is cleared. The source and frequency are selected with the IRCF<1:0> bits of the OSCCON register.

When one of the HFINTOSC frequencies is selected, the frequency of the internal oscillator can be trimmed by adjusting the TUN<4:0> bits of the OSCTUNE register.

Operation after a Power-on Reset (POR) or wake-up from Sleep is delayed by the oscillator start-up time. Delays are typically longer for the LFINTOSC than HFINTOSC because of the very low-power operation and relatively narrow bandwidth of the LF internal oscillator. However, when another peripheral keeps the oscillator running during Sleep, the start-up time is delayed to allow the memory bias to stabilize.

FIGURE 4-4: INTERNAL CLOCK MODE OPERATION



Note 1: Alternate pin functions are listed in **Section 1.0 "Device Overview"**.

4.2.2.1 Oscillator Ready Bits

The HTS and LTS bits of the OSCCON register indicate the status of the HFINTOSC and LFINTOSC, respectively. When either bit is set, it indicates that the corresponding oscillator is running and stable.

5.1 Alternate Pin Function

The Alternate Pin Function Control (APFCON) register is used to steer specific peripheral input and output functions between different pins. The APFCON register is shown in Register 5-1. For this device family, the following functions can be moved between different pins.

- Timer1 Gate
- COG1

These bits have no effect on the values of any TRIS register. PORT and TRIS overrides will be routed to the correct pin. The unselected pin will be unaffected.

5.2 Register Definitions: Alternate Pin Function Control

REGISTER 5-1: APFCON: ALTERNATE PIN FUNCTION CONTROL REGISTER

U-0	U-0	U-0	R/W-0/0	U-0	U-0	U-0	U-0
—	—	—	T1GSEL	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **T1GSEL:** Timer 1 Gate Input Pin Selection bit
1 = T1G function is on RA3
0 = T1G function is on RA4

bit 3-0 **Unimplemented:** Read as ‘0’

5.4 Additional Pin Functions

Every PORTA pin on the PIC16F753 has an interrupt-on-change option and a weak pull-up option. The next three sections describe these functions.

5.4.1 ANSELA REGISTER

The ANSELA register (Register 5-5) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELA bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

5.4.2 WEAK PULL-UPS

Each of the PORTA pins, except RA3, has an individually configurable internal weak pull-up. Control bits WPUx enable or disable each pull-up. Refer to Register 5-6. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the $\overline{\text{RAPU}}$ bit of the OPTION_REG register. A weak pull-up is automatically enabled for RA3 when configured as $\overline{\text{MCLR}}$ and disabled when RA3 is an I/O. There is no software control of the $\overline{\text{MCLR}}$ pull-up.

5.4.3 INTERRUPT-ON-CHANGE

Each PORTA pin is individually configurable as an interrupt-on-change pin. Control bits IOCA enable or disable the interrupt function for each pin. Refer to Register 5-7. The interrupt-on-change is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of PORTA. The 'mismatch' outputs of the last read are OR'd together to set the PORTA Change Interrupt Flag bit (IOCIF) in the INTCON register (Register 2-3).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, clears the interrupt by:

a) Any read of PORTA AND Clear flag bit IOCIF. This will end the mismatch condition;

   OR

b) Any write of PORTA AND Clear flag bit IOCIF will end the mismatch condition;

A mismatch condition will continue to set flag bit IOCIF. Reading PORTA will end the mismatch condition and allow flag bit IOCIF to be cleared. The latch holding the last read value is not affected by a $\overline{\text{MCLR}}$ nor BOR Reset. After these Resets, the IOCIF flag will continue to be set if a mismatch is present.

Note:	If a change on the I/O pin should occur when any PORTA operation is being executed, then the IOCIF interrupt flag may not get set.

6.0 TIMER0 MODULE

The Timer0 module is an 8-bit timer/counter with the following features:

- 8-bit timer/counter register (TMR0)
- 8-bit prescaler (shared with Watchdog Timer)
- Programmable internal or external clock source
- Programmable external clock edge selection
- Interrupt on overflow

Figure 6-1 is a block diagram of the Timer0 module.

6.1 Timer0 Operation

When used as a timer, the Timer0 module can be used as either an 8-bit timer or an 8-bit counter.

6.1.1 8-BIT TIMER MODE

When used as a timer, the Timer0 module will increment every instruction cycle (without prescaler). Timer mode is selected by clearing the T0CS bit of the OPTION register to '0'.

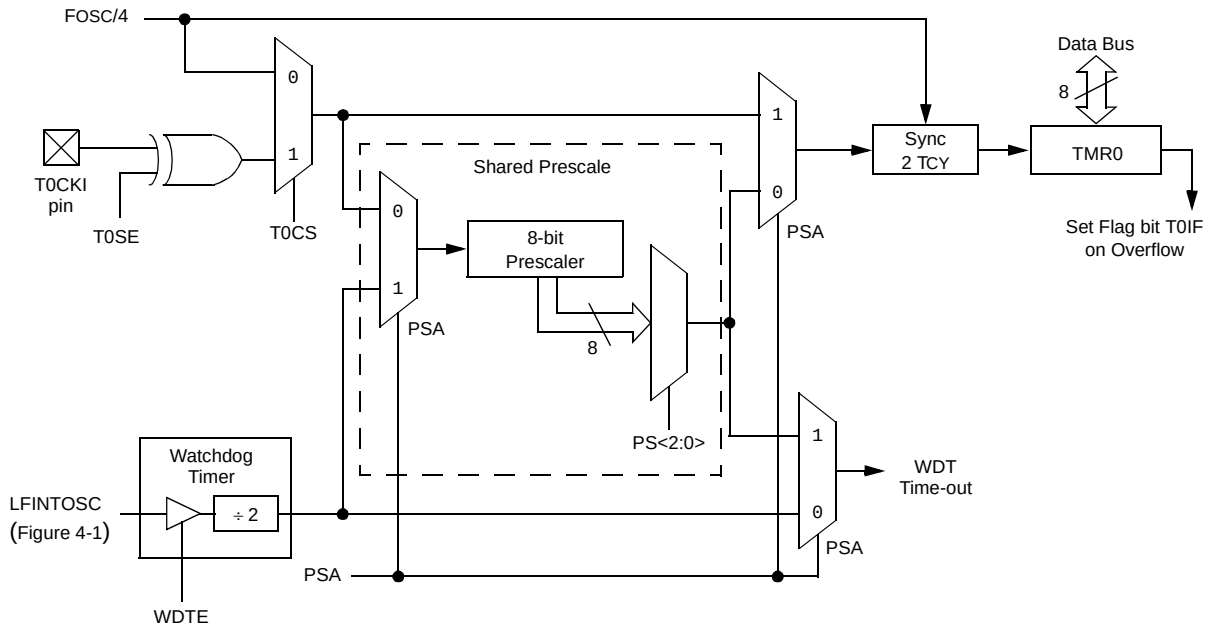
When TMR0 is written, the increment is inhibited for two instruction cycles immediately following the write.

Note:	The value written to the TMR0 register can be adjusted, in order to account for the two instruction cycle delay when TMR0 is written.

6.1.2 8-BIT COUNTER MODE

When used as a counter, the Timer0 module will increment on every rising or falling edge of the T0CKI pin. The incrementing edge is determined by the T0SE bit of the OPTION_REG register. Counter mode is selected by setting the T0CS bit of the OPTION register to '1'.

FIGURE 6-1: TIMER0 WITH SHARED PRESCALE BLOCK DIAGRAM



Note 1: T0SE, T0CS, PSA, PS<2:0> are bits in Register 6-1.

2: WDTE bit is in Register 19-1.

FIGURE 7-5: TIMER1 GATE SINGLE-PULSE MODE

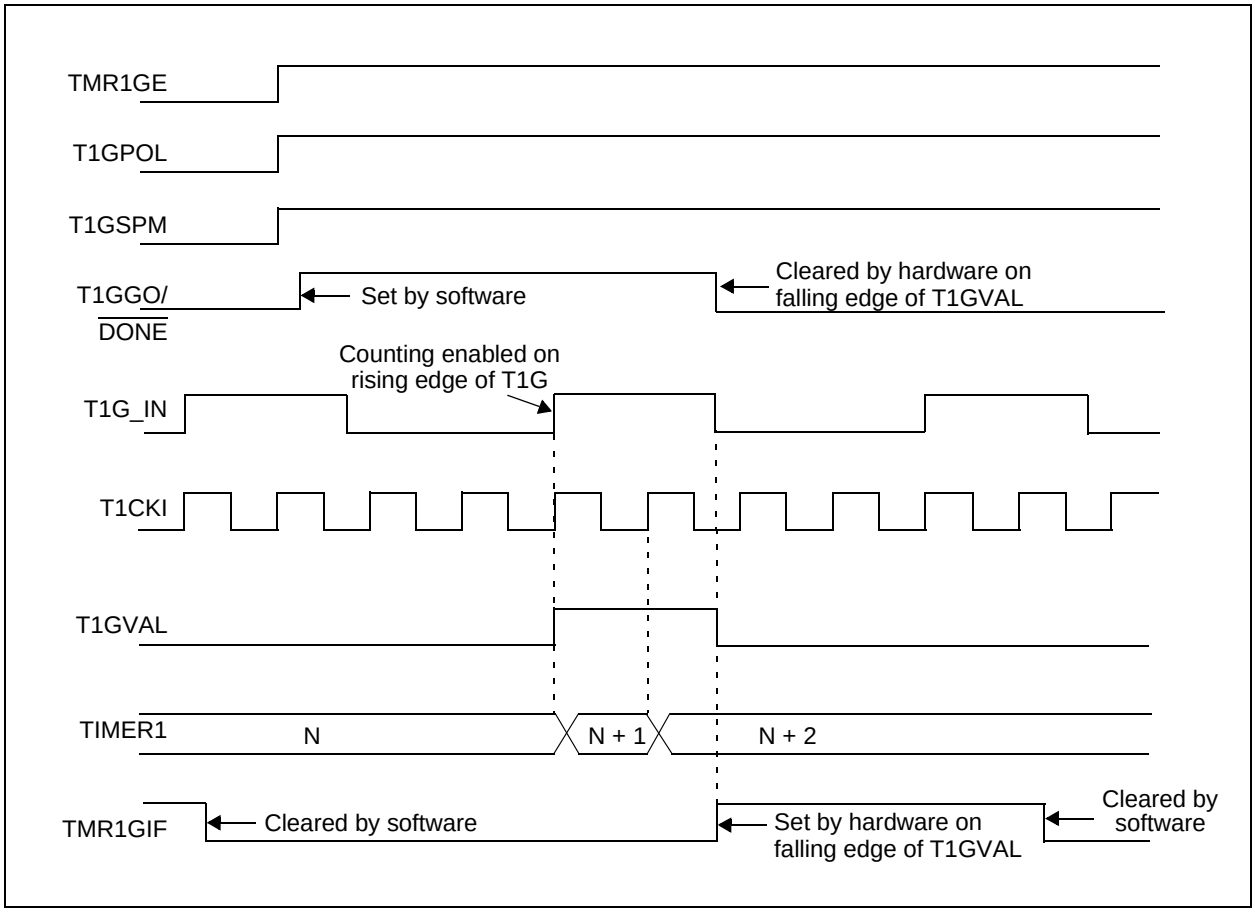
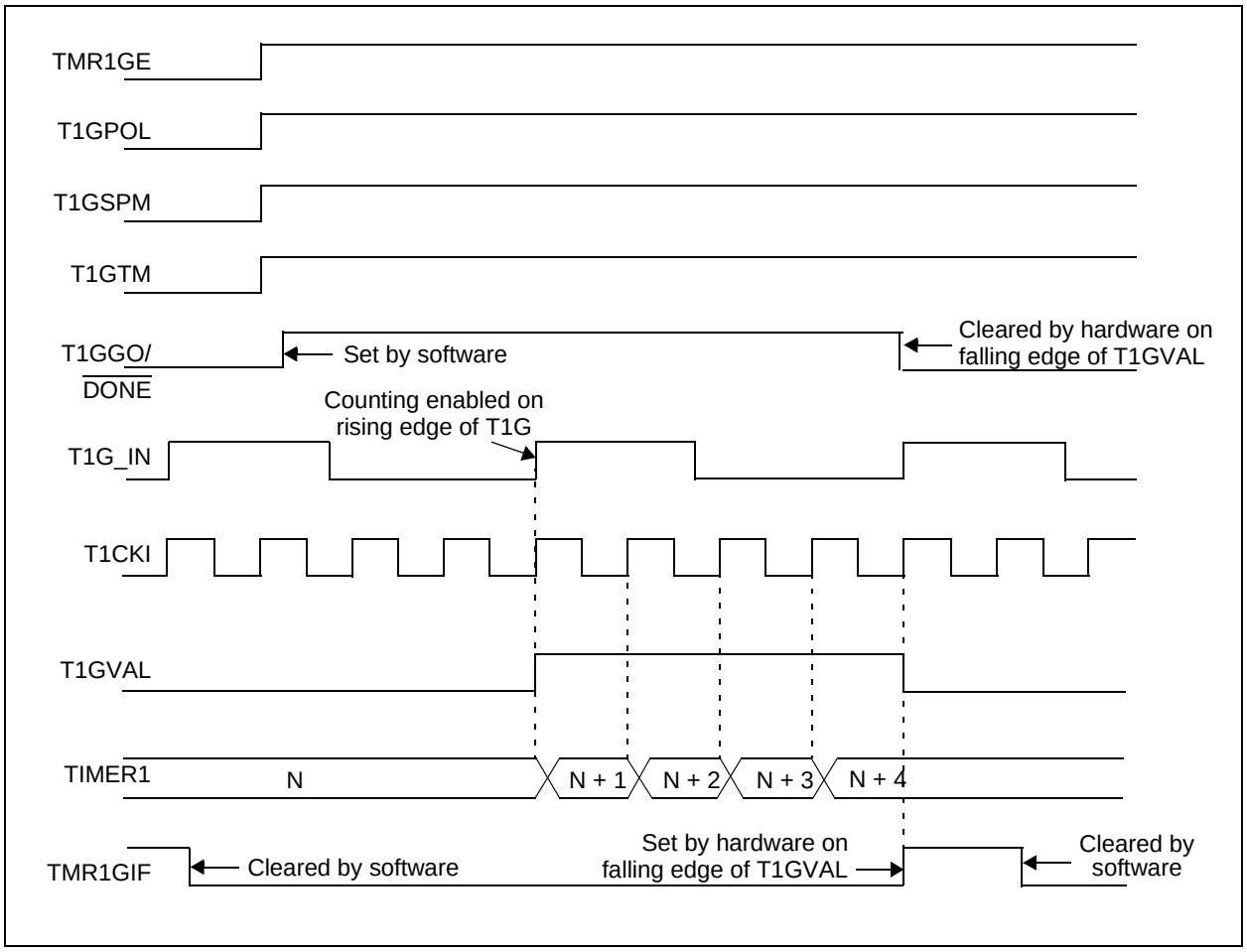


FIGURE 7-6: TIMER1 GATE SINGLE-PULSE AND TOGGLE COMBINED MODE



9.1 HLT Operation

The clock input to the HLT module is the system instruction clock (FOSC/4). HLTMRx increments on each rising clock edge.

A 4-bit counter/prescaler on the clock input provides the following prescale options:

- Direct input
- Divide-by-4
- Divide-by-16
- Divide-by-64

The prescale options are selected by the prescaler control bits, HxCKPS<1:0> of the HLTxCON0 register.

The value of HLTMRx is compared to that of the Period register, HLTPRx, on each clock cycle. When the two values match, then the comparator generates a match signal as the HLTimerx output. This signal also resets the value of HLTMRx to 00h on the next clock rising edge and drives the output counter/postscaler (see **Section 9.2 "HLT Interrupt"**).

The HLTMRx and HLTPRx registers are both directly readable and writable. The HLTMRx register is cleared on any device Reset, whereas the HLTPRx register initializes to FFh. Both the prescaler and postscaler counters are cleared on any of the following events:

- A write to the HLTMRx register
- A write to the HLTxCON0 register
- Power-on Reset (POR)
- Brown-out Reset (BOR)
- $\overline{\text{MCLR}}$ Reset
- Watchdog Timer (WDT) Reset
- Stack Overflow Reset
- Stack Underflow Reset
- RESET Instruction

Note:	HLTMRx is not cleared when HLTxCON0 is written.

9.2 HLT Interrupt

The HLT can also generate an optional device interrupt. The HLTMRx output signal (HLTMRx-to-HLTPRx match) provides the input for the 4-bit counter/postscaler. The overflow output of the postscaler sets the HLTMRxIF bit of the PIR1 register. The interrupt is enabled by setting the HLTMRx Match Interrupt Enable bit, HLTMRxIE of the PIE1 register.

A range of 16 postscale options (from 1:1 through 1:16 inclusive) can be selected with the postscaler control bits, HxOUTPS<3:0>, of the HLTxCON0 register.

9.3 Peripheral Resets

Resets driven from the selected peripheral output prevents the HLTMRx from matching the HLTPRx register and generating an output. In this manner, the HLT can be used as a hardware time limit to other peripherals.

In this device, the primary purpose of the HLT is to limit the COG PWM duty cycle. Normally, the COG operation uses analog feedback to determine the PWM duty cycle. The same feedback signal is used as an HLT Reset input. The HLTPRx register is set to occur at the maximum allowed duty cycle. If the analog feedback to the COG exceeds the maximum time, then an HLTMRx-to-HLTPRx match will occur and generate the output needed to limit the COG drive output.

The HLTMRx can be reset by one of several selectable peripheral sources. Reset inputs include:

- CCP1 output
- Comparator 1 output
- Comparator 2 output
- COGxFLT pin
- COG1OUT0
- COG1OUT1

The external Reset input is selected with the HxERS<2:0> bits of the HLTxCON1 register. High and low Reset enables are selected with the HxREREN and HxFEREN bits, respectively. Setting the HxRES and HxFES bits makes the respective rising and falling Reset events edge sensitive. Reset inputs that are not edge sensitive are level sensitive.

HLTMRx Resets are synchronous with the HLT clock. In other words, HLTMRx is cleared on the rising edge of the HLT clock after the enabled Reset event occurs.

If an enabled external Reset occurs at the same time a write occurs to the TMR4A register, the write to the timer takes precedence and pending Resets are cleared.

9.4 HLTimerx Output

The unscaled output of HLTMRx is available only to the COG module, where it is used as a selectable limit to the maximum COG period.

9.5 HLT Operation During Sleep

The HLT cannot be operated while the processor is in Sleep mode. The contents of the HLTMRx register will remain unchanged while the processor is in Sleep mode.

11.5.4 RISING EVENT DEAD BAND

Rising event dead band adds a delay between the COGxOUT1 signal deactivation and the COGxOUT0 signal activation. The rising event dead-band time starts when the rising_event output goes true.

See Section 11.5.1, Asynchronous Delay Chain Dead-band Delay and Section 11.5.2, Synchronous Counter Dead-band Delay for more information on setting the rising edge dead-band time.

11.5.5 FALLING EVENT DEAD BAND

Falling event dead band adds a delay between the COGxOUT1 signal deactivation and the COGxOUT0 signal activation. The falling event dead-band time starts when the falling_event output goes true.

See Section 11.5.1, Asynchronous Delay Chain Dead-band Delay and Section 11.5.2, Synchronous Counter Dead-band Delay for more information on setting the rising edge dead-band time.

11.5.6 DEAD-BAND OVERLAP

There are two cases of dead-band overlap:

- Rising-to-falling
- Falling-to-rising

11.5.6.1 Rising-to-Falling Overlap

In this case, the falling event occurs while the rising event dead-band counter is still counting. When this happens, the COGxOUT0 drive is suppressed and the dead band extends by the falling event dead-band time. At the termination of the extended dead-band time, the COGxOUT1 drive goes true.

11.5.6.2 Falling-to-Rising Overlap

In this case, the rising event occurs while the falling event dead-band counter is still counting. When this happens, the COGxOUT1 drive is suppressed and the dead band extends by the rising event dead-band time. At the termination of the extended dead-band time, the COGxOUT0 drive goes true.

11.6 Blanking Control

Input blanking is a function, whereby the event inputs can be masked or blanked for a short period of time. This is to prevent electrical transients caused by the turn-on/off of power components from generating a false input event.

The COG contains two blanking counters: one triggered by the rising event and the other triggered by the falling event. The counters are cross-coupled with the events they are blanking. The falling event blanking counter is used to blank rising input events and the rising event blanking counter is used to blank falling input events. Once started, blanking extends for the time specified by the corresponding blanking counter.

Blanking is timed by counting COG_clock periods from zero up to the value in the blanking count register. Use Equation 11-1 to calculate blanking times.

11.6.1 FALLING EVENT BLANKING OF RISING EVENT INPUTS

The falling event blanking counter inhibits rising event inputs from triggering a rising event. The falling event blanking time starts when the rising event output drive goes false.

The falling event blanking time is set by the value contained in the COGxBKF register (Register 11-12). Blanking times are calculated using the formula shown in Equation 11-1.

When the COGxBKF value is zero, the falling event blanking is disabled and the blanking counter output is true, thereby allowing the event signal to pass straight through to the event trigger circuit.

11.6.2 RISING EVENT BLANKING OF FALLING EVENT INPUTS

The rising event blanking counter inhibits falling event inputs from triggering a falling event. The rising event blanking time starts when the falling event output drive goes false.

The rising event blanking time is set by the value contained in the COGxBKR register (Register 11-11).

When the COGxBKR value is zero, the rising event blanking is disabled and the blanking counter output is true, thereby allowing the event signal to pass straight through to the event trigger circuit.

11.6.3 BLANKING TIME UNCERTAINTY

When the rising and falling sources that trigger the blanking counters are asynchronous to the COG_clock, it creates uncertainty in the blanking time. The maximum uncertainty is equal to one COG_clock period. Refer to Equation 11-1 and Example 11-2 for more detail.

11.7 Phase Delay

It is possible to delay the assertion of either or both the rising event and falling event. This is accomplished by placing a non-zero value in COGxPHR or COGxPHF phase delay count register, respectively (Register 11-13 and Register 11-14). Refer to Figure 11-5 for COG operation with CCP1 and phase delay. The delay from the input rising event signal switching to the actual assertion of the events is calculated the same as the dead-band and blanking delays. Please see Equation 11-1.

REGISTER 12-2: ADCON1: A/D CONTROL REGISTER 1

U-0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	R/W-0/0
—	ADCS<2:0>			—	—	—	ADPREF1
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **ADCS<2:0>:** A/D Conversion Clock Select bits
000 = FOSC/2
001 = FOSC/8
010 = FOSC/32
011 = FRC (clock supplied from an internal oscillator with a divisor of 16)
100 = FOSC/4
101 = FOSC/16
110 = FOSC/64

bit 3-1 **Unimplemented:** Read as ‘0’

bit 0 **ADPREF1:** ADC Positive Voltage Reference Selection bit
0 = VDD
1 = VREF+

19.4 Interrupts

The PIC16F753/HV753 has multiple sources of interrupt:

- External Interrupt (INT pin)
- Interrupt-On-Change (IOC) Interrupts
- Timer0 Overflow Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- Hardware Limit Timer (HLT) Interrupt
- Comparator Interrupt (C1/C2)
- ADC Interrupt
- Complementary Output Generator (COG)
- CCP1 Interrupt
- Flash Memory Self-Write

The Interrupt Control register (INTCON) and Peripheral Interrupt Request Registers (PIRx) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

The Global Interrupt Enable bit, GIE of the INTCON register, enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in the INTCON register and PIEx registers. GIE is cleared on Reset.

When an interrupt is serviced, the following actions occur automatically:

- The GIE is cleared to disable any further interrupt.
- The return address is pushed onto the stack.
- The PC is loaded with 0004h.

The Return from Interrupt instruction, `RETFIE`, exits the interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT Pin Interrupt
- Interrupt-On-Change (IOC) Interrupts
- Timer0 Overflow Interrupt

The peripheral interrupt flags are contained in the PIR1 and PIR2 registers. The corresponding interrupt enable bit is contained in the PIE1 and PIE2 registers.

The following interrupt flags are contained in the PIR1 register:

- A/D Interrupt
- Comparator Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- Enhanced CCP Interrupt

For external interrupt events, such as the INT pin or PORTA change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 19-8). The latency is the same for one or two-cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

Note 1:	Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.
2:	When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts, which were ignored, are still pending to be serviced when the GIE bit is set again.

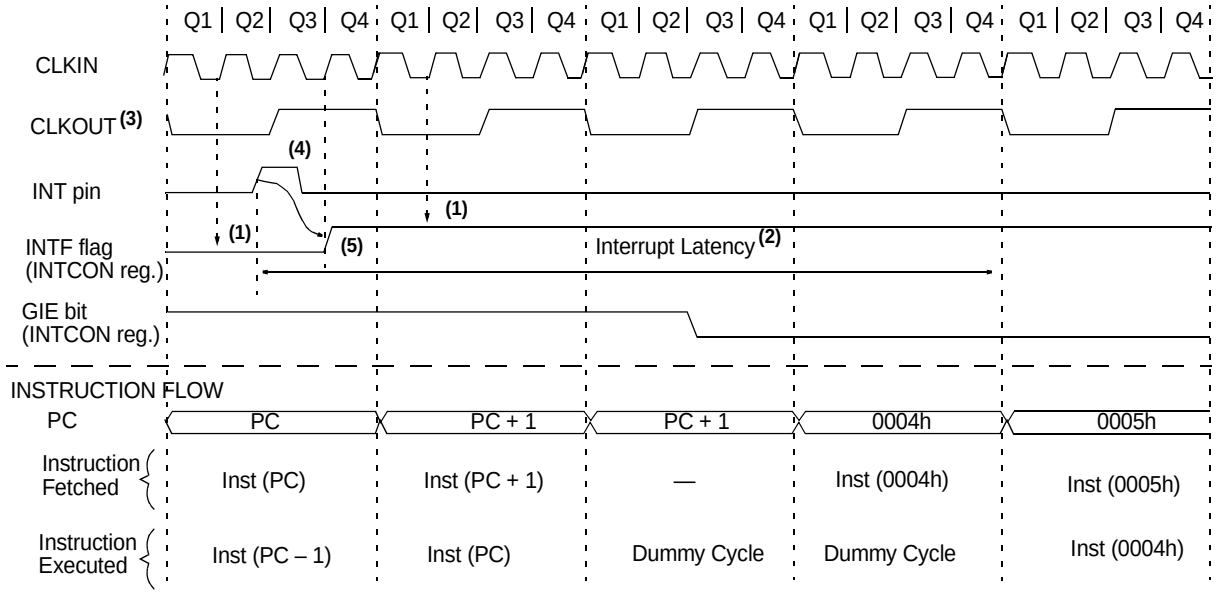
For additional information on Timer1, Timer2, comparators, ADC, Enhanced CCP modules, refer to the respective peripheral section.

19.4.1 RA2/INT INTERRUPT

The external interrupt on the RA2/INT pin is edge-triggered; either on the rising edge if the INTEDG bit of the OPTION register is set, or the falling edge, if the INTEDG bit is clear. When a valid edge appears on the RA2/INT pin, the INTF bit of the INTCON register is set. This interrupt can be disabled by clearing the INTE control bit of the INTCON register. The INTF bit must be cleared by software in the Interrupt Service Routine before re-enabling this interrupt. The RA2/INT interrupt can wake-up the processor from Sleep, if the INTE bit was set prior to going into Sleep. See **Section 19.7 "Power-Down Mode (Sleep)"** for details on Sleep and Figure 19-10 for timing of wake-up from Sleep through RA2/INT interrupt.

Note:	The ANSEL register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0' and cannot generate an interrupt.

FIGURE 19-8: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).

2: Asynchronous interrupt latency = 3-4 TCY. Synchronous latency = 3 TCY, where TCY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: CLKOUT is available only in INTOSC and RC Oscillator modes.

4: For minimum width of INT pulse, refer to AC specifications in **Section 22.0 "Electrical Specifications"**.

5: INTF is enabled to be set any time during the Q4-Q1 cycles.

TABLE 19-6: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	T0IE	INTE	IOCIE	T0IF	INTF	IOCIF	17
IOCAF	—	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	45
IOCAN	—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	45
IOCAP	—	—	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	45
LATA	—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0	43
PIE1	TMR1GIE	ADIE	—	—	HLTMR2IE	HLTMR1IE	TMR2IE	TMR1IE	18
PIR1	TMR1GIF	ADIF	—	—	HLTMR2IF	HLTMR1IF	TMR2IF	TMR1IF	20

Legend: x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by the interrupt module.

TABLE 19-9: SUMMARY OF CONFIGURATION WORD WITH WATCHDOG TIMER

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG(1)	13:8	—	—	$\overline{\text{DEBUG}}$	$\overline{\text{CLKOUTEN}}$	WRT<1:0>		BOREN<1:0>		150
	7:0	—	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	—	—	FOSC0	

Legend: — = unimplemented location, read as '1'. Shaded cells are not used by Watchdog Timer.

Note 1: See Register 19-1 for operation of all Configuration Word register bits.

22.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40° to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on pins with respect to V_{SS}

- on V_{DD} pin
  - PIC16HV753 ..... -0.3V to +6.5V
  - PIC16F753 ..... -0.3V to +6.5V
- on $\overline{MCLR}$ ..... -0.3V to +13.5V
- on all other pins ..... -0.3V to (V_{DD} + 0.3V)

Maximum current

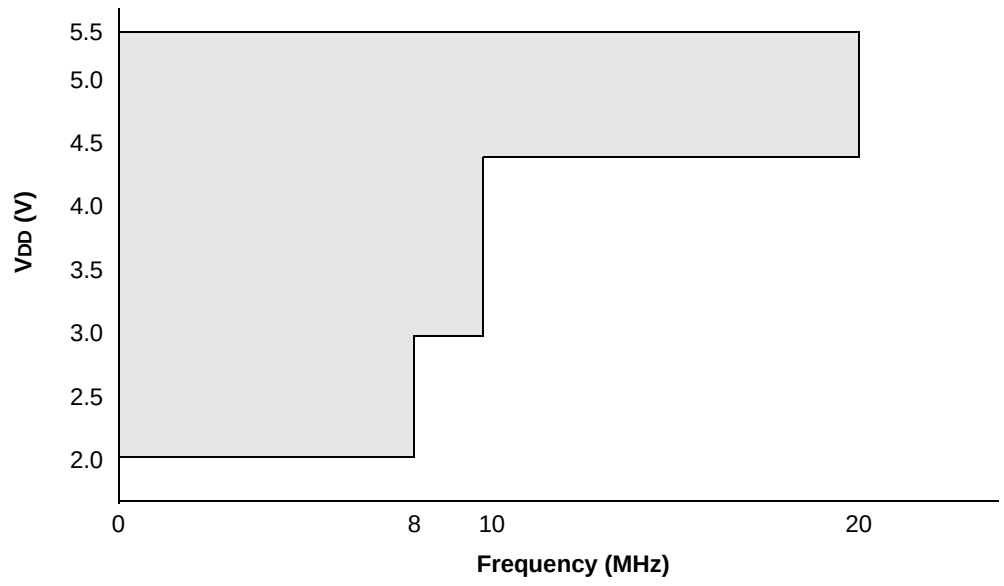
- on V_{SS} pin(1)
  - -40°C ≤ T_A ≤ +85°C ..... 95 mA
  - -40°C ≤ T_A ≤ +125°C ..... 95 mA
- on V_{DD} pin(1)
  - -40°C ≤ T_A ≤ +85°C ..... 95 mA
  - -40°C ≤ T_A ≤ +125°C ..... 95 mA
- on RA1, RA4, RA5 ..... 25 mA
- on RC4, RC5 ..... 50 mA

Clamp current, I_K (V_{PIN} < 0 or V_{PIN} > V_{DD}) ..... ± 20 mA

Note 1: Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characteristics. See Table 22-6 to calculate device specific limitations.

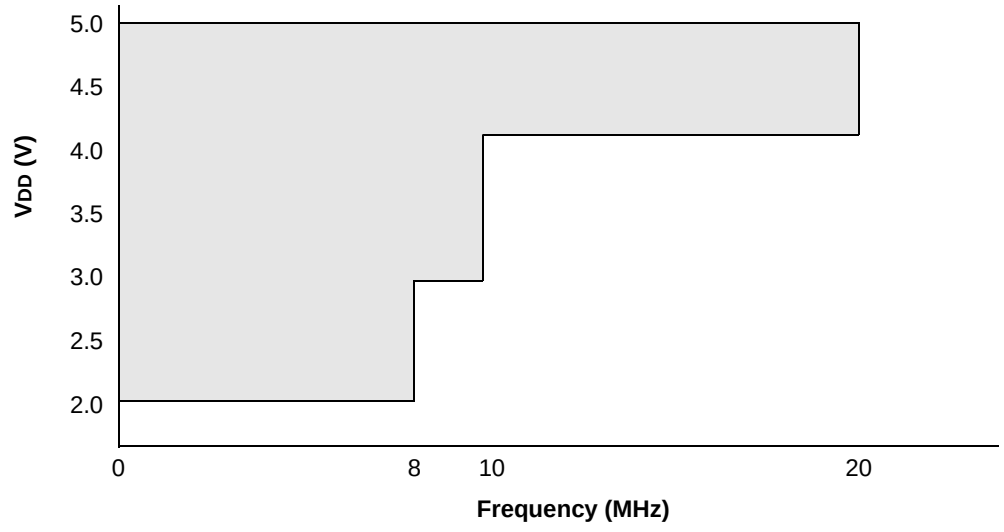
† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

FIGURE 22-1: PIC16F753 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 22-2: PIC16HV753 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

TABLE 22-18: ADC CONVERSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated) V_{DD} = 3.0V, T_A = 25°C							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
AD130 *	TAD	ADC Internal FRC Oscillator Period	3.0	6.0	9.0	µs	At VDD = 2.5V
			1.6	4.0	6.0	µs	At VDD = 5.0V
		ADC Clock Period	1.6	—	9.0	µs	FOSC-based, VREF ≥ 3.0V
			3.0	—	9.0	µs	TOSC-based, VREF full range(2)
AD131	TCNV	Conversion Time (not including Acquisition Time)(1)	—	11	—	TAD	Set GO/$\overline{\text{DONE}}$ bit to conversion complete
AD132 *	TACQ	Acquisition Time	—	11.5	—	µs	
AD133 *	TAMP	Amplifier Settling Time	—	—	5	µs	
AD134	TGO	Q4 to A/D Clock Start	—	TOSC/2	—	—	
	THCD	Holding Capacitor Disconnect Time	— —	1/2 TAD 1/2 TAD + 1 TCY	— —	—	FOSC-based ADCS<2:0> = x11 (ADC FRC mode)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The ADRES register may be read on the following TCY cycle. See **Section 12.4 "A/D Acquisition Requirements"** for minimum conditions.

2: Full range for PIC16HV753 powered by the shunt regulator is the 5V regulated voltage.

FIGURE 22-10: PIC16F753/HV753 A/D CONVERSION TIMING (ADC CLOCK FOSC-BASED)

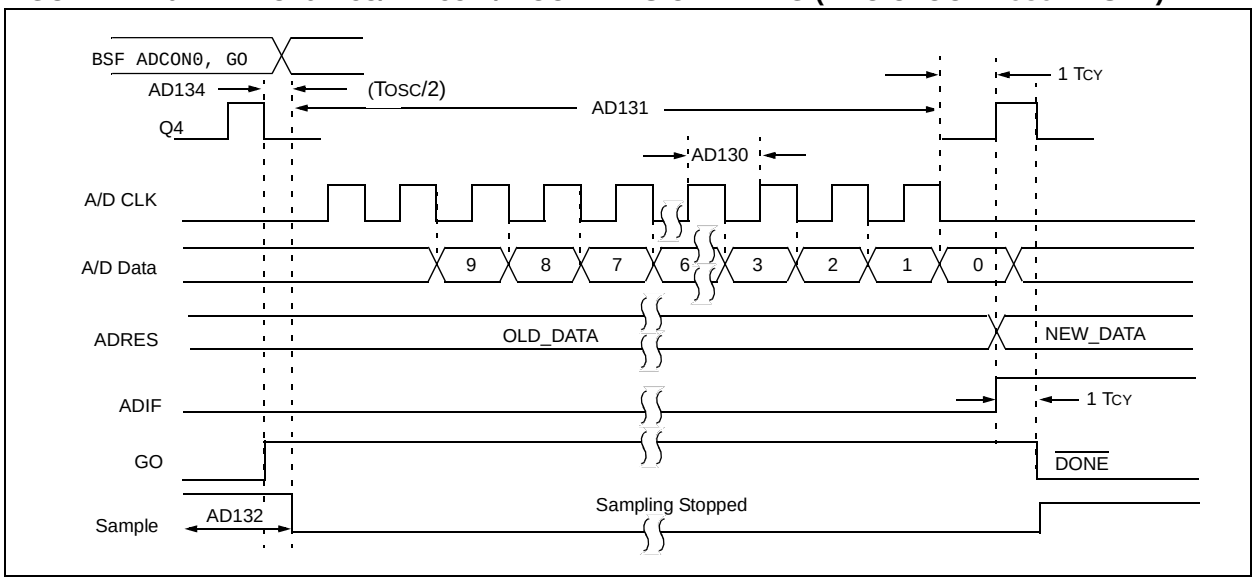


FIGURE 23-20: IPD, BROWN-OUT RESET (BOR), PIC16HV753 ONLY

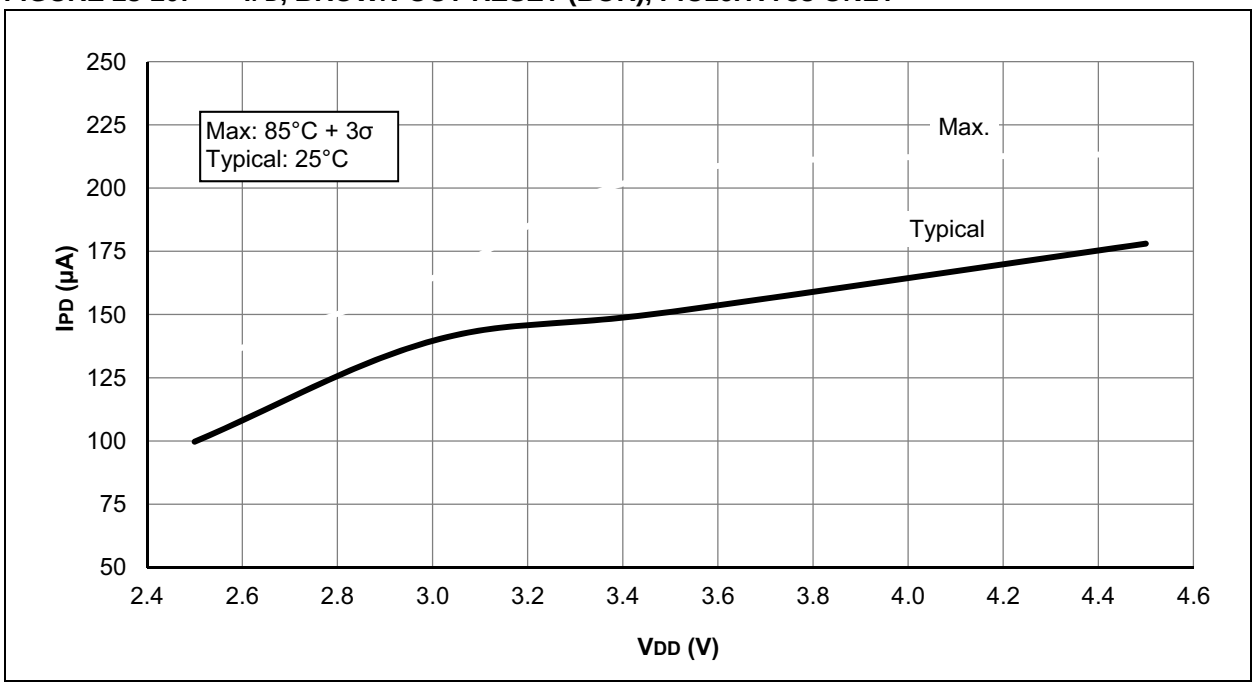


FIGURE 23-21: IPD, BROWN-OUT RESET (BOR), PIC16F753 ONLY

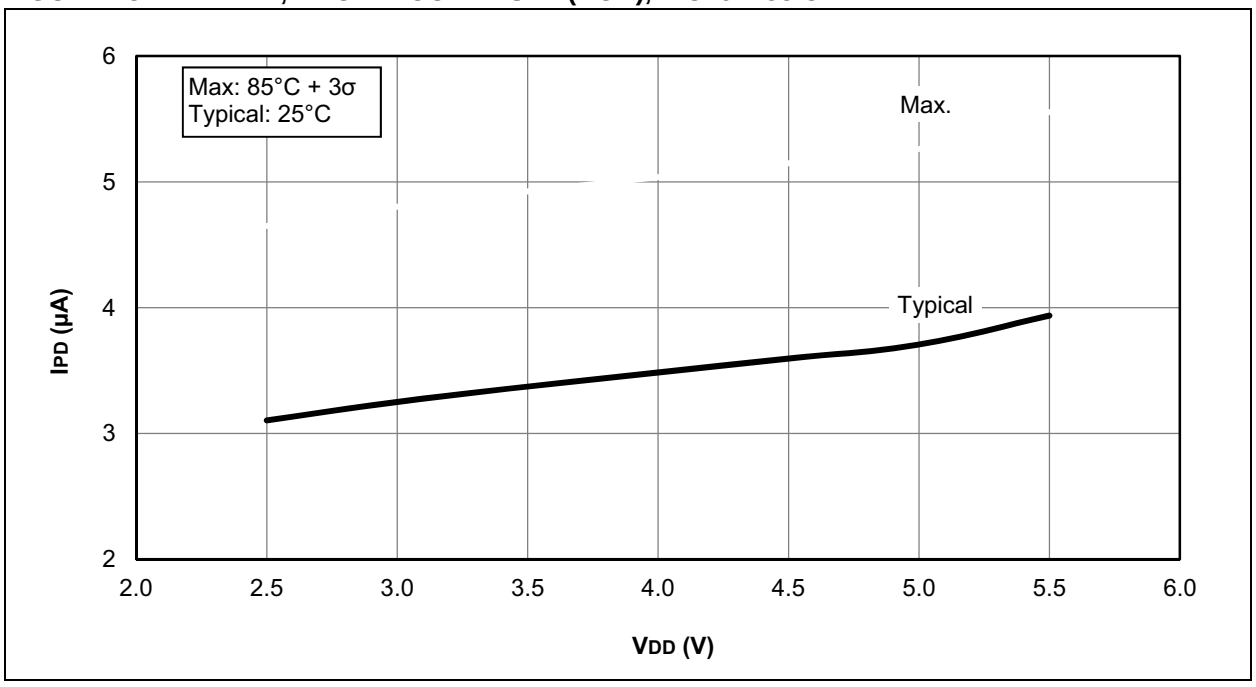


FIGURE 23-24: IPD, TIMER1 OSCILLATOR, FOSC = 32 kHz, PIC16HV753 ONLY

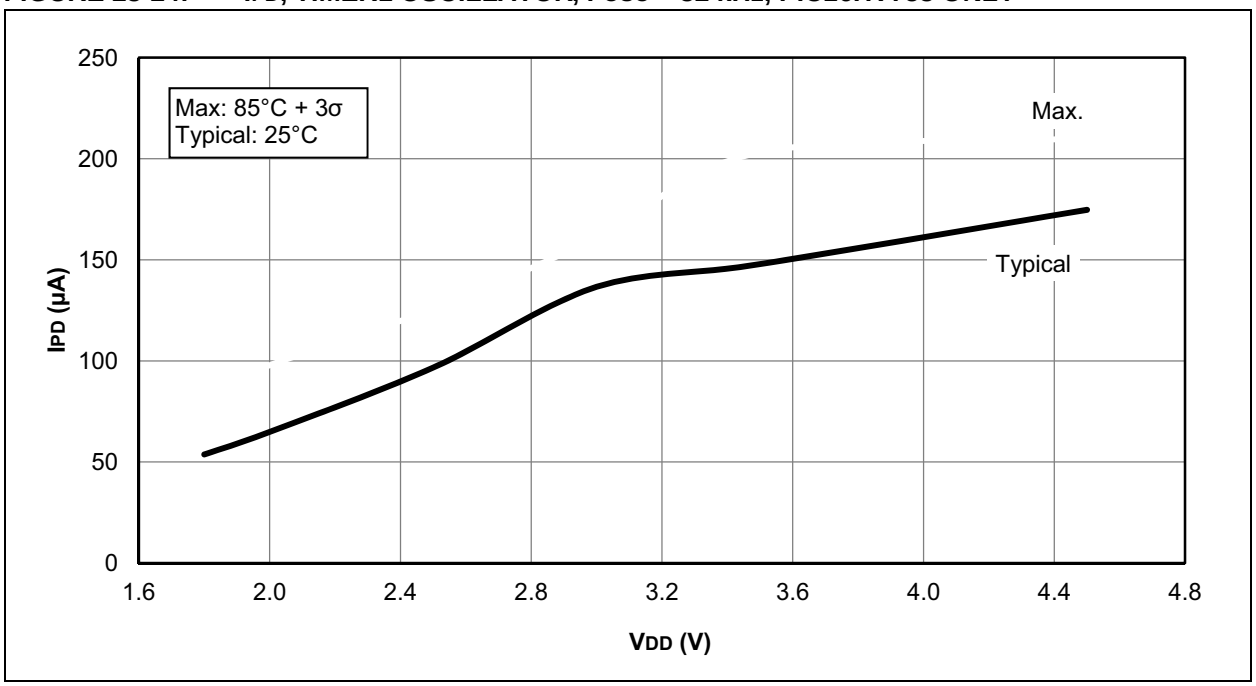
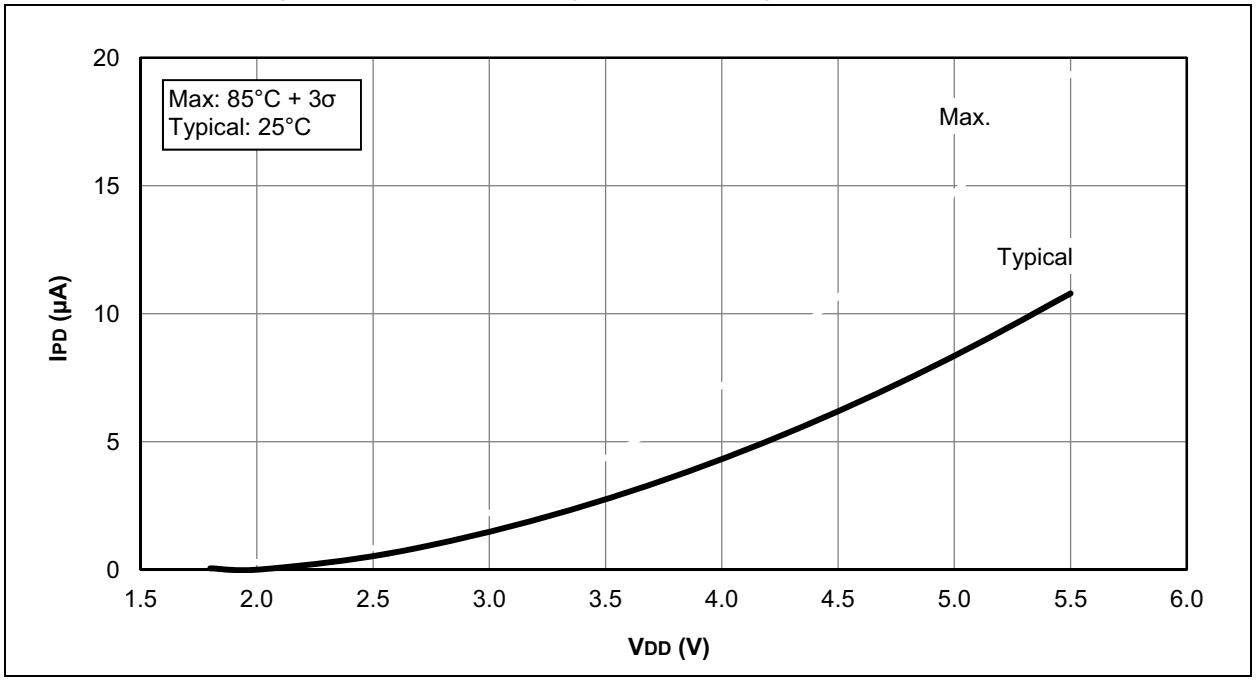


FIGURE 23-25: IPD, TIMER1 OSCILLATOR, FOSC = 32 kHz, PIC16F753 ONLY



PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-	X	/XX	XXX
Device	Tape and Reel Option		Temperature Range	Package	Pattern

Device:	PIC16F753 PIC16HV753	
Tape and Reel Option:	Blank T	= Standard packaging (tube or tray) = Tape and Reel(1)
Temperature Range:	I E	= -40°C to +85°C (Industrial) = -40°C to +125°C (Extended)
Package:	P SL ST ML	= 14-lead Plastic Dual In-line (PDIP) = 14-lead Plastic Small Outline (3.90 mm) (SOIC) = 14-lead Plastic Thin Shrink Small Outline (4.4 mm) (TSSOP) = 16-lead Plastic Quad Flat, No Lead Package (4x4x0.9 mm) (QFN)
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC16F753-I/ML301
Tape and Reel,
Industrial temperature,
QFN 4x43 package,
QTP pattern #301

b) PIC16F753-E/P
Extended temperature
PDIP package

c) PIC16F753-E/SL
Extended temperature,
SOIC package

d) PIC16HV753-E/ST
Extended temperature,
TSSOP 4.4 mm package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.