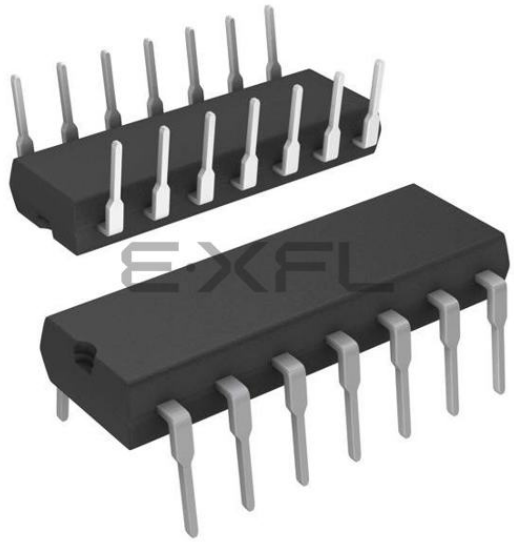

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 8x10b; D/A 1x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	14-DIP (0.300", 7.62mm)
Supplier Device Package	14-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16hv753-i-p

TABLE 1-1: PIC16F753/HV753 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN0+/DACOUT/ FVROUT/ICSPDAT	RA0	TTL	HP	General purpose I/O with IOC and WPU.
	AN0	AN	—	A/D Channel 0 input.
	C1IN0+	AN	—	Comparator C1 positive input.
	DACOUT	—	AN	DAC unbuffered Voltage Reference output.
	FVROUT	—	AN	DAC/FVR buffered Voltage Reference output.
	ICSPDAT	ST	HP	Serial Programming Data I/O.
RA1/AN1/C1IN0-/C2IN0-/ VREF+/FVRIN/ICSPCLK	RA1	TTL	CMOS	General purpose I/O with IOC and WPU.
	AN1	AN	—	A/D Channel 1 input.
	C1IN0-	AN	—	Comparator C1 negative input.
	C2IN0-	AN	—	Comparator C2 negative input.
	VREF+	AN	—	A/D Positive Voltage Reference input.
	FVRIN	AN	—	Voltage reference input.
	ICSPCLK	ST	—	Serial Programming Clock.
RA2/AN2/INT/C1OUT/ T0CKI/COG1FLT	RA2	ST	HP	General purpose I/O with IOC and WPU.
	AN2	AN	—	A/D Channel 2 input.
	INT	ST	—	External interrupt.
	C1OUT	—	HP	Comparator C1 output.
	T0CKI	ST	—	Timer0 clock input.
	COG1FLT	ST	—	COG auto-shutdown fault input.
RA3(1)/T1G(3)/VPP/$\overline{\text{MCLR}}$(4)	RA3	TTL	—	General purpose input with WPU.
	T1G	ST	—	Timer1 Gate input.
	VPP	HV	—	Programming voltage.
	$\overline{\text{MCLR}}$	ST	—	Master Clear w/internal pull-up.
RA4/AN3/T1G(2)/CLKOUT	RA4	TTL	CMOS	General purpose I/O with IOC and WPU.
	AN3	AN	—	A/D Channel 3 input.
	T1G	ST	—	Timer1 Gate input.
	CLKOUT	—	CMOS	FOSC/4 output.
RA5/T1CKI/COG1OUT0(3)/ C2IN1-/CLKIN	RA5	TTL	CMOS	General purpose I/O with IOC and WPU.
	T1CKI	ST	—	Timer1 clock input.
	CLKIN	ST	—	External Clock input (EC mode).
RC0/AN4/OPA1IN+/C2IN0+	RC0	TTL	CMOS	General purpose I/O with IOC and WPU.
	AN4	AN	—	A/D Channel 4 input.
	OPA1IN+	AN	—	Op amp positive input.
	C2IN0+	AN	—	Comparator C2 positive input.
RC1/AN5/OPA1IN-/C1IN1-/ C2IN1-	RC1	TTL	CMOS	General purpose I/O with IOC and WPU.
	AN5	AN	—	A/D Channel 5 input.
	OPA1IN-	AN	—	Op amp negative input.
	C1IN1-	AN	—	Comparator C1 negative input.
	C2IN1-	AN	—	Comparator C2 negative input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels
HP = High Power HV = High Voltage
* Alternate pin function.

Note 1: Input only.
2: Default pin function via the APFCON register.
3: Alternate pin function via the APFCON register.
4: RA3 pull-up is enabled when pin is configured as $\overline{\text{MCLR}}$ in Configuration Word.

TABLE 1-1: PIC16F753/HV753 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC2/AN6/SLPCIN/ OPA1OUT/C1IN2-/C2IN2-	RC2	TTL	CMOS	General purpose I/O with IOC and WPU.
	AN6	AN	—	A/D Channel 6 input.
	OPA1OUT	AN	HP	Op amp output.
	C1IN2-	AN	—	Comparator C1 negative input.
	C2IN2-	AN	—	Comparator C2 negative input.
RC3/AN7/C1IN3-/C2IN3-	RC3	TTL	CMOS	General purpose I/O with IOC and WPU.
	AN7	AN	—	A/D Channel 7 input.
	C1IN3-	AN	—	Comparator C1 negative input.
	C2IN3-	AN	—	Comparator C2 negative input.
RC4/COG1OUT1/C2OUT	RC4	TTL	CMOS	General purpose I/O with IOC and WPU.
	COG1OUT1	—	CMOS	COG output Channel 1.
	C2OUT	—	HP	Comparator C2 output.
RC5/COG1OUT0/CCP1	RC5	TTL	CMOS	General purpose I/O with IOC and WPU.
	COG1OUT0	—	CMOS	COG output Channel 0.
	CCP1	—	HP	Capture/Compare/PWM 1.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels
HP = High Power HV = High Voltage
* Alternate pin function.

Note 1: Input only.
2: Default pin function via the APFCON register.
3: Alternate pin function via the APFCON register.
4: RA3 pull-up is enabled when pin is configured as $\overline{\text{MCLR}}$ in Configuration Word.

TABLE 2-3: PIC16F753/HV753 SPECIAL REGISTERS SUMMARY BANK 2

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR	Value on all other Resets
Bank 2											
100h	INDF	INDF<7:0>								xxxx xxxx	xxxx xxxx
101h	TMR0	TMR0<7:0>								xxxx xxxx	uuuu uuuu
102h	PCL	PCL<7:0>								0000 0000	0000 0000
103h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
104h	FSR	FSR<7:0>								xxxx xxxx	uuuu uuuu
105h	LATA	—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0	--xx -xxx	--uu -uuu
106h	—	Unimplemented								—	—
107h	LATC	—	—	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	--xx xxxx	--uu uuuu
108h	IOCAN	—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	--00 0000	--00 0000
109h	IOCCN	—	—	IOCCN5	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0	--00 0000	--00 0000
10Ah	PCLATH	—	—	—	PCLATH<4:0>					---0 0000	---0 0000
10Bh	INTCON	GIE	PEIE	T0IE	INTE	IOCIE	T0IF	INTF	IOCIF	0000 0000	0000 0000
10Ch	WPUA	—	—	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	--11 1111	--11 1111
10Dh	WPUC	—	—	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	--11 1111	--11 1111
10Eh	SLRCONC	—	—	SLRC5	SLRC4	—	—	—	—	--00 ----	--00 ----
10Fh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$	---- --qq	---- --uu
110h	TMR2	TMR2<7:0>								0000 0000	0000 0000
111h	PR2	PR2<7:0>								1111 1111	1111 1111
112h	T2CON	—	T2OUTPS<3:0>				TMR2ON	T2CKPS<1:0>		-000 0000	-000 0000
113h	HLTMR1	Holding Register for the 8-bit Hardware Limit Timer1 Count								0000 0000	0000 0000
114h	HLTPR1	HLTMR1 Module Period Register								1111 1111	1111 1111
115h	HLT1CON0	—	H1OUTPS<3:0>				H1ON	H1CKPS<1:0>		-000 0000	-000 0000
116h	HLT1CON1	H1FES	H1RES	—	H1ERS<2:0>			H1FEREN	H1REREN	11-0 0000	11-0 0000
117h	HLTMR2	Holding Register for the 8-bit Hardware Limit Timer2 Count								0000 0000	0000 0000
118h	HLTPR2	HLTMR2 Module Period Register								1111 1111	1111 1111
119h	HLT2CON0	—	H2OUTPS<3:0>				H2ON	H2CKPS<1:0>		-000 0000	-000 0000
11Ah	HLT2CON1	H2FES	H2RES	—	H2ERS<2:0>			H2FEREN	H2REREN	11-0 0000	11-0 0000
11Bh	—	Unimplemented								—	—
11Ch	—	Unimplemented								—	—
11Dh	—	Unimplemented								—	—
11Eh	SLPCCON0	SC1EN	—	—	SC1POL	SC1TSS<1:0>		—	SC1INS	0-00 00-0	0-00 00-0
11Fh	SLPCCON1	—	—	—	SC1RNG	SC1ISET<3:0>				---0 0000	---0 0000

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition shaded = unimplemented.

2.3.5 PIE2 REGISTER

The PIE2 register contains the Peripheral Interrupt Enable bits, as shown in Register 2-5.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 2-5: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 1

U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0
—	—	C2IE	C1IE	—	COG1IE	—	CCP1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **C2IE:** Comparator 2 Interrupt Enable bit
1 = Enables the Comparator 2 interrupt
0 = Disables the Comparator 2 interrupt

bit 4 **C1IE:** Comparator 1 Interrupt Enable bit
1 = Enables the Comparator 1 interrupt
0 = Disables the Comparator 1 interrupt

bit 3 **Unimplemented:** Read as '0'

bit 2 **COG1IE:** COG 1 Interrupt Flag bit
1 = COG1 interrupt enabled
0 = COG1 interrupt disabled

bit 1 **Unimplemented:** Read as '0'

bit 0 **CCP1IE:** CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

3.3 Register Definitions: Flash Program Memory Control

REGISTER 3-1: PMDATL: PROGRAM MEMORY DATA LOW BYTE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PMDATL<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PMDATL<7:0>**: Eight Least Significant Data bits to Write or Read from Program Memory

REGISTER 3-2: PMADRL: PROGRAM MEMORY ADDRESS LOW BYTE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PMADRL<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PMADRL<7:0>**: Eight Least Significant Address bits for Program Memory Read/Write Operation

REGISTER 3-3: PMDATH: PROGRAM MEMORY DATA HIGH BYTE REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	PMDATH<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **PMDATH<5:0>**: Six Most Significant Data bits from Program Memory

REGISTER 3-4: PMADRH: PROGRAM MEMORY ADDRESS HIGH BYTE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	PMADRH<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **PMADRH<1:0>**: Specifies the two Most Significant Address bits or High bits for Program Memory Reads.

5.0 I/O PORTS

Depending on the device selected and peripherals enabled, there are up to two ports available. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Each port has three standard registers for its operation.

These registers are:

- TRISx registers (data direction)
- PORTx registers (reads the levels on the pins of the device)
- LATx registers (output latch)

Some ports may have one or more of the following additional registers. These registers are:

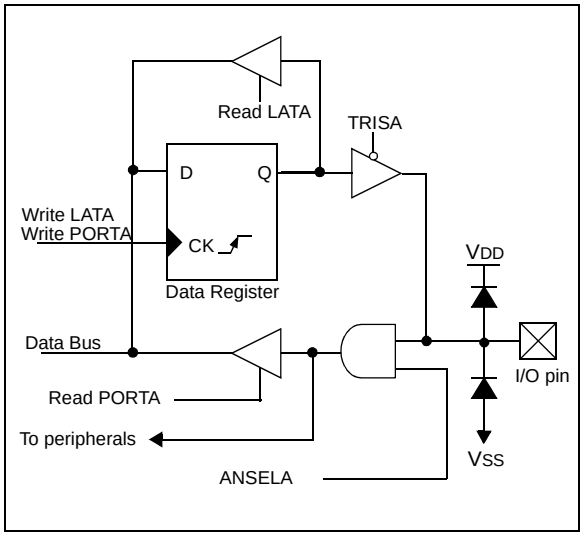
- ANSELx (analog select)
- WPUx (weak pull-up)
- SLRCONx registers (slew rate)

The Data Latch (LATx registers) is useful for read-modify-write operations on the values that the I/O pins are driving.

A write operation to the LATx register has the same affect as a write to the corresponding PORTx register. A read of the LATx register reads the values held in the I/O PORT latches, while a read of the PORTx register reads the actual I/O pin value.

Ports with analog functions also have an ANSELx register which can disable the digital input and save power. A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 5-1.

FIGURE 5-1: GENERIC I/O PORTA OPERATION



EXAMPLE 5-1: INITIALIZING PORTA

```
; This code example illustrates
; initializing the PORTA register. The
; other ports are initialized in the same
; manner.

BANKSEL  PORTA        ;
CLRF     PORTA        ;Init PORTA
BANKSEL  LATA         ;Data Latch
CLRF     LATA         ;
BANKSEL  ANSELA       ;
CLRF     ANSELA       ;digital I/O
BANKSEL  TRISA        ;
MOVLW    B'00111000'  ;Set RA<5:3> as inputs
MOVWF    TRISA        ;and set RA<2:0> as
                      ;outputs
```

5.4 Additional Pin Functions

Every PORTA pin on the PIC16F753 has an interrupt-on-change option and a weak pull-up option. The next three sections describe these functions.

5.4.1 ANSELA REGISTER

The ANSELA register (Register 5-5) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELA bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

5.4.2 WEAK PULL-UPS

Each of the PORTA pins, except RA3, has an individually configurable internal weak pull-up. Control bits WPUx enable or disable each pull-up. Refer to Register 5-6. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the $\overline{\text{RAPU}}$ bit of the OPTION_REG register. A weak pull-up is automatically enabled for RA3 when configured as $\overline{\text{MCLR}}$ and disabled when RA3 is an I/O. There is no software control of the $\overline{\text{MCLR}}$ pull-up.

5.4.3 INTERRUPT-ON-CHANGE

Each PORTA pin is individually configurable as an interrupt-on-change pin. Control bits IOCA enable or disable the interrupt function for each pin. Refer to Register 5-7. The interrupt-on-change is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of PORTA. The 'mismatch' outputs of the last read are OR'd together to set the PORTA Change Interrupt Flag bit (IOCIF) in the INTCON register (Register 2-3).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, clears the interrupt by:

a) Any read of PORTA AND Clear flag bit IOCIF. This will end the mismatch condition;

   OR

b) Any write of PORTA AND Clear flag bit IOCIF will end the mismatch condition;

A mismatch condition will continue to set flag bit IOCIF. Reading PORTA will end the mismatch condition and allow flag bit IOCIF to be cleared. The latch holding the last read value is not affected by a $\overline{\text{MCLR}}$ nor BOR Reset. After these Resets, the IOCIF flag will continue to be set if a mismatch is present.

Note:	If a change on the I/O pin should occur when any PORTA operation is being executed, then the IOCIF interrupt flag may not get set.

REGISTER 5-15: WPUC: WEAK PULL-UP PORTC REGISTER

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **WPUC<5:0>:** Weak Pull-up Control bits**(1,2,3)**
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: Global $\overline{\text{RAPU}}$ must be enabled for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is in Output mode (TRISC = 0).
3: The RC3 pull-up is enabled when configured as $\overline{\text{MCLR}}$ in the Configuration Word, otherwise it is disabled as an input and reads as ‘0’.

REGISTER 5-16: IOCCP: INTERRUPT-ON-CHANGE POSITIVE EDGE REGISTER

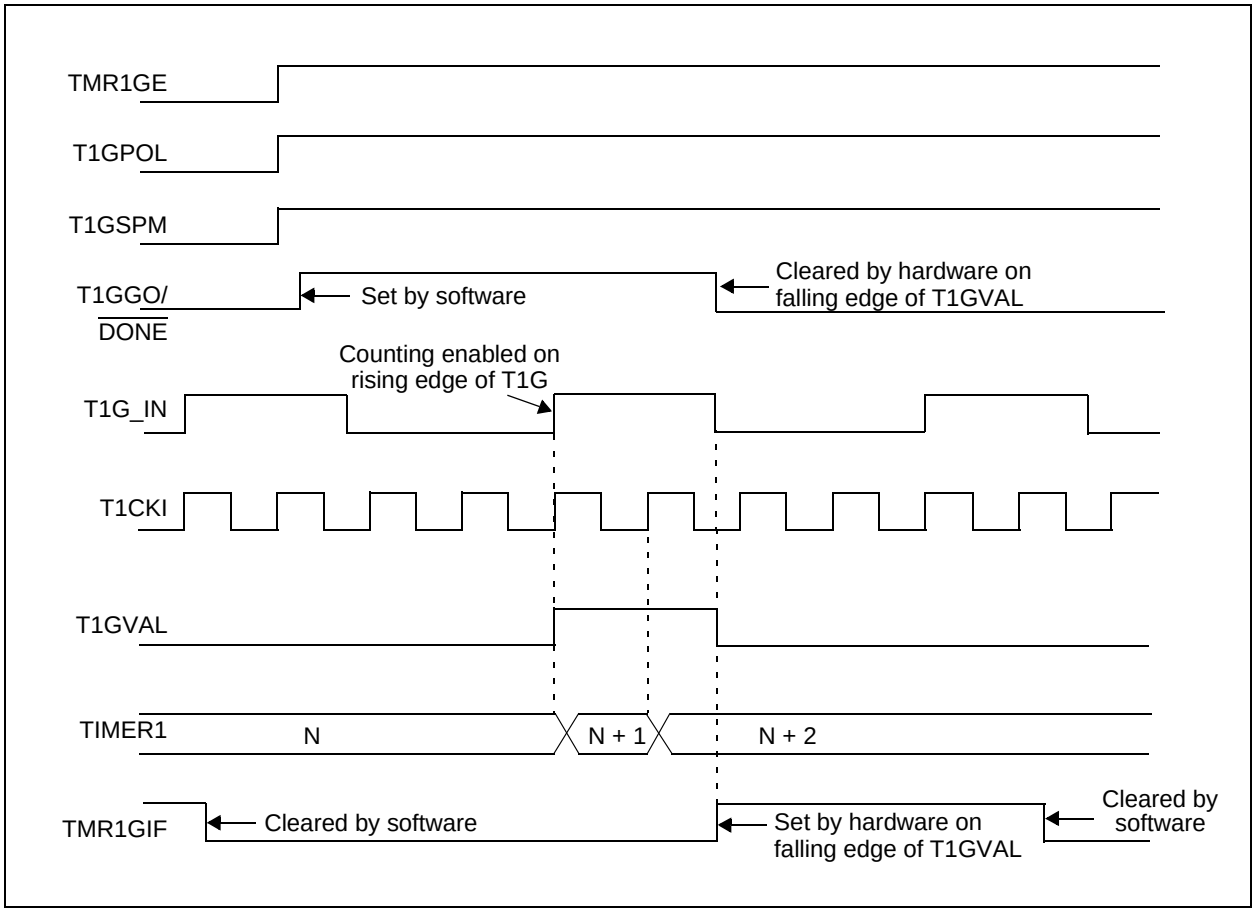
U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IOCCP5	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-0 **IOCCP<5:0>:** Interrupt-on-Change Positive Edge Enable bits
1 = Interrupt-on-Change enabled on the pin for a positive going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin.

FIGURE 7-5: TIMER1 GATE SINGLE-PULSE MODE



12.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESL and ADRESH).

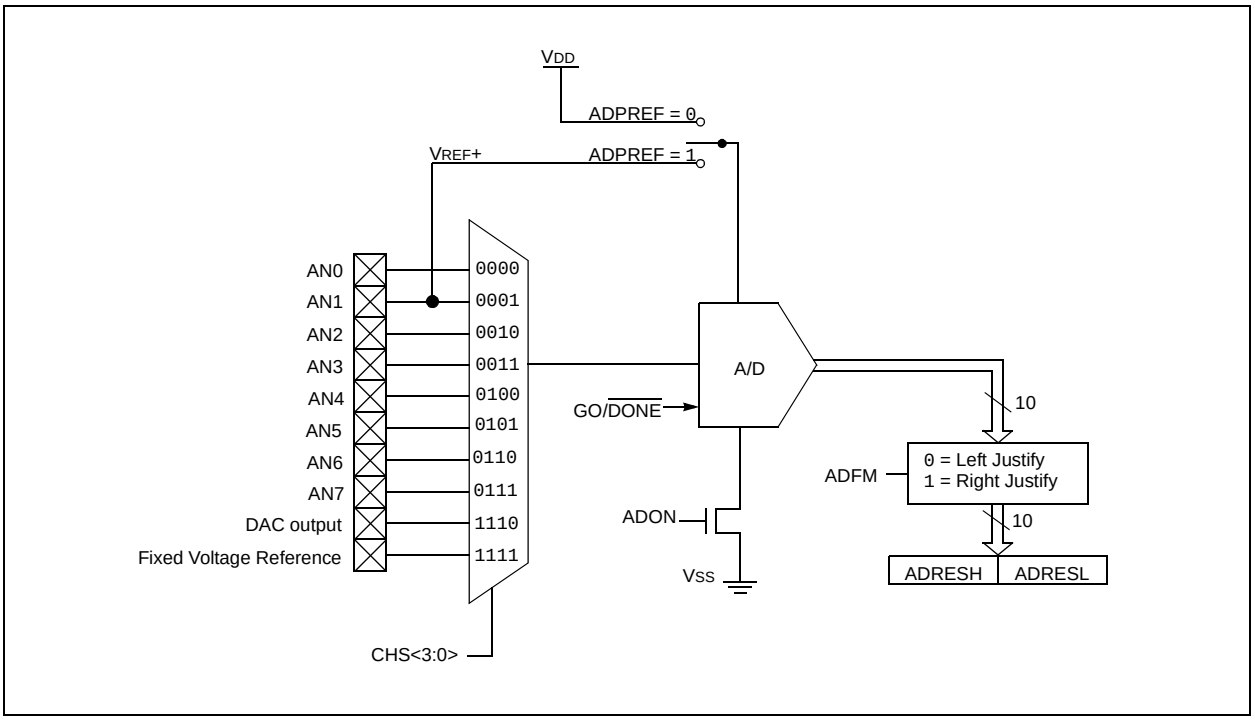
The ADC voltage reference is software selectable to either VDD or a voltage applied to the external reference pins.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake up the device from Sleep.

Figure 12-1 shows the block diagram of the ADC.

Note:	The ADRESL and ADRESH registers are read-only.

FIGURE 12-1: ADC BLOCK DIAGRAM

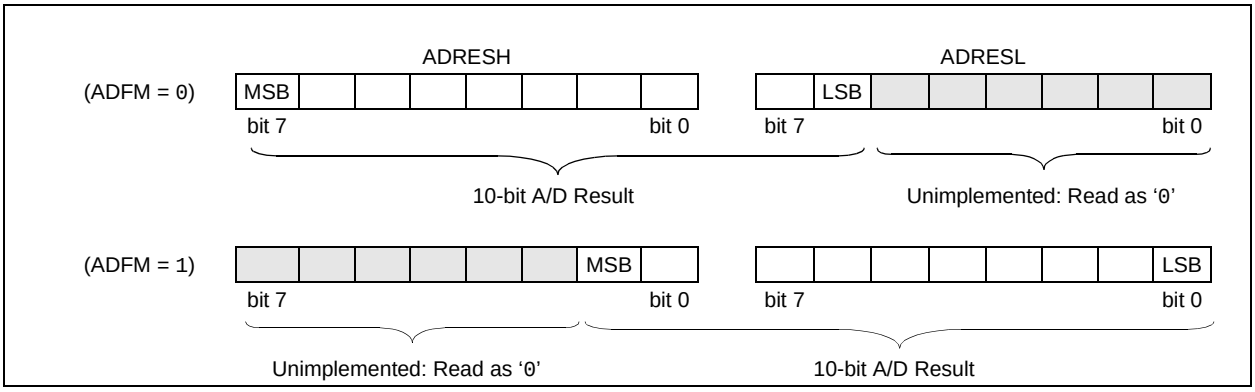


12.1.6 RESULT FORMATTING

The 10-bit A/D conversion result can be supplied in two formats, left justified or right justified. The ADFM bit of the ADCON0 register controls the output format.

Figure 12-4 shows the two output formats.

FIGURE 12-3: 10-BIT A/D CONVERSION RESULT FORMAT



12.2 ADC Operation

12.2.1 STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'. Setting the GO/$\overline{\text{DONE}}$ bit of the ADCON0 register to a '1' will start the Analog-to-Digital conversion.

Note:	The GO/$\overline{\text{DONE}}$ bit should not be set in the same instruction that turns on the ADC. Refer to **Section 12.2.6 "A/D Conversion Procedure"**.

12.2.2 COMPLETION OF A CONVERSION

When the conversion is complete, the ADC module will:

- Clear the GO/$\overline{\text{DONE}}$ bit
- Set the ADIF flag bit
- Update the ADRESH:ADRESL registers with new conversion result

12.2.3 TERMINATING A CONVERSION

If a conversion must be terminated before completion, the GO/$\overline{\text{DONE}}$ bit can be cleared in software. The ADRESH:ADRESL registers will not be updated with the partially complete Analog-to-Digital conversion sample. Instead, the ADRESH:ADRESL register pair will retain the value of the previous conversion. Additionally, a 2 TAD delay is required before another acquisition can be initiated. Following this delay, an input acquisition is automatically started on the selected channel.

Note:	A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

12.2.4 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC clock source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than FRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

12.2.5 SPECIAL EVENT TRIGGER

The CCP Special Event Trigger allows periodic ADC measurements without software intervention. When this trigger occurs, the GO/$\overline{\text{DONE}}$ bit is set by hardware and the Timer1 counter resets to zero.

Using the Special Event Trigger does not assure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met.

See **Section 10.0 "Capture/Compare/PWM Modules"** for more information.

TABLE 12-2: SUMMARY OF ASSOCIATED ADC REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	ADFM	—	CHS<3:0>				GO/$\overline{\text{DONE}}$	ADON	109
ADCON1	—	ADCS<2:0>			—	—	—	ADPREF1	110
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	44
ADRESH(2)	Most Significant eight bits of the left shifted A/D result or two bits of the right shifted result								111*
ADRESL(2)	Least Significant two bits of the left shifted result or eight bits of the right shifted result								109*
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	43
INTCON	GIE	PEIE	T0IE	INTE	IOCIE	T0IF	INTF	IOCIF	17
PIE1	TMR1GIE	ADIE	—	—	HLTMR2IE	HLTMR1IE	TMR2IE	TMR1IE	18
PIR1	TMR1GIF	ADIF	—	—	HLTMR2IF	HLTMR1IF	TMR2IF	TMR1IF	20
TRISA	—	—	TRISA5	TRISA4	TRISA3(1)	TRISA2	TRISA1	TRISA0	43

Legend: x = unknown, u = unchanged, – = unimplemented read as '0'. Shaded cells are not used for ADC module.

* Page provides register information.

Note 1: TRISA3 always reads '1'.

2: Read-only register.

15.0 COMPARATOR MODULE

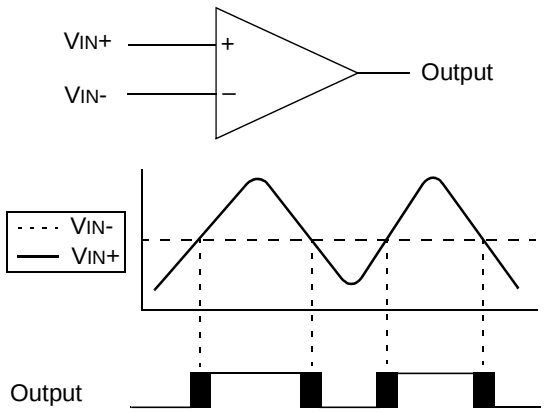
Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed-signal building blocks because they provide analog functionality independent of program execution. The analog comparator module includes the following features:

- Independent comparator control
- Programmable input selection
- Comparator output is available internally/externally
- Programmable output polarity
- Interrupt-on-change
- Wake-up from Sleep
- Programmable Speed/Power optimization
- PWM shutdown
- Programmable and Fixed Voltage Reference

15.1 Comparator Overview

A single comparator is shown in Figure 15-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

FIGURE 15-1: SINGLE COMPARATOR



Note: The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.

19.5 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and STATUS registers). This must be implemented in software.

Temporary holding registers W_TEMP and STATUS_TEMP should be placed in the last 16 bytes of GPR (see Figure 2-2). These 16 locations are common to all banks and do not require banking. This makes context save and restore operations simpler. The code shown in Example 19-1 can be used to:

- Store the W register
- Store the STATUS register
- Execute the ISR code
- Restore the Status (and Bank Select Bit register)
- Restore the W register

Note:	The PIC16F753/HV753 does not require saving the PCLATH. However, if computed GOTOs are used in both the ISR and the main code, the PCLATH must be saved and restored in the ISR.

EXAMPLE 19-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF   W_TEMP              ;Copy W to TEMP register
SWAPF   STATUS,W            ;Swap status to be saved into W
                            ;Swaps are used because they do not affect the status bits
MOVWF   STATUS_TEMP         ;Save status to bank zero STATUS_TEMP register
:
:(ISR)                      ;Insert user code here
:
SWAPF   STATUS_TEMP,W       ;Swap STATUS_TEMP register into W
                            ;(sets bank to original state)
MOVWF   STATUS              ;Move W into STATUS register
SWAPF   W_TEMP,F            ;Swap W_TEMP
SWAPF   W_TEMP,W            ;Swap W_TEMP into W
```

19.6 Watchdog Timer (WDT)

The Watchdog Timer is a free running timer, using LFINTOSC oscillator as its clock source. The WDT is enabled by setting the WDTE bit of the Configuration Word (default setting). When WDTE is set, the LFINTOSC will always be enabled to provide a clock source to the WDT module.

During normal operation, a WDT time-out generates a device Reset. If the device is in Sleep mode, a WDT time-out causes the device to wake-up and continue with normal operation.

The WDT can be permanently disabled by programming the Configuration bit, WDTE, as clear (**Section 19.1 “Configuration Bits”**).

19.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms (with no prescaler). The time-out periods vary with temperature, V_{DD} and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device Reset.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

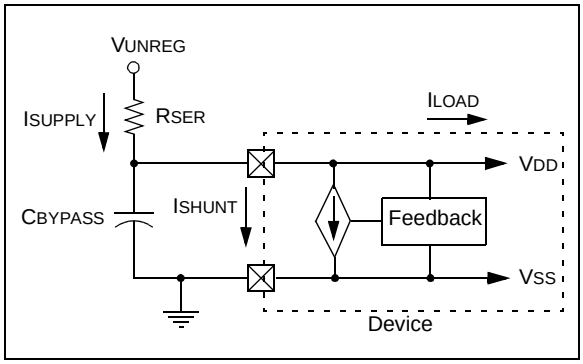
20.0 SHUNT REGULATOR (PIC16HV753 ONLY)

The PIC16HV753 devices include a permanent internal 5 volt (nominal) shunt regulator in parallel with the VDD pin. This eliminates the need for an external voltage regulator in systems sourced by an unregulated supply. All external devices connected directly to the VDD pin will share the regulated supply voltage and contribute to the total VDD supply current (ILOAD).

20.1 Regulator Operation

A shunt regulator generates a specific supply voltage by creating a voltage drop across a pass resistor RSER. The voltage at the VDD pin of the microcontroller is monitored and compared to an internal voltage reference. The current through the resistor is then adjusted, based on the result of the comparison, to produce a voltage drop equal to the difference between the supply voltage VUNREG and the VDD of the microcontroller. See Figure 20-1 for voltage regulator schematic.

FIGURE 20-1: SHUNT REGULATOR



An external current limiting resistor, RSER, located between the unregulated supply, VUNREG, and the VDD pin, drops the difference in voltage between VUNREG and VDD. RSER must be between RMAX and RMIN as defined by Equation 20-1.

EQUATION 20-1: RSER LIMITING RESISTOR

$$R_{MAX} = \frac{(VU_{MIN} - 5V)}{1.05 \bullet (1\ mA + I_{LOAD})}$$

$$R_{MIN} = \frac{(VU_{MAX} - 5V)}{0.95 \bullet (50\ mA)}$$

Where:

RMAX = maximum value of RSER (ohms)

RMIN = minimum value of RSER (ohms)

VUMIN = minimum value of VUNREG

VUMAX = maximum value of VUNREG

VDD = regulated voltage (5V nominal)

ILOAD = maximum expected load current in mA including I/O pin currents and external circuits connected to VDD.

1.05 = compensation for +5% tolerance of RSER

0.95 = compensation for -5% tolerance of RSER

20.2 Regulator Considerations

The supply voltage VUNREG and load current are not constant. Therefore, the current range of the regulator is limited. Selecting a value for RSER must take these three factors into consideration.

Since the regulator uses the band gap voltage as the regulated voltage reference, this voltage reference is permanently enabled in the PIC16HV753 devices.

The shunt regulator will still consume current when below operating voltage range for the shunt regulator.

20.3 Design Considerations

For more information on using the shunt regulator and managing current load, see Application Note *AN1035*, *Designing with HV Microcontrollers* (DS01035).

22.1 Standard Operating Conditions

The standard operating conditions for any device are defined as:

Operating Voltage: $V_{DDMIN} \leq V_{DD} \leq V_{DDMAX}$
Operating Temperature: $T_{A\_MIN} \leq T_A \leq T_{A\_MAX}$

V_{DD} — Operating Supply Voltage(1)

PIC16F753

V_{DDMIN} ($F_{OSC} \leq 8$ MHz) ..... +2.0V
V_{DDMIN} (8 MHz < $F_{OSC} \leq 10$ MHz) ..... +3.0V
V_{DDMAX} (10 MHz < $F_{OSC} \leq 20$ MHz) ..... +5.5V

PIC16HV753

V_{DDMIN} ($F_{OSC} \leq 8$ MHz) ..... +2.0V
V_{DDMIN} (8 MHz < $F_{OSC} \leq 10$ MHz) ..... +3.0V
V_{DDMAX} (10 MHz < $F_{OSC} \leq 20$ MHz) ..... +5.0V

T_A — Operating Ambient Temperature Range

Industrial Temperature

T_{A_MIN} ..... -40°C
T_{A_MAX} ..... +85°C

Extended Temperature

T_{A_MIN} ..... -40°C
T_{A_MAX} ..... +125°C

Note 1: See Parameter D001, DS Characteristics: Supply Voltage.

TABLE 22-3: POWER-DOWN CURRENTS (I_{PD}) (CONTINUED)(1,2)

PIC16F753		Standard Operating Conditions (unless otherwise stated) Sleep mode						
PIC16HV753								
Param No.	Device Characteristics	Min.	Typ†	Max. 85°C	Max. 125°C	Units	Conditions	
							V_{DD}	Note
	Power-down Base Current (I_{PD})(2, 3)							
D025		—	0.10	0.41	3.51	µA	3.0	A/D Current(1), no conversion in progress
		—	0.12	0.55	4.41	µA	5.0	
D025		—	145	171	175	µA	3.0	
		—	185	226	231	µA	4.5	
D026		—	20	37	37	µA	2.0	DAC Current(1)
		—	30	46	46	µA	3.0	
		—	50	76	76	µA	5.0	
D026		—	85	155	155	µA	2.0	
		—	165	213	213	µA	3.0	
		—	215	284	284	µA	4.5	
D027		—	115	185	203	µA	2.0	FVR Current(1), FVRBUFEN = 1, FVROUT buffer enabled
		—	120	193	219	µA	3.0	
		—	125	196	224	µA	5.0	
D027		—	65	126	145	µA	2.0	
		—	136	171	182	µA	3.0	
		—	175	226	231	µA	4.5	
D028		—	1	2	4	µA	2.0	T1OSC Current, TMR1CS <1:0> = 11
		—	2	3	5	µA	3.0	
		—	9	20	21	µA	5.0	
D028		—	65	126	140	µA	2.0	
		—	136	172	180	µA	3.0	
		—	175	228	235	µA	4.5	
D029		—	140	258	265	µA	2.0	Op-Amp Current(1)
		—	155	326	340	µA	3.0	
		—	165	421	422	µA	5.0	
D029		—	140	260	265	µA	2.0	
		—	155	325	340	µA	3.0	
		—	165	400	410	µA	4.5	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral Δ current can be determined by subtracting the base I_{PD} current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{SS}.

3: Shunt regulator is always ON and always draws operating current.

TABLE 22-4: I/O PORTS

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
	VIL	**Input Low Voltage**					
		I/O PORT:					
D030		with TTL buffer	—	—	0.8	V	4.5V ≤ VDD ≤ 5.5V
D030A			—	—	0.15 VDD	V	2.0V ≤ VDD ≤ 4.5V
D031		with Schmitt Trigger buffer	—	—	0.2 VDD	V	2.0V ≤ VDD ≤ 5.5V
	VIH	**Input High Voltage**					
		I/O PORT:					
D040		with TTL buffer	2.0	—	—	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.25 VDD + 0.8	—	—	V	2.0V ≤ VDD ≤ 4.5V
D041		with Schmitt Trigger buffer	0.8 VDD	—	—	V	2.0V ≤ VDD ≤ 5.5V
D042		$\overline{MCLR}$	0.8 VDD	—	—	V	
	IIL	**Input Leakage Current(1)**					
D060		I/O ports	—	± 0.1	± 1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance, 85°C
D061		RA3/$\overline{MCLR}$(2)	—	± 0.7	± 5	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance, 85°C
D063			—	± 0.1	± 5	µA	EC Configuration
	IPUR	**Weak Pull-up Current(3)**					
D070*			50	250	400	µA	VDD = 5.0V, VPIN = VSS
	VOL	**Output Low Voltage**					
D080		I/O Ports (excluding RC4, RC5)	—	—	0.6	V	IOL = 7 mA, VDD = 4.5V -40°C ≤ TA ≤ +125°C IOL = 8.5 mA, VDD = 4.5V -40°C ≤ TA ≤ +85°C
		I/O Ports RC4 and RC5	—	—	0.6	V	IOL = 14 mA, VDD = 4.5V -40°C ≤ TA ≤ +125°C IOL = 17 mA, VDD = 4.5V -40°C ≤ TA ≤ +85°C
	VOH	**Output High Voltage**					
D090		I/O Ports (excluding RC4, RC5)	VDD-0.7	—	—	V	IOH = -2.5 mA, VDD = 4.5V -40°C ≤ TA ≤ +125°C IOH = -3 mA, VDD = 4.5V -40°C ≤ TA ≤ +85°C
		I/O Ports RC4 and RC5	VDD-0.7	—	—	V	IOH = -5 mA, VDD = 4.5V -40°C ≤ TA ≤ +125°C IOH = -6 mA, VDD = 4.5V -40°C ≤ TA ≤ +85°C

* These parameters are characterized but not tested.

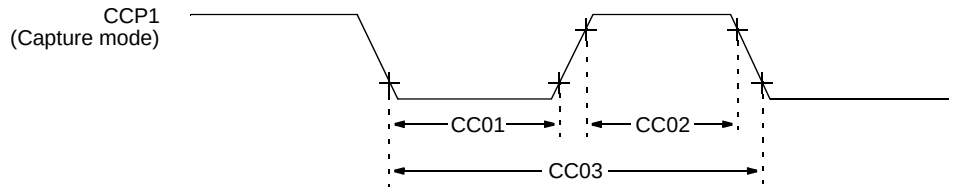
† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Negative current is defined as current sourced by the pin.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: This specification applies to all weak pull-up pins, including the weak pull-up found on RA3/$\overline{MCLR}$. When RA3/$\overline{MCLR}$ is configured as $\overline{MCLR}$ Reset pin, the weak pull-up is always enabled.

FIGURE 22-9: PIC16F753/HV753 CAPTURE/COMPARE/PWM TIMINGS (CCP)



Note: Refer to Figure 22-3 for load conditions.

TABLE 22-12: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP)

Standard Operating Conditions (unless otherwise stated)								
Param No.	**Sym.**	**Characteristic**		**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
CC01*	TccL	CCP1 Input Low Time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC02*	TccH	CCP1 Input High Time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC03*	TccP	CCP1 Input Period		$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 4 or 16)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 22-13: COMPARATOR SPECIFICATIONS(1)

Standard Operating Conditions (unless otherwise stated) VDD = 5.0V, -40°C ≤ TA ≤ +125°C							
Param No.	**Sym.**	**Characteristics**	**Min.**	**Typ†**	**Max.**	**Units**	**Comments**
CM01	VIOFF	Input Offset Voltage(3)	—	± 10 ± 10	± 20 ± 20	mV mV	CxSP = 1 CxSP = 0
CM02	VICM	Input Common Mode Voltage(2)	0	—	VDD – 1.5	V	
CM03	CMRR	Common Mode Rejection Ratio	—	55	—	dB	
CM04A*	TRT(2)	Response Time	—	55	70	ns	CxSP = 1
			—	65	100	ns	CxSP = 0
CM05*	TMC20V	Comparator Mode Change to Output Valid	—	—	10	µs	
CM06	CHYSTER	Comparator Hysteresis	—	20	50	mV	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

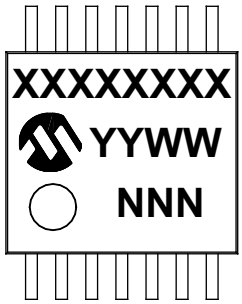
Note 1: See **Section 23.0 "DC and AC Characteristics Graphs and Charts"**and **Section 22.0 "Electrical Specifications"** for operating characterization.

2: Response time is measured with one comparator input at (VDD - 1.5V)/2 - 100 mV to (VDD - 1.5V)/2 + 20 mV. The other input is at (VDD -1.5V)/2.

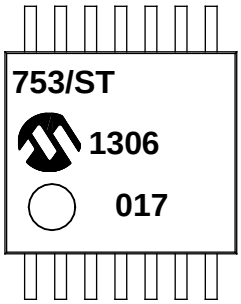
3: Input offset voltage is measured with one comparator input at (VDD - 1.5V)/2.

24.2 Package Marking Information

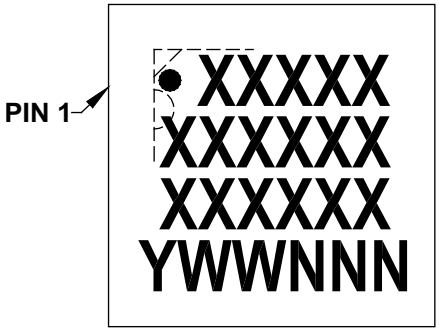
14-Lead TSSOP (4.4 mm)



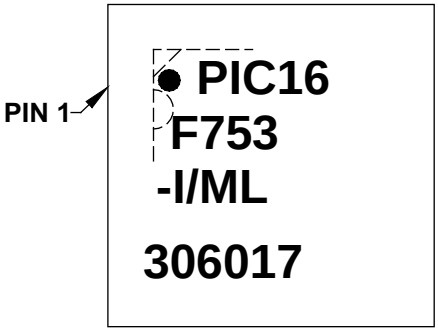
Example



16-Lead QFN (4x4x0.9 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.