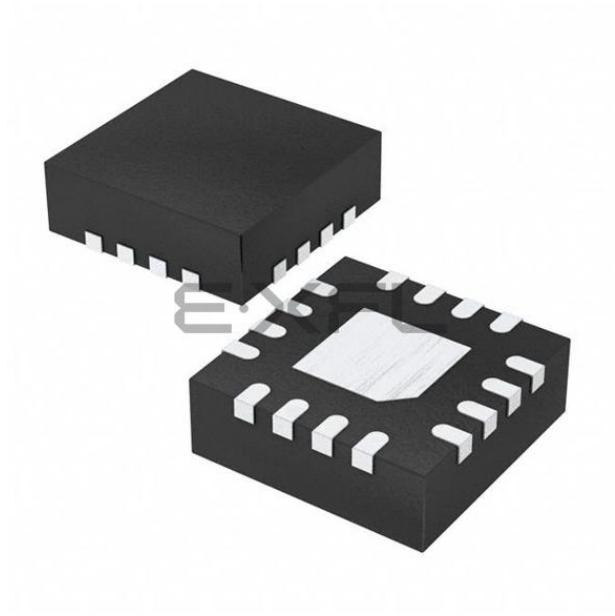

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 8x10b; D/A 1x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VQFN Exposed Pad
Supplier Device Package	16-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16hv753t-i-ml

- Complementary Output Generator (COG):
  - Complementary Waveforms from selectable sources
  - Two I/O (50 mA) for direct MOSFET drive
  - Rising and/or Falling edge dead-band control
  - Phase control, Blanking control
  - Auto-shutdown
  - Slope Compensation Circuit for use with SMPS power supplies

TABLE 1: PIC16F753/HV753 FAMILY TYPES

Device	Data Sheet Index	Program Memory Flash (words)	Self-Read/Write Flash Memory	Data SRAM (bytes)	I/Os(2)	10-bit ADC (ch)	Comparators	Timers (8/16-bit)	CCP	Complementary Output Generator (COG)	DAC	Op Amp	Shunt Regulator	Debug(1)	XLP
PIC12F752	(1)	1K	Y	64	6	4	2	3/1	1	Y	5-bit	N	N	H	Y
PIC12HV752	(1)	1K	Y	64	6	4	2	3/1	1	Y	5-bit	N	Y	H	Y
PIC16F753	(2)	2K	Y	128	12	8	2	3/1	1	Y	9-bit	Y	N	I/H	Y
PIC16HV753	(2)	2K	Y	128	12	8	2	3/1	1	Y	9-bit	Y	Y	I/H	Y

Note 1: I - Debugging, Integrated on Chip; H - Debugging, Requires Debug Header.

2: One pin is input-only.

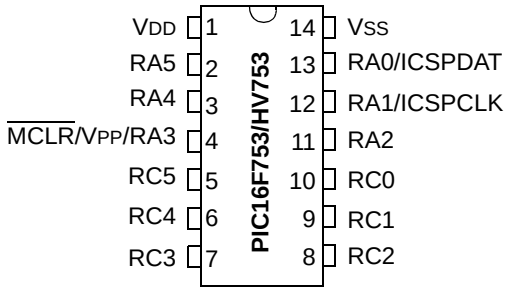
Data Sheet Index: (Unshaded devices are described in this document.)

1: DS40001576 PIC12F752/HV752 Data Sheet, 8-Pin Flash-Based, 8-Bit CMOS Microcontrollers.

2: DS40001709 PIC16F753/HV753 Data Sheet, 14/16-Pin Flash-based, 8-Bit CMOS Microcontrollers.

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

FIGURE 1: 14-PIN PDIP, SOIC, TSSOP DIAGRAM



Note: See Table 2 for location of all peripheral functions.

REGISTER 3-5: PMCON1: PROGRAM MEMORY CONTROL 1 REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/S/HC-0/0	R/S/HC-0/0
—	—	—	—	—	WREN	WR	RD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
S = Bit can only be set	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HC = Bit is cleared by hardware

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2 **WREN:** Program/Erase Enable bit
- 1 = Allows program/erase cycles
- 0 = Inhibits programming/erasing of program Flash

bit 1 **WR:** Write Control bit
- 1 = Initiates a program Flash program/erase operation
  The operation is self-timed and the bit is cleared by hardware once operation is complete.
  The WR bit can only be set (not cleared) in software.
- 0 = Program/erase operation to the Flash is complete and inactive

bit 0 **RD:** Read Control bit
- 1 = Initiates a program Flash read. Read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software.
- 0 = Does not initiate a program Flash read

REGISTER 3-6: PMCON2: PROGRAM MEMORY CONTROL 2 REGISTER

W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0
Program Memory Control Register 2							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
S = Bit can only be set	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **Flash Memory Unlock Pattern bits:**
To unlock writes, a 55h must be written first, followed by an AAh, before setting the WR bit of the PMCON1 register. The value written to this register is used to unlock the writes. There are specific timing requirements on these writes.

FIGURE 7-3: TIMER1 GATE COUNT ENABLE MODE

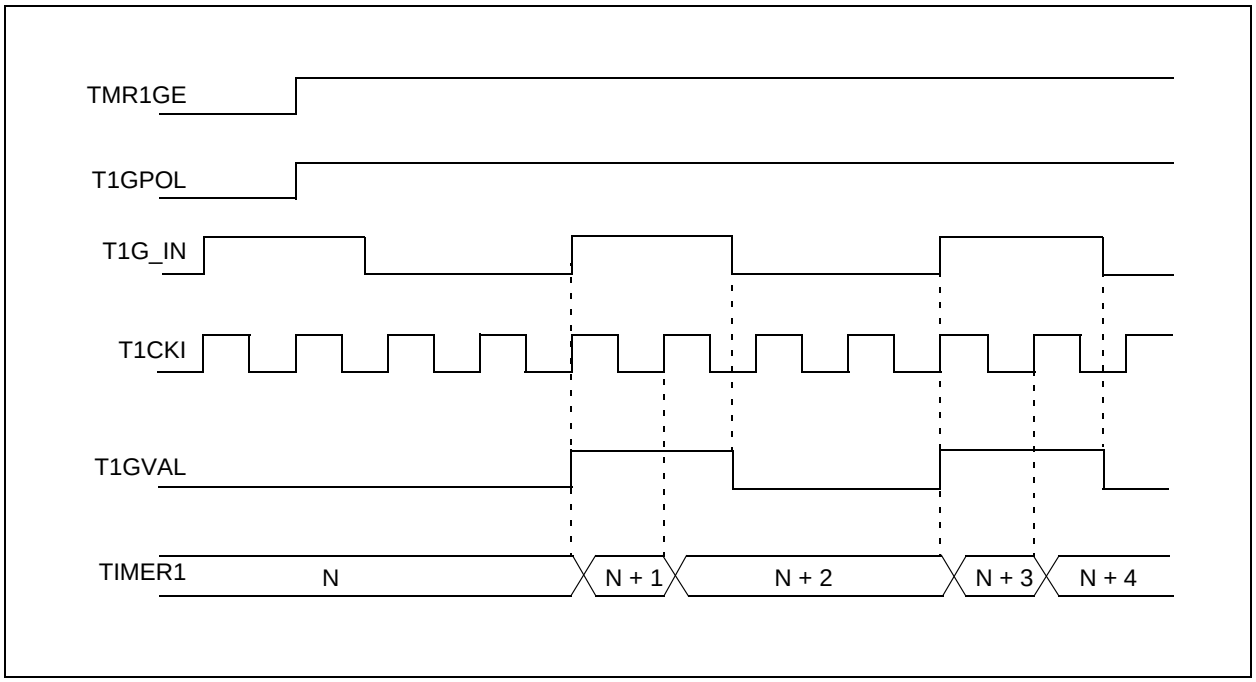
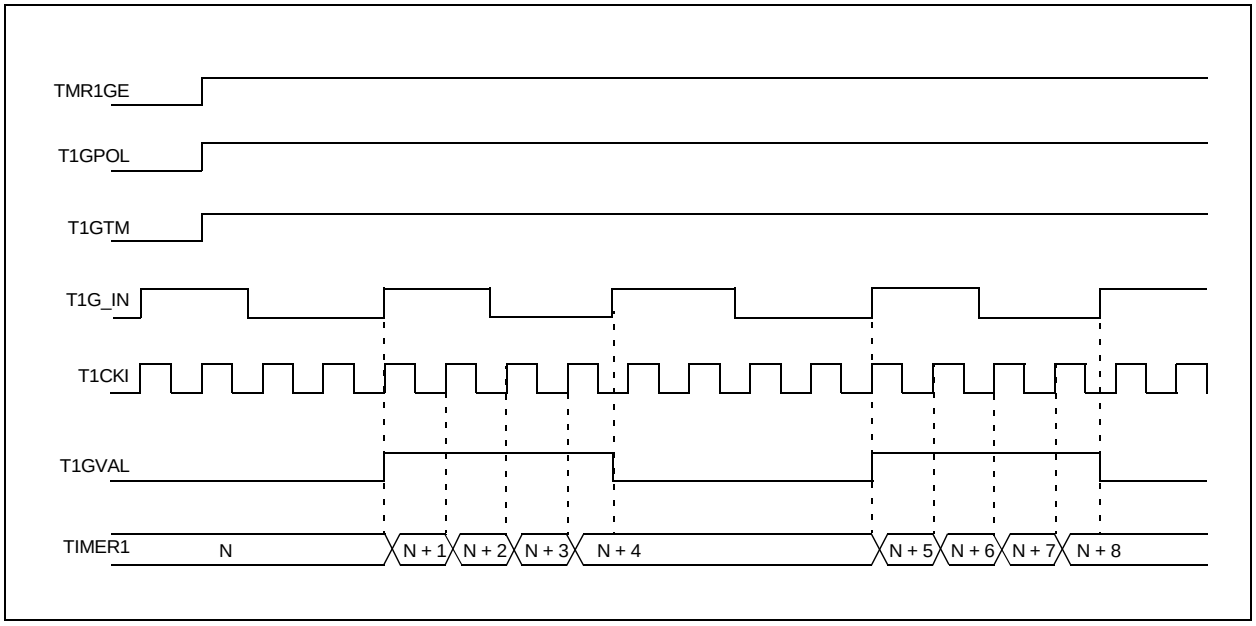


FIGURE 7-4: TIMER1 GATE TOGGLE MODE



REGISTER 11-2: COGxCON1: COG CONTROL REGISTER 1

R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
GxRDBTS	GxFDBTS	—	—	—	—	GxCS<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7 **GxRDBTS:** COGx Rising Event Dead-band Timing Source Select bit
1 = Delay chain and COGxDBR are used for dead-band timing generation
0 = COGx_clk and COGxDBR are used for dead-band timing generation

bit 6 **GxFDBTS:** COGx Falling Event Dead-band Timing Source Select bit
1 = Delay chain and COGxDF are used for dead-band timing generation
0 = COGx_clk and COGxDBF are used for dead-band timing generation

bit 5-2 **Unimplemented:** Read as ‘0’

bit 1-0 **GxCS<1:0>:** COGx Clock Source Select bits
11 = Reserved
10 = HFINTOSC (stays active during Sleep)
01 = FOSC/4
00 = FOSC

12.2.6 A/D CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure Port:
   - Disable pin output driver (See TRIS register)
   - Configure pin as analog
2. Configure the ADC module:
   - Select ADC conversion clock
   - Configure voltage reference
   - Select ADC input channel
   - Select result format
   - Turn on ADC module
3. Configure ADC interrupt (optional):
   - Clear ADC interrupt flag
   - Enable ADC interrupt
   - Enable peripheral interrupt
   - Enable global interrupt**(1)**
4. Wait the required acquisition time**(2)**.
5. Start conversion by setting the GO/$\overline{\text{DONE}}$ bit.
6. Wait for ADC conversion to complete by one of the following:
   - Polling the GO/$\overline{\text{DONE}}$ bit
   - Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC Result
8. Clear the ADC interrupt flag (required if interrupt is enabled).

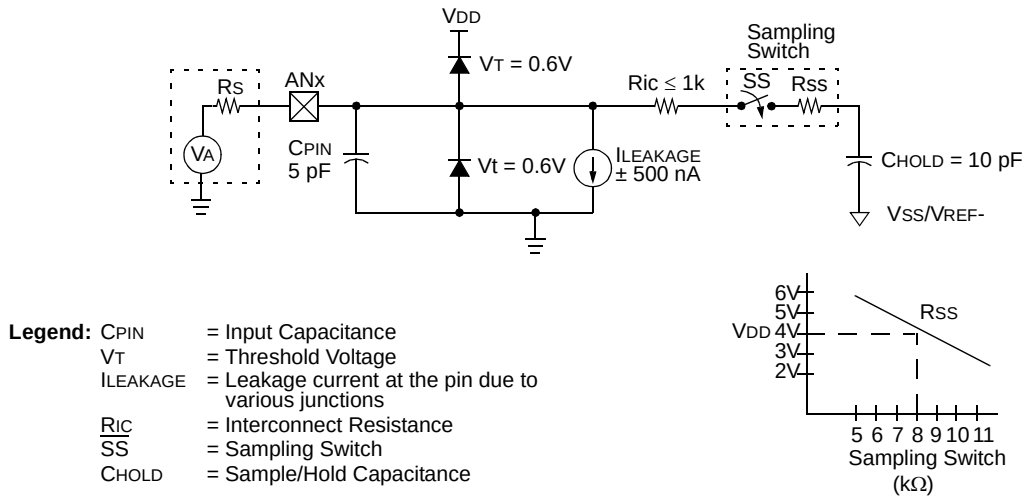
Note 1: The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

2: See **Section 12.4 "A/D Acquisition Requirements"**.

EXAMPLE 12-1: A/D CONVERSION

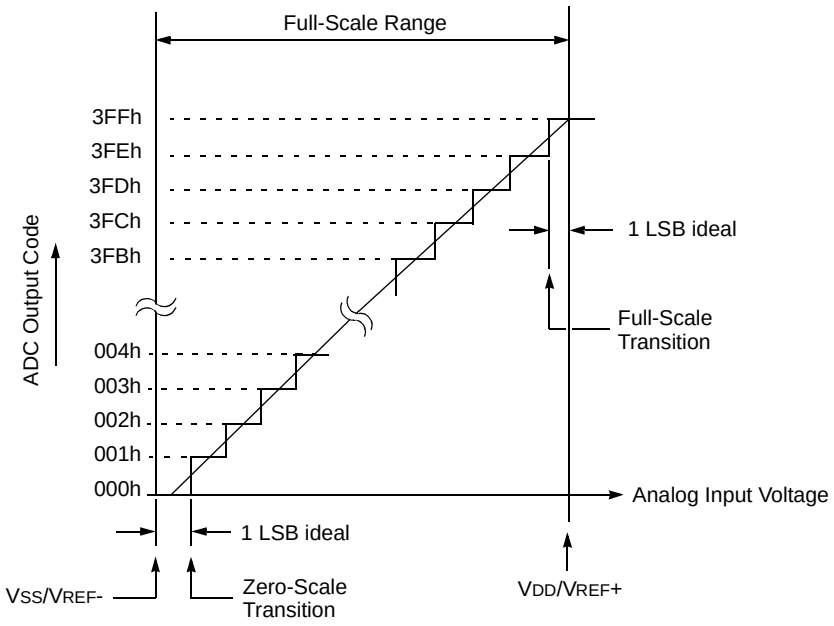
```
;This code block configures the ADC
;for polling, Vdd reference, Frc clock
;and RA0 input.
;
;Conversion start & polling for completion
; are included.
;
  BANKSEL  TRISA       ;
  BSF      TRISA,0     ;Set RA0 to input
  BANKSEL  ADCON1      ;
  MOVLW    B'01110000' ;ADC Frc clock,
  IORWF    ADCON1      ; and RA0 as analog
  BANKSEL  ADCON0      ;
  MOVLW    B'10000001' ;Right justify,
  MOVWF    ADCON0      ;Vdd Vref, AN0, On
  CALL     SampleTime  ;Acquisiton delay
  BSF      ADCON0,GO   ;Start conversion
TEST AGAIN
  BTFSC    ADCON0,GO   ;Is conversion done?
  GOTO     TEST AGAIN  ;No, test again
  BANKSEL  ADRESH      ;
  MOVF     ADRESH,W    ;Read upper 2 bits
  MOVWF    RESULTHI    ;Store in GPR space
  BANKSEL  ADRESL      ;
  MOVF     ADRESL,W    ;Read lower 8 bits
  MOVWF    RESULTLO    ;Store in GPR space
```

FIGURE 12-4: ANALOG INPUT MODEL



Legend: CPIN = Input Capacitance
VT = Threshold Voltage
ILEAKAGE = Leakage current at the pin due to various junctions
RIC = Interconnect Resistance
SS = Sampling Switch
CHOLD = Sample/Hold Capacitance

FIGURE 12-5: ADC TRANSFER FUNCTION



REGISTER 14-2: DACxREFH: DAC REFERENCE HIGH REGISTER (DACxFM = 0)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
DACR<8:1>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **DACR<8:1>**: DAC Reference Selection bits
DACxOUT = (DACR<8:0> x (Vdac_ref)/512)

REGISTER 14-3: DACxREFL: DAC REFERENCE LOW REGISTER (DACxFM = 0)

R/W-0/0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
DACR0	—	—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **DACR0**: DAC Reference Selection bits
DACxOUT = (DACR<8:0> x (Vdac_ref)/512)

bit 6-0 **Unimplemented**: Read as ‘0’

16.0 OPERATIONAL AMPLIFIER (OPA) MODULE

The Operational Amplifier (OPA) is a standard three-terminal device requiring external feedback to operate. The OPA module has the following features:

- External Connections to I/O Ports
- Selectable Unity Gain Bandwidth Product Option
- Low-Leakage Inputs
- Factory-Calibrated Input Offset Voltage

16.1 OPAxCON0 Register

The OPAxCON0 register, shown in Register 16-1, controls the OPA module.

The OPA module is enabled by setting the OPAxEN bit of the OPAxCON register. When enabled, the OPA forces the output driver of the OPAxOUT pin into tri-state to prevent contention between the driver and the OPA output.

The OPAxUGM bit of the OPAxCON register enables the Unity Gain Bandwidth mode (voltage follower) of the amplifier. In Unity Gain mode, the OPAxNCH<1:0> inputs are disabled. The default mode is normal three-terminal operation.

Note:	When the OPA module is enabled, the OPAxOUT pin is driven by the op amp output, not by the PORT digital driver. Refer to **Section 22.0 "Electrical Specifications"** for the op amp output drive capability.

16.2 Effects of a Reset

A device Reset forces all registers to their Reset state. This disables the OPA module.

16.3 OPA Module Performance

Common AC and DC performance specifications for the OPA module:

- Common Mode Voltage Range
- Leakage Current
- Input Offset Voltage
- Open Loop Gain
- Gain Bandwidth Product

Common mode voltage range is the specified voltage range for the OPAx+ and OPAx- inputs, for which the OPA module will perform within its specifications. The OPA module is designed to operate with input voltages between V_{SS} and V_{DD}. Behavior for Common mode voltages greater than V_{DD} or below V_{SS} is not guaranteed.

Leakage current is a measure of the small source or sink currents on the OPAx+ and OPAx- inputs. To minimize the effect of leakage currents, the effective impedances connected to the OPAx+ and OPAx- inputs should be kept as small as possible and equal. Input offset voltage is a measure of the voltage difference between the OPAx+ and OPAx- inputs in a closed loop circuit with the OPA in its linear region. The offset voltage will appear as a DC offset in the output equal to the input offset voltage, multiplied by the gain of the circuit.

The input offset voltage is also affected by the Common mode voltage. The OPA is factory-calibrated to minimize the input offset voltage of the module. Open loop gain is the ratio of the output voltage to the differential input voltage (OPAx+) - (OPAx-). The gain is greatest at DC and falls off with frequency.

Gain Bandwidth Product or GBWP is the frequency at which the open loop gain falls off to 0 dB. The lower GBWP is optimized for systems requiring low-frequency response and low-power consumption.

18.2 Instruction Descriptions

ADDLW	Add literal and W
Syntax:	[*label*] ADDLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) + k → (W)
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the 8-bit literal 'k' and the result is placed in the W register.

ADDWF	Add W and f
Syntax:	[*label*] ADDWF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) + (f) → (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

ANDLW	AND literal with W
Syntax:	[*label*] ANDLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) .AND. (k) → (W)
Status Affected:	Z
Description:	The contents of W register are AND'ed with the 8-bit literal 'k'. The result is placed in the W register.

ANDWF	AND W with f
Syntax:	[*label*] ANDWF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) .AND. (f) → (destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

BCF	Bit Clear f
Syntax:	[*label*] BCF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSF	Bit Set f
Syntax:	[*label*] BSF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

BTFSC	Bit Test f, Skip if Clear
Syntax:	[*label*] BTFSC f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	skip if (f<b>) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b' in register 'f' is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2-cycle instruction.

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - (W) → (destination)

Status Affected: C, DC, Z

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

C = 0	W > f
C = 1	W ≤ f
DC = 0	W<3:0> > f<3:0>
DC = 1	W<3:0> ≤ f<3:0>

SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f<3:0>) → (destination<7:4>),
(f<7:4>) → (destination<3:0>)

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

XORLW **Exclusive OR literal with W**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Description: The contents of the W register are XOR'ed with the 8-bit literal 'k'. The result is placed in the W register.

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (destination)

Status Affected: Z

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

19.5 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and STATUS registers). This must be implemented in software.

Temporary holding registers W_TEMP and STATUS_TEMP should be placed in the last 16 bytes of GPR (see Figure 2-2). These 16 locations are common to all banks and do not require banking. This makes context save and restore operations simpler. The code shown in Example 19-1 can be used to:

- Store the W register
- Store the STATUS register
- Execute the ISR code
- Restore the Status (and Bank Select Bit register)
- Restore the W register

Note:	The PIC16F753/HV753 does not require saving the PCLATH. However, if computed GOTOs are used in both the ISR and the main code, the PCLATH must be saved and restored in the ISR.

EXAMPLE 19-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF   W_TEMP              ;Copy W to TEMP register
SWAPF   STATUS,W            ;Swap status to be saved into W
                            ;Swaps are used because they do not affect the status bits
MOVWF   STATUS_TEMP         ;Save status to bank zero STATUS_TEMP register
:
:(ISR)                      ;Insert user code here
:
SWAPF   STATUS_TEMP,W       ;Swap STATUS_TEMP register into W
                            ;(sets bank to original state)
MOVWF   STATUS              ;Move W into STATUS register
SWAPF   W_TEMP,F            ;Swap W_TEMP
SWAPF   W_TEMP,W            ;Swap W_TEMP into W
```

19.6 Watchdog Timer (WDT)

The Watchdog Timer is a free running timer, using LFINTOSC oscillator as its clock source. The WDT is enabled by setting the WDTE bit of the Configuration Word (default setting). When WDTE is set, the LFINTOSC will always be enabled to provide a clock source to the WDT module.

During normal operation, a WDT time-out generates a device Reset. If the device is in Sleep mode, a WDT time-out causes the device to wake-up and continue with normal operation.

The WDT can be permanently disabled by programming the Configuration bit, WDTE, as clear (**Section 19.1 “Configuration Bits”**).

19.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms (with no prescaler). The time-out periods vary with temperature, V_{DD} and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device Reset.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

22.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40° to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on pins with respect to V_{SS}

- on V_{DD} pin
  - PIC16HV753 ..... -0.3V to +6.5V
  - PIC16F753 ..... -0.3V to +6.5V
- on $\overline{MCLR}$ ..... -0.3V to +13.5V
- on all other pins ..... -0.3V to (V_{DD} + 0.3V)

Maximum current

- on V_{SS} pin(1)
  - -40°C ≤ T_A ≤ +85°C ..... 95 mA
  - -40°C ≤ T_A ≤ +125°C ..... 95 mA
- on V_{DD} pin(1)
  - -40°C ≤ T_A ≤ +85°C ..... 95 mA
  - -40°C ≤ T_A ≤ +125°C ..... 95 mA
- on RA1, RA4, RA5 ..... 25 mA
- on RC4, RC5 ..... 50 mA

Clamp current, I_K (V_{PIN} < 0 or V_{PIN} > V_{DD}) ..... ± 20 mA

Note 1: Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characteristics. See Table 22-6 to calculate device specific limitations.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

TABLE 22-2: SUPPLY CURRENT (I_{DD})(1,2) (CONTINUED)

PIC16F753			Standard Operating Conditions (unless otherwise stated)					
PIC16HV753								
Param No.	Device Characteristics	Min.	Typ†	Max. 85°C	Max. 125°C	Units	Conditions	
							V_{DD}	Note
	Supply Current (I_{DD})(1, 2)							
D014		—	318	382	382	µA	2.0	F_{OSC} = 4 MHz HFINTOSC mode
		—	450	502	502	µA	3.0	
		—	825	100	100	µA	5.0	
D014		—	330	485	485	µA	2.0	F_{OSC} = 4 MHz HFINTOSC mode
		—	526	658	658	µA	3.0	
		—	775	980	980	µA	4.5	
D015		—	505	595	595	µA	2.0	F_{OSC} = 8 MHz HFINTOSC mode
		—	740	1200	1200	µA	3.0	
		—	1.5	1.8	1.8	mA	5.0	
D015		—	500	690	690	µA	2.0	F_{OSC} = 8 MHz HFINTOSC mode
		—	800	1100	1100	µA	3.0	
		—	1.23	1.7	1.7	mA	4.5	
D016		—	2.6	3.08	3.08	mA	4.5	F_{OSC} = 20 MHz EC Oscillator mode
		—	2.97	3.53	3.53	mA	5.0	
D016		—	2.6	3.3	3.3	mA	4.5	F_{OSC} = 20 MHz EC Oscillator mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{SS}; $\overline{MCLR}$ = V_{DD}; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

FIGURE 22-5: CLKOUT AND I/O TIMING

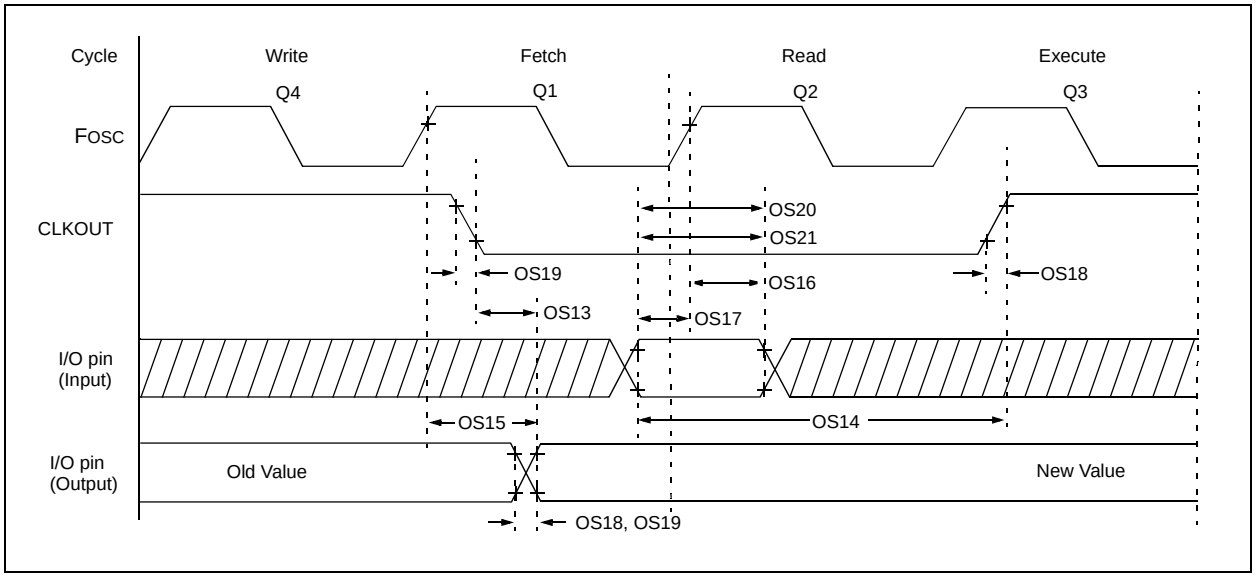


TABLE 22-9: CLKOUT AND I/O TIMING PARAMETERS

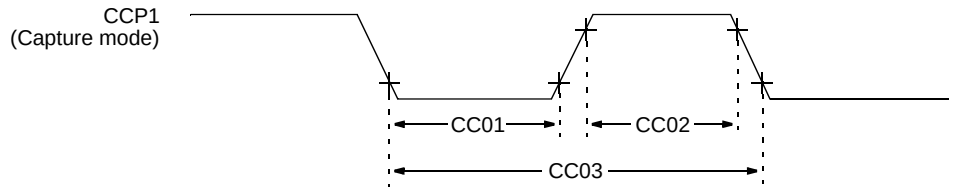
Standard Operating Conditions (unless otherwise stated)							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ †**	**Max.**	**Units**	**Conditions**
OS13	TCKL2IOV	CLKOUT↓ to Port out valid(1)	—	—	20	ns	
OS14	TIOV2CKH	Port input valid before CLKOUT↑(1)	TOSC + 200 ns	—	—	ns	
OS15	TOSH2IOV	FOSC↑ (Q1 cycle) to Port out valid	—	50	70*	ns	VDD = 5.0V
OS16	TOSH2IOI	FOSC↑ (Q2 cycle) to Port input invalid (I/O in setup time)	50	—	—	ns	VDD = 5.0V
OS17	TIOV2OSH	Port input valid to FOSC↑ (Q2 cycle) (I/O in setup time)	20	—	—	ns	
OS18	TIOR	Port output rise time	— —	40 15	72 32	ns ns	VDD = 2.0V VDD = 5.0V
OS19	TIOF	Port output fall time	— —	28 15	55 30	ns ns	VDD = 2.0V VDD = 5.0V
OS20*	TINP	INT pin input high or low time	25	—	—	ns	
OS21*	TIOC	Interrupt-on-change new input level time	TCY	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated.

Note 1: Measurements are taken in RC mode where CLKOUT output is 4 x TOSC.

FIGURE 22-9: PIC16F753/HV753 CAPTURE/COMPARE/PWM TIMINGS (CCP)



Note: Refer to Figure 22-3 for load conditions.

TABLE 22-12: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP)

Standard Operating Conditions (unless otherwise stated)								
Param No.	**Sym.**	**Characteristic**		**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
CC01*	TccL	CCP1 Input Low Time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC02*	TccH	CCP1 Input High Time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC03*	TccP	CCP1 Input Period		$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 4 or 16)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 22-13: COMPARATOR SPECIFICATIONS(1)

Standard Operating Conditions (unless otherwise stated) VDD = 5.0V, -40°C ≤ TA ≤ +125°C							
Param No.	**Sym.**	**Characteristics**	**Min.**	**Typ†**	**Max.**	**Units**	**Comments**
CM01	VIOFF	Input Offset Voltage(3)	—	± 10 ± 10	± 20 ± 20	mV mV	CxSP = 1 CxSP = 0
CM02	VICM	Input Common Mode Voltage(2)	0	—	VDD – 1.5	V	
CM03	CMRR	Common Mode Rejection Ratio	—	55	—	dB	
CM04A*	TRT(2)	Response Time	—	55	70	ns	CxSP = 1
			—	65	100	ns	CxSP = 0
CM05*	TMC20V	Comparator Mode Change to Output Valid	—	—	10	µs	
CM06	CHYSTER	Comparator Hysteresis	—	20	50	mV	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: See **Section 23.0 "DC and AC Characteristics Graphs and Charts"**and **Section 22.0 "Electrical Specifications"** for operating characterization.

2: Response time is measured with one comparator input at (VDD - 1.5V)/2 - 100 mV to (VDD - 1.5V)/2 + 20 mV. The other input is at (VDD -1.5V)/2.

3: Input offset voltage is measured with one comparator input at (VDD - 1.5V)/2.

FIGURE 23-18: IPD, FIXED VOLTAGE REFERENCE (FVR), PIC16HV753 ONLY

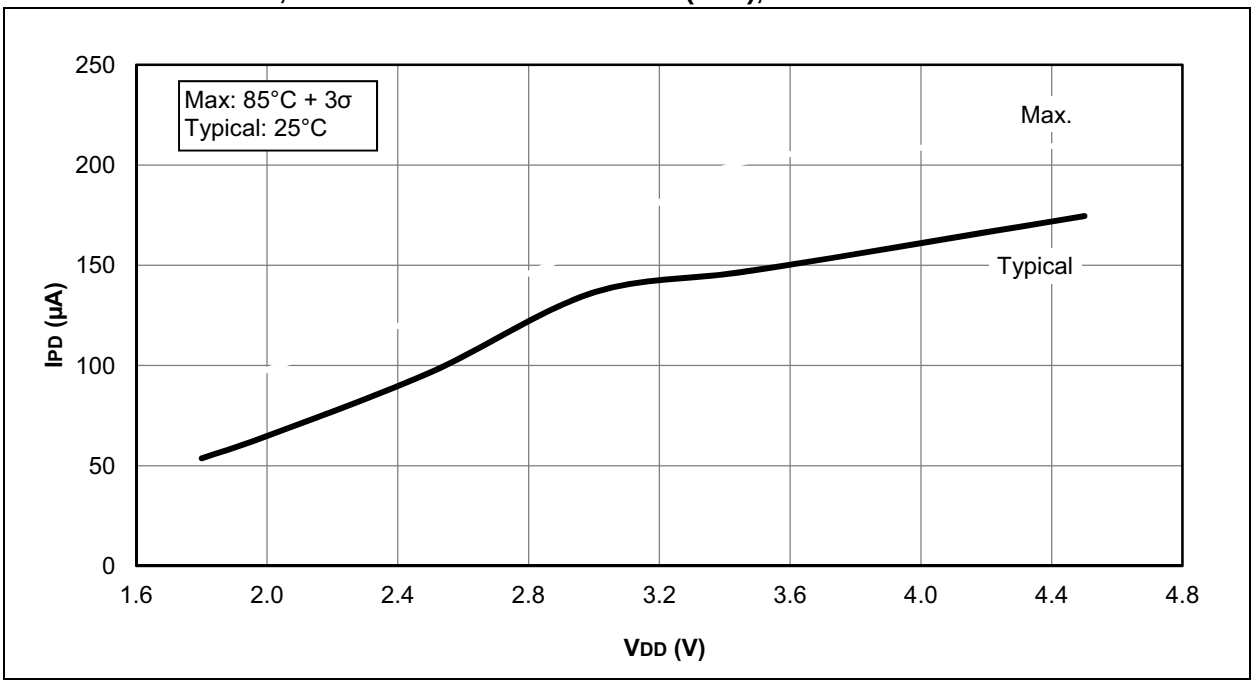


FIGURE 23-19: IPD, FIXED VOLTAGE REFERENCE (FVR), PIC16F753 ONLY

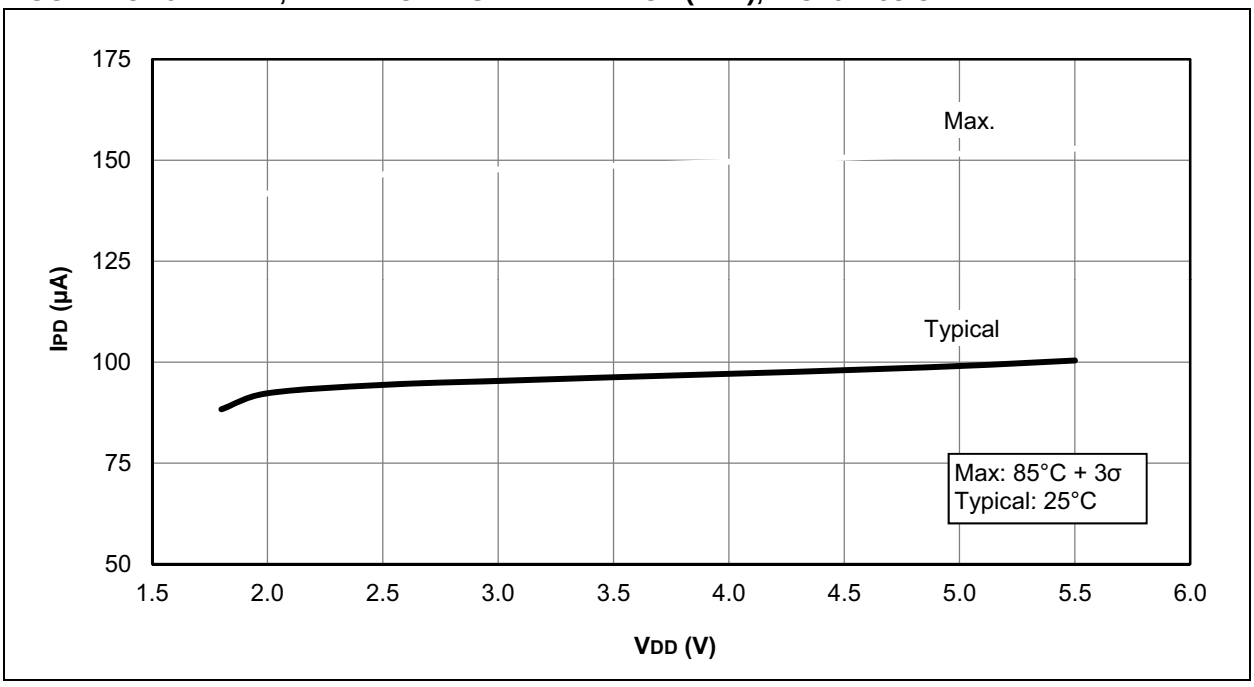


FIGURE 23-22: I_{PD}, DAC, PIC16HV753 ONLY

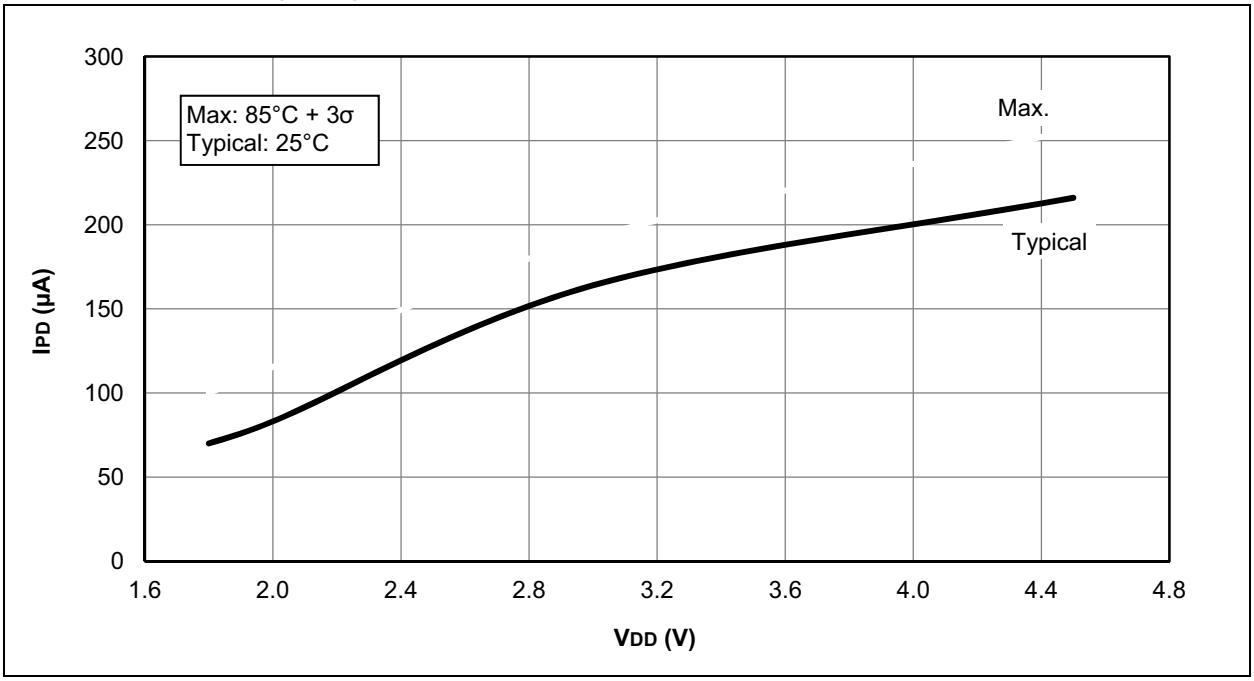
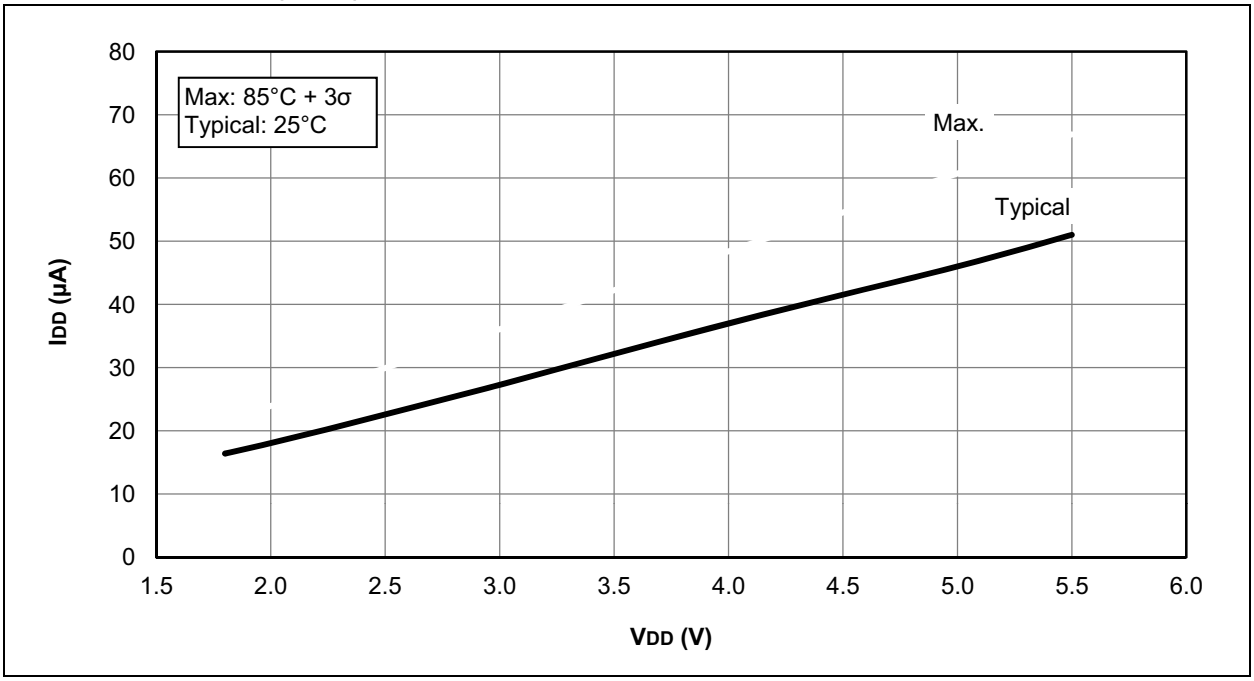


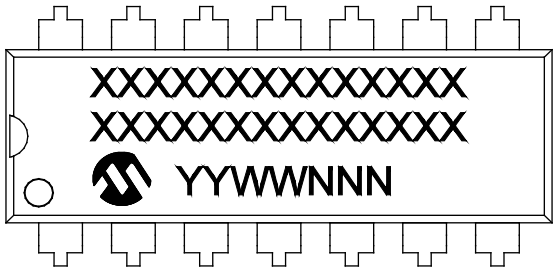
FIGURE 23-23: I_{PD}, DAC, PIC16F753 ONLY



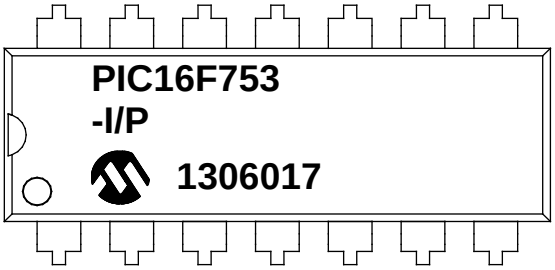
24.0 PACKAGING INFORMATION

24.1 Package Marking Information

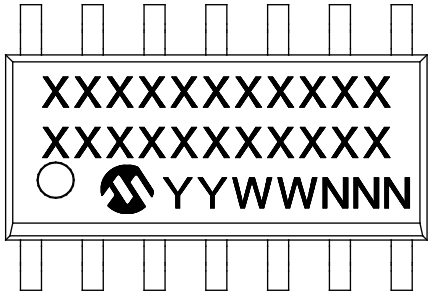
14-Lead PDIP (300 mil)



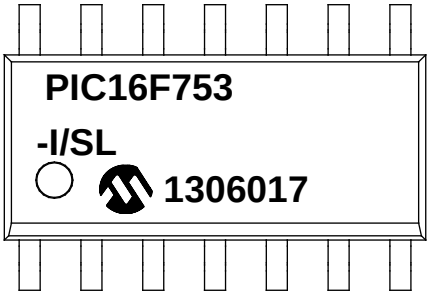
Example



14-Lead SOIC (3.90 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-	X	/XX	XXX
Device	Tape and Reel Option		Temperature Range	Package	Pattern

Device:	PIC16F753 PIC16HV753	
Tape and Reel Option:	Blank T	= Standard packaging (tube or tray) = Tape and Reel(1)
Temperature Range:	I E	= -40°C to +85°C (Industrial) = -40°C to +125°C (Extended)
Package:	P SL ST ML	= 14-lead Plastic Dual In-line (PDIP) = 14-lead Plastic Small Outline (3.90 mm) (SOIC) = 14-lead Plastic Thin Shrink Small Outline (4.4 mm) (TSSOP) = 16-lead Plastic Quad Flat, No Lead Package (4x4x0.9 mm) (QFN)
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC16F753-I/ML301
Tape and Reel,
Industrial temperature,
QFN 4x43 package,
QTP pattern #301

b) PIC16F753-E/P
Extended temperature
PDIP package

c) PIC16F753-E/SL
Extended temperature,
SOIC package

d) PIC16HV753-E/ST
Extended temperature,
TSSOP 4.4 mm package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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