Cirrus Logic Inc. - EP7311-CB-90 Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM7TDMI
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	90MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	256-LFBGA
Supplier Device Package	256-PBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep7311-cb-90

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Processor Core - ARM720T

The EP7311 incorporates an ARM 32-bit RISC microcontroller that controls a wide range of on-chip peripherals. The processor utilizes a three-stage pipeline consisting of fetch, decode and execute stages. Key features include:

- ARM (32-bit) and Thumb (16-bit compressed) instruction sets
- Enhanced MMU for Microsoft Windows CE and other operating systems
- 8 KB of 4-way set-associative cache.
- Translation Look Aside Buffers with 64 Translated Entries

Power Management

The EP7311 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V allowing the device to achieve a performance level equivalent to 60 MIPS. The device has three basic power states:

- Operating — This state is the full performance state. All the clocks and peripheral logic are enabled.
- Idle — This state is the same as the Operating State, except the CPU clock is halted while waiting for an event such as a key press.
- Standby — This state is equivalent to the computer being switched off (no display), and the main oscillator shut down. An event such as a key press can wake-up the processor.

Pin Mnemonic	I/O	Pin Description
BATOK	I	Battery ok input
nEXTPWR	I	External power supply sense input
nPWRFL	I	Power fail sense input
nBATCHG	I	Battery changed sense input

Table A. Power Management Pin Assignments

MaverickKey™ Unique ID

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

Both a specific 32-bit ID as well as a 128-bit random ID is programmed into the EP7311 through the use of laser probing technology. These IDs can then be used to match secure copyrighted content with the ID of the target device the EP7311 is powering, and then deliver the copyrighted information over a secure connection. In addition, secure transactions can benefit by also matching device IDs to server IDs. MaverickKey IDs provide a level of hardware security required for today’s Internet appliances.

Memory Interfaces

There are two main external memory interfaces. The first one is the ROM/SRAM/FLASH-style interface that has programmable wait-state timings and includes burst-mode capability, with six chip selects decoding six 256 MB sections of addressable space. For maximum flexibility, each bank can be specified to be 8-, 16-, or 32-bits wide. This allows the use of 8-bit-wide boot ROM options to minimize overall system cost. The on-chip boot ROM can be used in product manufacturing to serially download system code into system FLASH memory. To further minimize system memory requirements and cost, the ARM Thumb instruction set is supported, providing for the use of high-speed 32-bit operations in 16-bit op-codes and yielding industry-leading code density.

Pin Mnemonic	I/O	Pin Description
nCS[5:0]	O	Chip select out
A[27:0]	O	Address output
D[31:0]	I/O	Data I/O
nMOE/nSDCAS (Note)	O	ROM expansion OP enable
nMWE/nSDWE (Note)	O	ROM expansion write enable
HALFWORD	O	Halfword access select output
WORD	O	Word access select output
WRITE/nSDRAS (Note)	O	Transfer direction

Table B. Static Memory Interface Pin Assignments

Note: *Pins are multiplexed. See Table S on page 11 for more information.*

Pin Multiplexing

The following table shows the pin multiplexing of the MCP, SSI2 and the CODEC. The selection between SSI2 and the CODEC is controlled by the state of the SERSEL bit in SYSCON2. The choice between the SSI2, CODEC, and the MCP is controlled by the MCPSEL bit in SYSCON3 (see the EP73xx User's Manual for more information).

Pin Mnemonic	I/O	MCP	SSI2	CODEC
SSICLK	I/O	SIBCLK	SSICLK	PCMCLK
SSITXDA	O	SIBDOUT	SSITXDA	PCMOUT
SSIRXDA	I	SIBDIN	SSIRXDA	PCMIN
SSITXFR	I/O	SIBSYNC	SSITXFR	PCMSYNC
SSIRXFR	I	p/u	SSIRXFR	p/u
BUZ	O			

Table R. MCP/SSI2/CODEC Pin Multiplexing

The following table shows the pins that have been multiplexed in the EP7311.

Signal	Block	Signal	Block
nMOE	Static Memory	nSDCAS	SDRAM
nMWE	Static Memory	nSDWE	SDRAM
WRITE	Static Memory	nSDRAS	SDRAM
A[27:15]	Static Memory	DRA[0:12]	SDRAM
A[14:13]	Static Memory	DRA[13:14]	SDRAM
PD[7:6]	GPIO	SDQM[1:0]	SDRAM
RUN	System Configuration	CLKEN	System Configuration
nMEDCHG	Interrupt Controller	nBROM	Boot ROM select
PD[0]	GPIO	LEDFLSH	LED Flasher
PE[1:0]	GPIO	BOOTSEL[1:0]	System Configuration
PE[2]	GPIO	CLKSEL	System Configuration

Table S. Pin Multiplexing

System Design

As shown in system block diagram, simply adding desired memory and peripherals to the highly integrated EP7311 completes a low-power system solution. All necessary interface logic is integrated on-chip.

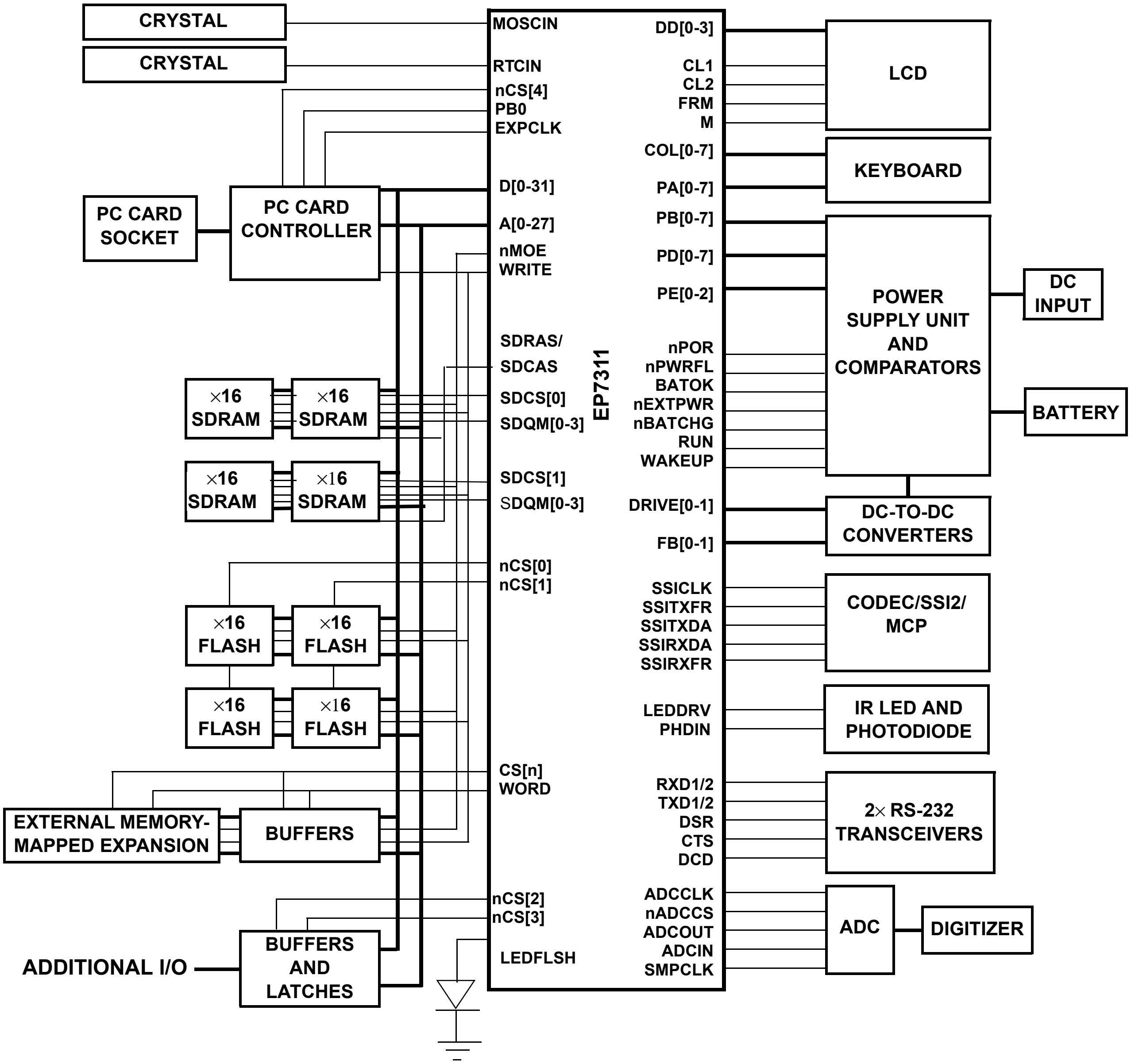

Figure 1. A Maximum EP7311 Based System

Note: A system can only use one of the following peripheral interfaces at any given time: SSI2,CODEC or MCP.

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CI/O	Transceiver capacitance	8	-	10.0	pF	
$IDD_{STANDBY}$ @ 25 C	Standby current consumption[1] Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	77 41	- -	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{STANDBY}$ @ 70 C	Standby current consumption[1] Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	- -	570 111	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{STANDBY}$ @ 85 C	Standby current consumption[1] Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	- -	1693 163	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
IDD_{idle} at 74 MHz	Idle current consumption[1] Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	6 10	- -	mA	Both oscillators running, CPU static, Cache enabled, LCD disabled, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$VDD_{STANDBY}$	Standby supply voltage	2.0	-	-	V	Minimum standby voltage for state retention, internal SRAM cache, and RTC operation only

a. Refer to the strength column in the pin assignment tables for all package types.
b. Assumes buffer has no pull-up or pull-down resistors.
c. The leakage value given assumes that the pin is configured as an input pin but is not currently being driven.

Note: *1) Total power consumption =* IDD_{CORE} *x 2.5 V +* IDD_{IO} *x 3.3 V*
2) A typical design will provide 3.3 V to the I/O supply (i.e., V_{DDIO}*), and 2.5 V to the remaining logic. This is to allow the I/O to be compatible with 3.3 V powered external logic (i.e., 3.3 V SDRAMs).*
2) Pull-up current = 50 µA typical at V_{DD} *= 3.3 V.*

SDRAM Load Mode Register Cycle

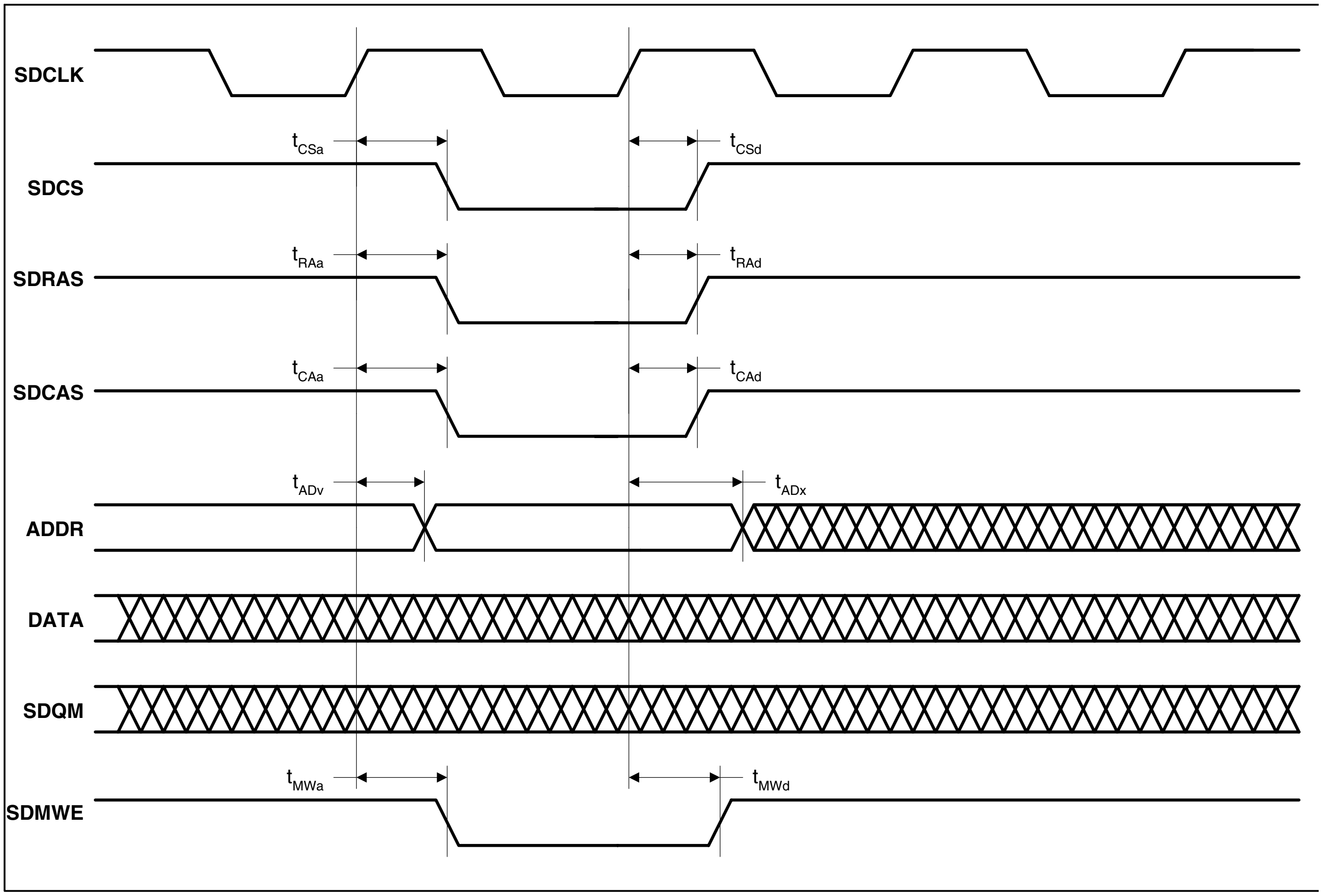

Figure 3. SDRAM Load Mode Register Cycle Timing Measurement

Note: *1. Timings are shown with CAS latency = 2*
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM control and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM control and data signals are approximately equal

SDRAM Burst Read Cycle

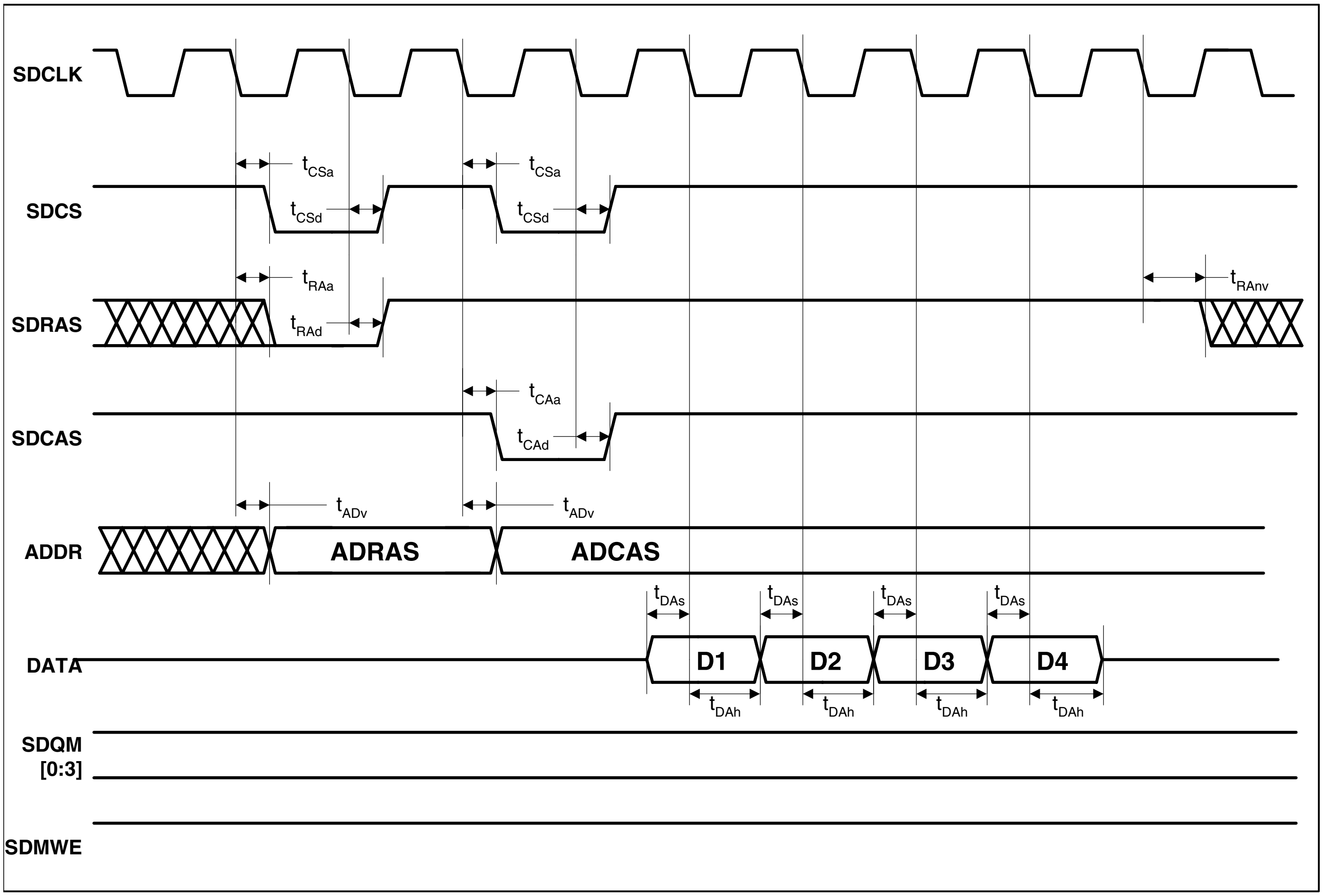

Figure 4. SDRAM Burst Read Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM control and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM control and data signals are approximately equal.

Static Memory

Figure 7 through Figure 10 define the timings associated with all phases of the Static Memory. The following table contains the values for the timings of each of the Static Memory modes.

Parameter	Symbol	Min	Typ	Max	Unit
EXPCLK rising edge to nCS assert delay time	t_{CSd}	2	8	20	ns
EXPCLK falling edge to nCS deassert hold time	t_{CSh}	2	7	20	ns
EXPCLK rising edge to A assert delay time	t_{Ad}	4	9	16	ns
EXPCLK falling edge to A deassert hold time	t_{Ah}	3	10	19	ns
EXPCLK rising edge to nMWE assert delay time	t_{MWd}	3	6	10	ns
EXPCLK rising edge to nMWE deassert hold time	t_{MWh}	3	6	10	ns
EXPCLK falling edge to nMOE assert delay time	t_{MOEd}	3	7	10	ns
EXPCLK falling edge to nMOE deassert hold time	t_{MOEh}	2	7	10	ns
EXPCLK falling edge to HALFWORD deassert delay time	t_{HWd}	2	8	20	ns
EXPCLK falling edge to WORD assert delay time	t_{WDd}	2	8	16	ns
EXPCLK rising edge to data valid delay time	t_{Dv}	8	13	21	ns
EXPCLK falling edge to data invalid delay time	t_{Dnv}	6	15	30	ns
Data setup to EXPCLK falling edge time	t_{Ds}	-	-	1	ns
EXPCLK falling edge to data hold time	t_{Dh}	-	-	3	ns
EXPCLK rising edge to WRITE assert delay time	t_{WRd}	5	11	23	ns
EXPREADY setup to EXPCLK falling edge time	t_{EXs}	-	-	0	ns
EXPCLK falling edge to EXPREADY hold time	t_{EXh}	-	-	0	ns

Static Memory Single Write Cycle

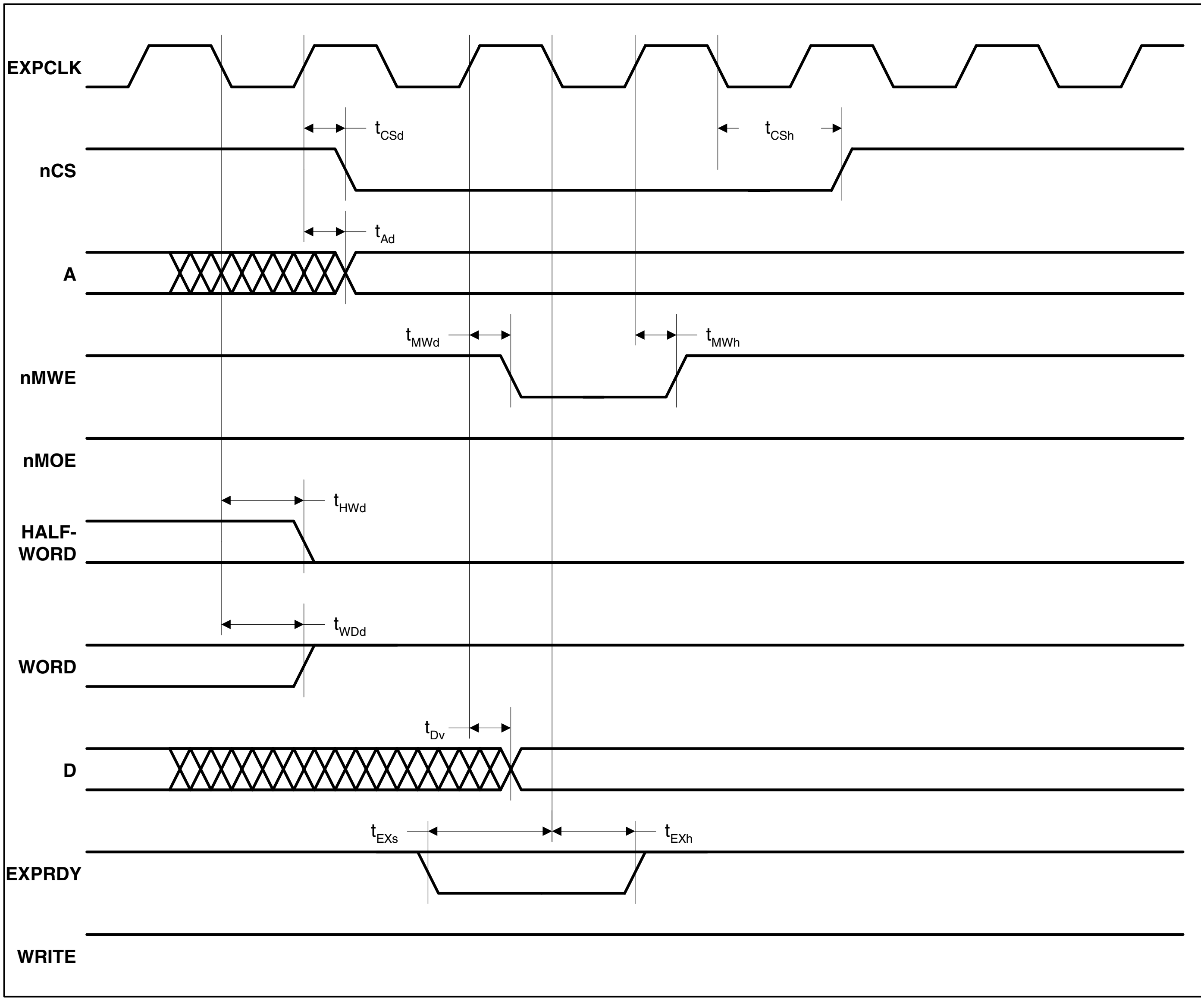

Figure 8. Static Memory Single Write Cycle Timing Measurement

Note: 1. *The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.*

2. *Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.*
3. *Address, Data, Halfword, Word, and Write hold state until next cycle.*

Static Memory Burst Write Cycle

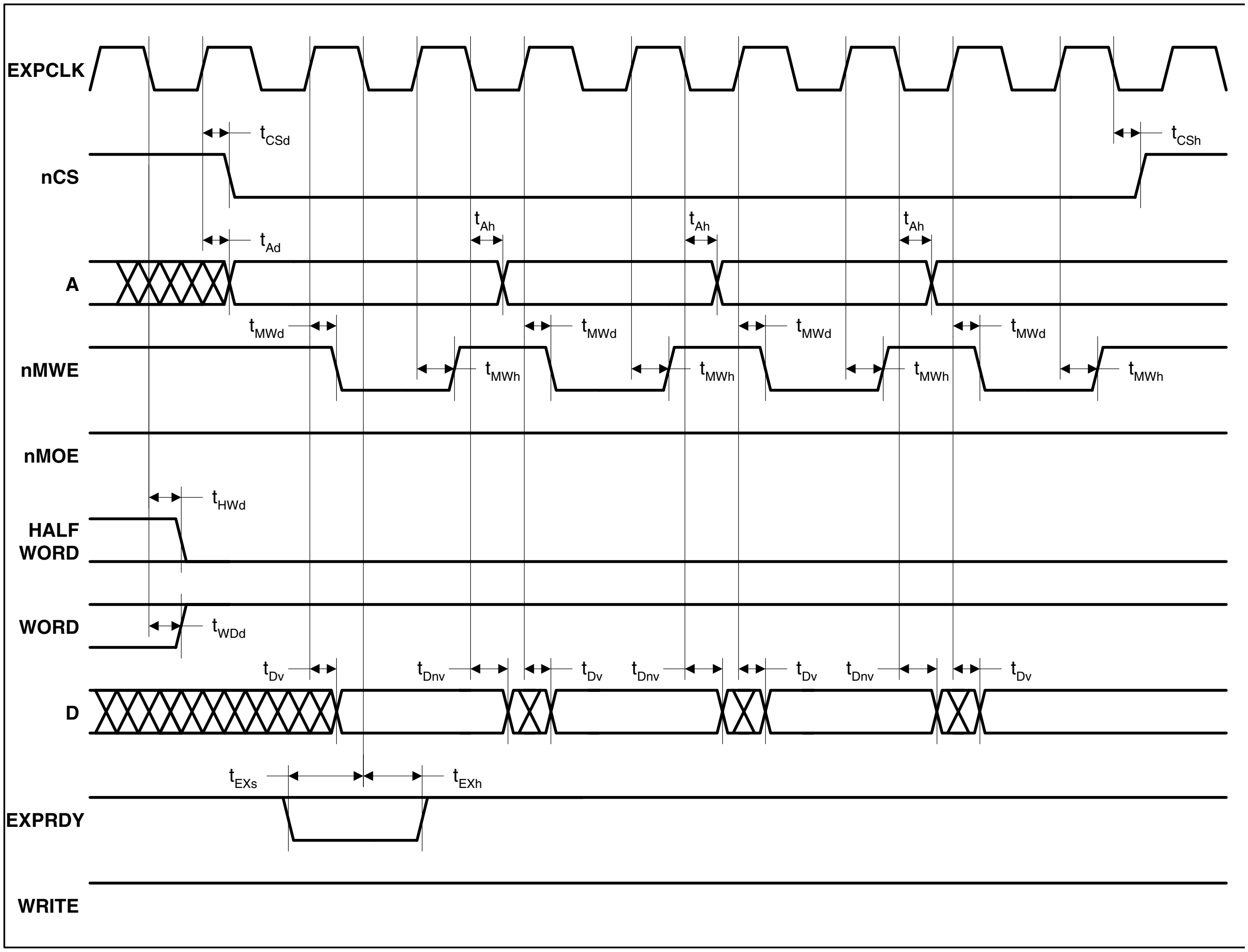

Figure 10. Static Memory Burst Write Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-1-1-1). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.

2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.

3. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.

4. Address, Data, Halfword, Word, and Write hold state until next cycle.

SSI1 Interface

Parameter	Symbol	Min	Max	Unit
ADCCLK falling edge to nADCCSS deassert delay time	t_{Cd}	9	10	ms
ADCIN data setup to ADCCLK rising edge time	t_{INs}	-	15	ns
ADCIN data hold from ADCCLK rising edge time	t_{INh}	-	14	ns
ADCCLK falling edge to data valid delay time	t_{Ovd}	– 7	13	ns
ADCCLK falling edge to data invalid delay time	t_{Od}	– 2	3	ns

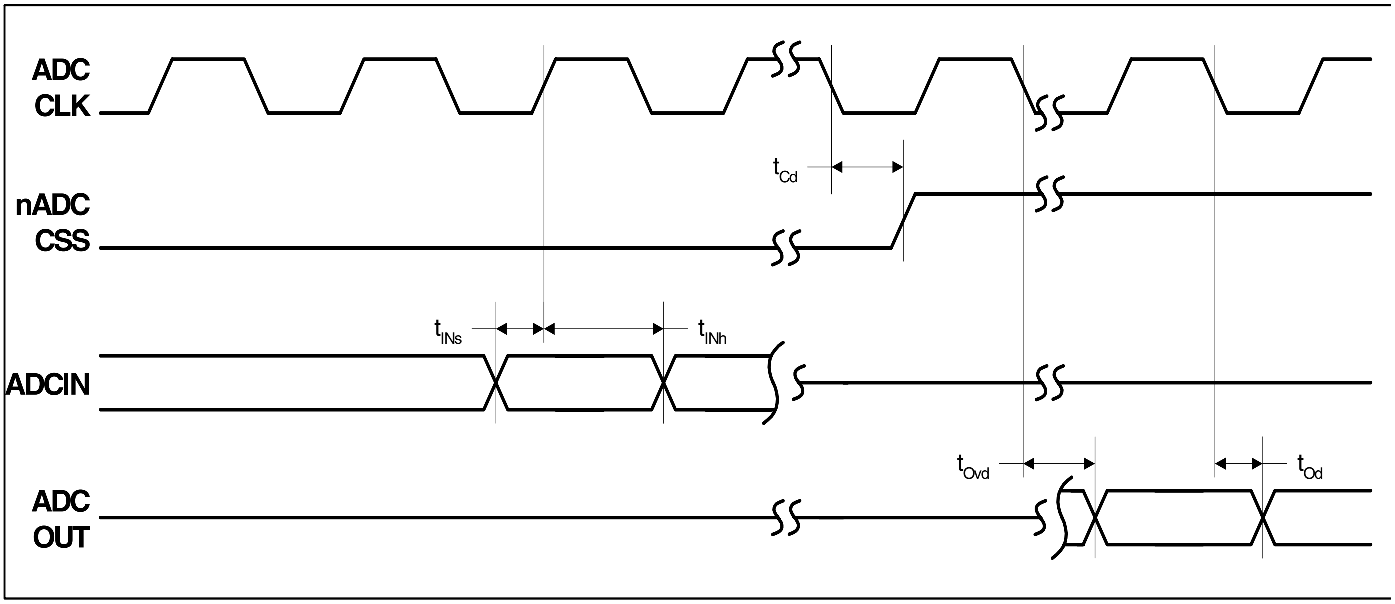

Figure 11. SSI1 Interface Timing Measurement

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
B8	DD[1]	1	Low	O	LCD serial display data
B9	M	1	Low	O	LCD AC bias drive
B10	CL[2]	1	Low	0	LCD pixel clock out
B11	D[0]	1	Low	I/O	Data I/O
B12	A[1]	2	Low	O	System byte address
B13	D[3]	2	Low	I/O	Data I/O
B14	A[4]	1	Low	O	System byte address
B15	D[6]	1	Low	I/O	Data I/O
B16	WAKEUP	Schmitt		I	System wake up input
B17	MOSCIN			I	Main oscillator input
B18	VSSIO			Pad ground	I/O ground
B19	VSSIO			Pad ground	I/O ground
B20	nURESET	Schmitt		I	User reset input
C1	RUN/CLKEN	1	Low	0	Run output / clock enable output
C2	EXPRDY	1		I	Expansion port ready input
C3	VDDIO			Pad power	Digital I/O power, 3.3 V
C4	nCS[4]	1	High	O	Chip select 4
C5	nCS[0]	1	High	O	Chip select 0
C6	SDCLK	2	Low	O	SDRAM clock out
C7	SDQM[3]	2	Low	O	SDRAM byte lane mask
C8	DD[0]	1	Low	O	LCD serial display data
C9	DD[3]	1	Low	O	LCD serial display data
C10	VDDCORE			Core power	Digital core power, 2.5 V
C11	A[0]	2	Low	O	System byte address
C12	D[2]	1	Low	I/O	Data I/O
C13	A[3]	2	Low	O	System byte address
C14	D[5]	1	Low	I/O	Data I/O
C15	A[6]	1	Low	O	System byte address
C16	VSSOSC			Oscillator ground	PLL ground
C17	VDDOSC			Oscillator power	Oscillator power in, 2.5V
C18	VSSIO			Pad ground	I/O ground
C19	BATOK			I	Battery ok input

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
C20	nPOR	Schmitt		I	Power-on reset input
D1	PB[7]	1	Input‡	I	GPIO port B
D2	RXD[2]			I	UART 2 receive data input
D3	VDDIO			Pad power	Digital I/O power, 3.3V
D18	VSSIO			Pad ground	I/O ground
D19	nBATCHG			I	Battery changed sense input
D20	A[7]	1	Low	O	System byte address
E1	PB[4]	1	Input‡	I	GPIO port B
E2	TXD[2]	1	High	O	UART 2 transmit data output
E3	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
E18	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
E19	nEXTPWR			I	External power supply sense input
E20	D[9]	1	Low	I/O	Data I/O
F1	PB[3]	1	Input‡	I/O	GPIO port B
F2	PB[6]	1	Input‡	I/O	GPIO port B
F3	TDI	with p/u*		I	JTAG data input
F18	D[7]	1	Low	I/O	Data I/O
F19	A[8]	1	Low	O	System byte address
F20	D[10]	1	Low	I/O	Data I/O
G1	PB[1]	1	Input‡	I/O	
G2	PB[2]	1	Input‡	I/O	GPIO port B
G3	PB[5]	1	Input‡	I/O	GPIO port B
G18	D[8]	1	Input‡	I/O	Data I/O
G19	A[9]	1	Low	O	System byte address
G20	D[11]	1	Low	I/O	Data I/O
H1	PA[7]	1	Input‡	I/O	GPIO port A
H[2]	TDO	1	Input‡	O	JTAG data out
H[3]	PB[0]	1	Input‡	I/O	GPIO port B
H[18]	A[10]	1	Low	O	System byte address

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
Y20	VDDIO			Pad power	Digital I/O power, 3.3V

[*] "With p/u" means with internal pull-up of 100 KOhms on the pin.

[†] Strength 1 = 4 ma
Strength 2 = 12 ma

[‡] Input. Port A,B,D,E GPIOs default to input at nPOR and URESET conditions.

256-Ball PBGA Package Characteristics

256-Ball PBGA Package Specifications

Figure 18. 256-Ball PBGA Package

Note: 1) For pin locations see Table V.
2) Dimensions are in millimeters (inches), and controlling dimension is millimeter
3) Before beginning any new EP7311 design, contact Cirrus Logic for the latest package information.

256-Ball PBGA Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VDDIO	nCS[4]	nCS[1]	SDCLK	SDQM[3]	DD[1]	M	VDDIO	D[0]	D[2]	A[3]	VDDIO	A[6]	MOSCOUT	VDDOSC	VSSIO	A
B	nCS[5]	VDDIO	nCS[3]	nMOE/ nSDCAS	VDDIO	nSDCS[1]	DD[2]	CL[1]	VDDCORE	D[1]	A[2]	A[4]	A[5]	WAKEUP	VDDIO	nURESET	B
C	VDDIO	EXPCLK	VSSIO	VDDIO	VSSIO	VSSIO	VSSIO	VDDIO	VSSIO	VSSIO	VSSIO	VDDIO	VSSIO	VSSIO	nPOR	nEXTPWR	C
D	WRITE/ nSDRAS	EXPRDY	VSSIO	VDDIO	nCS[2]	nMWE/ nSDWE	nSDCS[0]	CL[2]	VSSRTC	D[4]	nPWRFL	MOSCIN	VDDIO	VSSIO	D[7]	D[8]	D
E	RXD[2]	PB[7]	TDI	WORD	VSSIO	nCS[0]	SDQM[2]	FRM	A[0]	D[5]	VSSOSC	VSSIO	nMEDCHG/ nBROM	VDDIO	D[9]	D[10]	E
F	PB[5]	PB[3]	VSSIO	TXD[2]	RUN/ CLKEN	VSSIO	SDCKE	DD[3]	A[1]	D[6]	VSSRTC	BATOK	nBATCHG	VSSIO	D[11]	VDDIO	F
G	PB[1]	VDDIO	TDO	PB[4]	PB[6]	VSSRTC	VSSRTC	DD[0]	D[3]	VSSRTC	A[7]	A[8]	A[9]	VSSIO	D[12]	D[13]	G
H	PA[7]	PA[5]	VSSIO	PA[4]	PA[6]	PB[0]	PB[2]	VSSRTC	VSSRTC	A[10]	A[11]	A[12]	A[13]/ DRA[14]	VSSIO	D[14]	D[15]	H
J	PA[3]	PA[1]	VSSIO	PA[2]	PA[0]	TXD[1]	CTS	VSSRTC	VSSRTC	A[17]/ DRA[10]	A[16]/ DRA[11]	A[15]/ DRA[12]	A[14]/ DRA[13]	nTRST	D[16]	D[17]	J
K	LEDDRV	PHDIN	VSSIO	DCD	nTEST[1]	EINT[3]	VSSRTC	ADCIN	COL[4]	TCLK	D[20]	D[19]	D[18]	VSSIO	VDDIO	VDDIO	K
L	RXD[1]	DSR	VDDIO	nEINT[1]	PE[2]/ CLKSEL	VSSRTC	PD[0]/ LEDFLSH	VSSRTC	COL[6]	D[31]	VSSRTC	A[22]/ DRA[5]	A[21]/ DRA[6]	VSSIO	A[18]/ DRA[9]	A[19]/ DRA[8]	L
M	nTEST[0]	nEINT[2]	VDDIO	PE[0]/ BOOTSEL[0]	TMS	VDDIO	SSITXFR	DRIVE[1]	FB[0]	COL[0]	D[27]	VSSIO	A[23]/ DRA[4]	VDDIO	A[20]/ DRA[7]	D[21]	M
N	nEXTFIQ	PE[1]/ BOOTSEL[1]	VSSIO	VDDIO	PD[5]	PD[2]	SSIRXDA	ADCCLK	SMPCLK	COL[2]	D[29]	D[26]	HALFWORD	VSSIO	D[22]	D[23]	N
P	VSSRTC	RTCOUT	VSSIO	VSSIO	VDDIO	VSSIO	VSSIO	VDDIO	VSSIO	VDDIO	VSSIO	VSSIO	VDDIO	VSSIO	D[24]	VDDIO	P
R	RTCIN	VDDIO	PD[4]	PD[1]	SSITXDA	nADCCS	VDDIO	ADCOUT	COL[7]	COL[3]	COL[1]	D[30]	A[27]/ DRA[0]	A[25]/ DRA[2]	VDDIO	A[24]\ DRA[3]	R
T	VDDRTC	PD[7]/ SDQM[1]	PD[6]/ SDQM[0]	PD[3]	SSICLK	SSIRXFR	VDDCORE	DRIVE[0]	FB[1]	COL[5]	VDDIO	BUZ	D[28]	A[26]/ DRA[1]	D[25]	VSSIO	T

Table V. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
F7	SDCKE	O	SDRAM clock enable output
F8	DD[3]	O	LCD serial display data
F9	A[1]	O	System byte address
F10	D[6]	I/O	Data I/O
F11	VSSRTC	RTC ground	Real time clock ground
F12	BATOK	I	Battery ok input
F13	nBATCHG	I	Battery changed sense input
F14	VSSIO	Pad ground	I/O ground
F15	D[11]	I/O	Data I/O
F16	VDDIO	Pad power	Digital I/O power, 3.3V
G1	PB[1]	I	GPIO port B
G2	VDDIO	Pad power	Digital I/O power, 3.3V
G3	TDO	O	JTAG data out
G4	PB[4]	I	GPIO port B
G5	PB[6]	I	GPIO port B
G6	VSSRTC	Core ground	Real time clock ground
G7	VSSRTC	RTC ground	Real time clock ground
G8	DD[0]	O	LCD serial display data
G9	D[3]	I/O	Data I/O
G10	VSSRTC	RTC ground	Real time clock ground
G11	A[7]	O	System byte address
G12	A[8]	O	System byte address
G13	A[9]	O	System byte address
G14	VSSIO	Pad ground	I/O ground
G15	D[12]	I/O	Data I/O
G16	D[13]	I/O	Data I/O
H1	PA[7]	I	GPIO port A
H2	PA[5]	I	GPIO port A
H3	VSSIO	Pad ground	I/O ground
H4	PA[4]	I	GPIO port A
H5	PA[6]	I	GPIO port A
H6	PB[0]	I	GPIO port B
H7	PB[2]	I	GPIO port B
H8	VSSRTC	RTC ground	Real time clock ground
H9	VSSRTC	RTC ground	Real time clock ground
H10	A[10]	O	System byte address
H11	A[11]	O	System byte address
H12	A[12]	O	System byte address
H13	A[13]/DRA[14]	O	System byte address / SDRAM address
H14	VSSIO	Pad ground	I/O ground
H15	D[14]	I/O	Data I/O
H16	D[15]	I/O	Data I/O
J1	PA[3]	I	GPIO port A
J2	PA[1]	I	GPIO port A
J3	VSSIO	Pad ground	I/O ground
J4	PA[2]	I	GPIO port A
J5	PA[0]	I	GPIO port A
J6	TXD[1]	O	UART 1 transmit data out

Table V. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
J7	CTS	I	UART 1 clear to send input
J8	VSSRTC	RTC ground	Real time clock ground
J9	VSSRTC	RTC ground	Real time clock ground
J10	A[17]/DRA[10]	O	System byte address / SDRAM address
J11	A[16]/DRA[11]	O	System byte address / SDRAM address
J12	A[15]/DRA[12]	O	System byte address / SDRAM address
J13	A[14]/DRA[13]	O	System byte address / SDRAM address
J14	nTRST	I	JTAG async reset input
J15	D[16]	I/O	Data I/O
J16	D[17]	I/O	Data I/O
K1	LEDDRV	O	IR LED drivet
K2	PHDIN	I	Photodiode input
K3	VSSIO	Pad ground	I/O ground
K4	DCD	I	UART 1 data carrier detect
K5	nTEST[1]	I	Test mode select input
K6	EINT[3]	I	External interrupt
K7	VSSRTC	RTC ground	Real time clock ground
K8	ADCIN	I	SSI1 ADC serial input
K9	COL[4]	O	Keyboard scanner column drive
K10	TCLK	I	JTAG clock
K11	D[20]	I/O	Data I/O
K12	D[19]	I/O	Data I/O
K13	D[18]	I/O	Data I/O
K14	VSSIO	Pad ground	I/O ground
K15	VDDIO	Pad power	Digital I/O power, 3.3V
K16	VDDIO	Pad power	Digital I/O power, 3.3V
L1	RXD[1]	I	UART 1 receive data input
L2	DSR	I	UART 1 data set ready input
L3	VDDIO	Pad power	Digital I/O power, 3.3V
L4	nEINT[1]	I	External interrupt input
L5	PE[2]/CLKSEL	I	GPIO port E / clock input mode select
L6	VSSRTC	RTC ground	Real time clock ground
L7	PD[0]/LEDFLSH	I/O	GPIO port D / LED blinker output
L8	VSSRTC	Core ground	Real time clock ground
L9	COL[6]	O	Keyboard scanner column drive
L10	D[31]	I/O	Data I/O
L11	VSSRTC	RTC ground	Real time clock ground
L12	A[22]/DRA[5]	O	System byte address / SDRAM address
L13	A[21]/DRA[6]	O	System byte address / SDRAM address
L14	VSSIO	Pad ground	I/O ground
L15	A[18]/DRA[9]	O	System byte address / SDRAM address
L16	A[19]/DRA[8]	O	System byte address / SDRAM address
M1	nTEST[0]	I	Test mode select input
M2	nEINT[2]	I	External interrupt input
M3	VDDIO	Pad power	Digital I/O power, 3.3V
M4	PE[0]/BOOTSEL[0]	I	GPIO port E / Boot mode select
M5	TMS	I	JTAG mode select
M6	VDDIO	Pad power	Digital I/O power, 3.3V

Table W. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
44	T3	N1	nEXTFIQ	I	79
45	R1	L5	PE[2]/CLKSEL	I/O	80
46	R2	N2	PE[1]/BOOTSEL1	I/O	83
47	T1	M4	PE[0]/BOOTSEL0	I/O	86
53	T2	T2	PD[7]/SDQM[1]	I/O	89
54	V4	T3	PD[6/SDQM[0]]	I/O	92
55	W4	N5	PD[5]	I/O	95
56	Y4	R3	PD[4]	I/O	98
59	V5	T4	PD[3]	I/O	101
60	W5	N6	PD[2]	I/O	104
61	Y5	R4	PD[1]	I/O	107
62	V6	L7	PD[0]/LEDFLSH	O	110
68	W6	T6	SSIRXFR	I/O	122
69	Y6	K8	ADCIN	I	125
70	W8	R6	nADCCS	O	126
75	Y8	M8	DRIVE1	I/O	128
76	V9	T8	DRIVE0	I/O	131
77	W10	N8	ADCCLK	O	134
78	Y10	R8	ADCOUT	O	136
79	V11	N9	SMPCLK	O	138
80	W11	T9	FB1	I	140
82	Y11	M9	FB0	I	141
83	Y12	R9	COL7	O	142
84	W12	L9	COL6	O	144
85	V12	T10	COL5	O	146
86	Y13	K9	COL4	O	148
87	W13	R10	COL3	O	150
88	V13	N10	COL2	O	152
91	Y14	R11	COL1	O	154
92	W14	M10	COL0	O	156
93	A1	T12	BUZ	O	158
94	V14	L10	D[31]	I/O	160
95	Y15	R12	D[30]	I/O	163
96	W15	N11	D[29]	I/O	166
97	V15	T13	D[28]	I/O	169
99	Y16	R13	A[27]/DRA[0]	Out	172
100	W16	M11	D[27]	I/O	174
101	V16	T14	A[26]/DRA[1]	O	177

Table W. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
102	Y17	N12	D[26]	I/O	179
103	W17	R14	A[25]/DRA[2]	O	182
104	Y18	T15	D[25]	I/O	184
105	V17	N13	HALFWORD	O	187
106	W18	R16	A[24]/DRA[3]	O	189
109	Y19	P15	D[24]	I/O	191
110	W20	M13	A[23]/DRA[4]	O	194
111	U18	N16	D[23]	I/O	196
112	V20	L12	A[22]/DRA[5]	O	199
113	U19	N15	D[22]	I/O	201
114	U20	L13	A[21]/DRA[6]	O	204
115	T19	M16	D[21]	I/O	206
117	T20	M15	A[20]/DRA[7]	O	209
118	R19	K11	D[20]	I/O	211
119	R20	L16	A[19]/DRA[8]	O	214
120	T18	K12	D[19]	I/O	216
121	P19	L15	A[18]/DRA[9]	O	219
122	P20	K13	D[18]	I/O	221
126	R18	J10	A[17]/DRA[10]	O	224
127	N19	J16	D[17]	I/O	226
128	N20	J11	A[16]/DRA[11]	O	229
129	P18	J15	D[16]	I/O	231
130	M19	J12	A[15]/DRA[12]	O	234
131	N18	H16	D[15]	I/O	236
132	L20	J13	A[14]/DRA[13]	O	239
133	L19	H15	D[14]	I/O	241
134	M18	H13	A[13]/DRA[14]	O	244
135	K20	G16	D[13]	I/O	246
136	K19	H12	A[12]	O	249
137	K18	G15	D[12]	I/O	251
138	J20	H11	A[11]	O	254
141	J19	F15	D[11]	I/O	256
142	H20	H10	A[10]	O	259
143	H19	E16	D[10]	I/O	261
144	J18	G13	A[9]	O	264
145	K3	E15	D[9]	I/O	266
146	Y3	G12	A[8]	O	269
147	G20	D16	D[8]	I/O	271

Table W. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
148	H18	G11	A[7]	O	274
150	F20	D15	D[7]	I/O	276
151	G19	F13	nBATCHG	I	279
152	E20	C16	nEXTPWR	I	280
153	F19	F12	BATOK	I	281
154	G18	C15	nPOR	I	282
155	D20	E13	nMEDCHG/nBROM	I	283
156	F18	B16	nURESET	I	284
161	D19	B14	WAKEUP	I	285
162	E19	D11	nPWRFL	I	286
163	C19	A13	A[6]	O	287
164	C20	F10	D[6]	I/O	289
165	E18	B13	A[5]	O	292
166	B20	E10	D[5]	I/O	294
169	B16	B12	A[4]	O	297
170	A16	D10	D[4]	I/O	299
171	C15	A11	A[3]	O	302
172	B15	G9	D[3]	I/O	304
173	A15	B11	A[2]	O	307
175	C14	A10	D[2]	I/O	309
176	B14	F9	A[1]	O	312
177	A14	B10	D[1]	I/O	314
178	C13	E9	A[0]	O	317
179	B13	A9	D[0]	I/O	319
184	A13	D8	CL2	O	322
185	C12	B8	CL1	O	324
186	B12	E8	FRM	O	326
187	A12	A7	M	O	328
188	C11	F8	DD[3]	I/O	330
189	B11	B7	DD[2]	I/O	333
191	B10	A6	DD[1]	I/O	336
192	A10	G8	DD[0]	I/O	339
193	A9	B6	nSDCS[1]	O	342
194	B9	D7	nSDCS[0]	O	344
195	C9	A5	SDQM[3]	I/O	346
196	A8	E7	SDQM[2]	I/O	349
199	B8	F7	SDCKE	I/O	352
200	C8	A4	SDCLK	I/O	355

Ordering Information

Model	Temperature	Package
EP7311-CB	0 to +70 °C	256-pin PBGA, 17mm X 17mm
EP7311-CB-90 (90 MHz)		
EP7311-IB	-40 to +85 °C.	
EP7311-IB-90 (90 MHz)		
EP7311-CV	0 to +70 °C	208-pin LQFP.
EP7311-IV	-40 to +85 °C.	
EP7311-CR	0 to +70 °C	204-pin TFBGA, 13mm X 13mm.
EP7311-CR-90 (90 MHz)		

Environmental, Manufacturing, & Handling Information

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
EP7311-CB	225 °C	3	7 Days
EP7311-CB-90 (90 MHz)			
EP7311-IB			
EP7311-IB-90 (90 MHz)			
EP7311-CV			
EP7311-IV			
EP7311-CR			
EP7311-CR-90 (90 MHz)			

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

Revision History

Revision	Date	Changes
PP1	NOV 2003	First preliminary release.
F1	AUG 2005	Updated SDRAM timing. Added MSL data.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to www.cirrus.com

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