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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM7TDMI
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	90MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	208-LQFP
Supplier Device Package	208-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep7311-cv-90

The second is the programmable 16- or 32-bit-wide SDRAM interface that allows direct connection of up to two banks of SDRAM, totaling 512 Mb. To assure the lowest possible power consumption, the EP7311 supports self-refresh SDRAMs, which are placed in a low-power state by the device when it enters the low-power Standby State.

Pin Mnemonic	I/O	Pin Description
SDCLK	O	SDRAM clock output
SDCKE	O	SDRAM clock enable output
nSDCS[1:0]	O	SDRAM chip select out
WRITE/nSDRAS (Note 2)	O	SDRAM RAS signal output
nMOE/nSDCAS (Note 2)	O	SDRAM CAS control signal
nMWE/nSDWE (Note 2)	O	SDRAM write enable control signal
A[27:15]/DRA[0:12] (Note 1)	O	SDRAM address
A[14:13]/DRA[12:14]	O	SDRAM internal bank select
PD[7:6]/SDQM[1:0] (Note 2)	I/O	SDRAM byte lane mask
SDQM[3:2]	O	SDRAM byte lane mask
D[31:0]	I/O	Data I/O

Table C. SDRAM Interface Pin Assignments

Note: 1. Pins A[27:13] map to DRA[0:14] respectively. (i.e. A[27}/DRA[0}, A[26}/DRA[1], etc.) This is to balance the load for large memory systems.
2. Pins are multiplexed. See Table S on page 11 for more information.

Digital Audio Capability

The EP7311 uses its powerful 32-bit RISC processing engine to implement audio decompression algorithms in software. The nature of the on-board RISC processor, and the availability of efficient C-compilers and other software development tools, ensures that a wide range of audio decompression algorithms can easily be ported to and run on the EP7311

Universal Asynchronous Receiver/Transmitters (UARTs)

The EP7311 includes two 16550-type UARTs for RS-232 serial communications, both of which have two 16-byte FIFOs for receiving and transmitting data. The UARTs support bit rates up to 115.2 kbps. An IrDA SIR protocol encoder/decoder can be optionally switched into the RX/TX signals to/from UART 1 to enable these signals to drive an infrared communication interface directly.

Pin Mnemonic	I/O	Pin Description
TXD[1]	O	UART 1 transmit
RXD[1]	I	UART 1 receive
CTS	I	UART 1 clear to send
DCD	I	UART 1 data carrier detect
DSR	I	UART 1 data set ready
TXD[2]	O	UART 2 transmit
RXD[2]	I	UART 2 receive
LEDDRV	O	Infrared LED drive output
PHDIN	I	Photo diode input

Table D. Universal Asynchronous Receiver/Transmitters Pin Assignments

Multimedia Codec Port (MCP)

The Multimedia Codec Port provides access to an audio codec, a telecom codec, a touchscreen interface, four general purpose analog-to-digital converter inputs, and ten programmable digital I/O lines.

Pin Mnemonic	I/O	Pin Description
SIBCLK	O	Serial bit clock
SIBDOUT	O	Serial data out
SIBDIN	I	Serial data in
SIBSYNC	O	Sample clock

Table E. MCP Interface Pin Assignments

Note: See Table R on page 11 for information on pin multiplexes.

SDRAM Burst Read Cycle

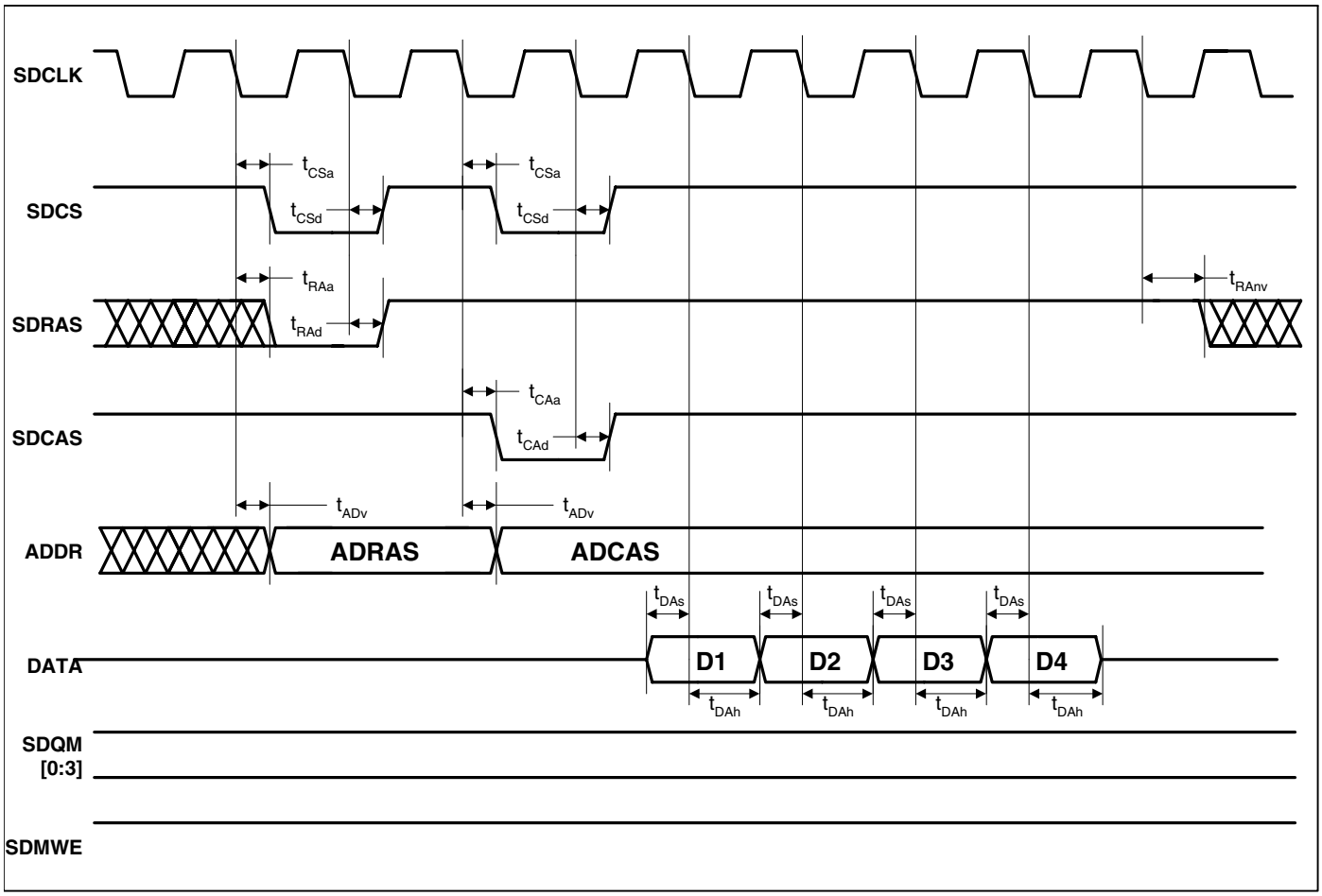


Figure 4. SDRAM Burst Read Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM control and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM control and data signals are approximately equal.

Static Memory

Figure 7 through Figure 10 define the timings associated with all phases of the Static Memory. The following table contains the values for the timings of each of the Static Memory modes.

Parameter	Symbol	Min	Typ	Max	Unit
EXPCLK rising edge to nCS assert delay time	t_{CSd}	2	8	20	ns
EXPCLK falling edge to nCS deassert hold time	t_{CSh}	2	7	20	ns
EXPCLK rising edge to A assert delay time	t_{Ad}	4	9	16	ns
EXPCLK falling edge to A deassert hold time	t_{Ah}	3	10	19	ns
EXPCLK rising edge to nMWE assert delay time	t_{MWd}	3	6	10	ns
EXPCLK rising edge to nMWE deassert hold time	t_{MWh}	3	6	10	ns
EXPCLK falling edge to nMOE assert delay time	t_{MOEd}	3	7	10	ns
EXPCLK falling edge to nMOE deassert hold time	t_{MOEh}	2	7	10	ns
EXPCLK falling edge to HALFWORD deassert delay time	t_{HWd}	2	8	20	ns
EXPCLK falling edge to WORD assert delay time	t_{WDd}	2	8	16	ns
EXPCLK rising edge to data valid delay time	t_{Dv}	8	13	21	ns
EXPCLK falling edge to data invalid delay time	t_{Dnv}	6	15	30	ns
Data setup to EXPCLK falling edge time	t_{Ds}	-	-	1	ns
EXPCLK falling edge to data hold time	t_{Dh}	-	-	3	ns
EXPCLK rising edge to WRITE assert delay time	t_{WRd}	5	11	23	ns
EXPREADY setup to EXPCLK falling edge time	t_{EXs}	-	-	0	ns
EXPCLK falling edge to EXPREADY hold time	t_{EXh}	-	-	0	ns

Static Memory Single Read Cycle

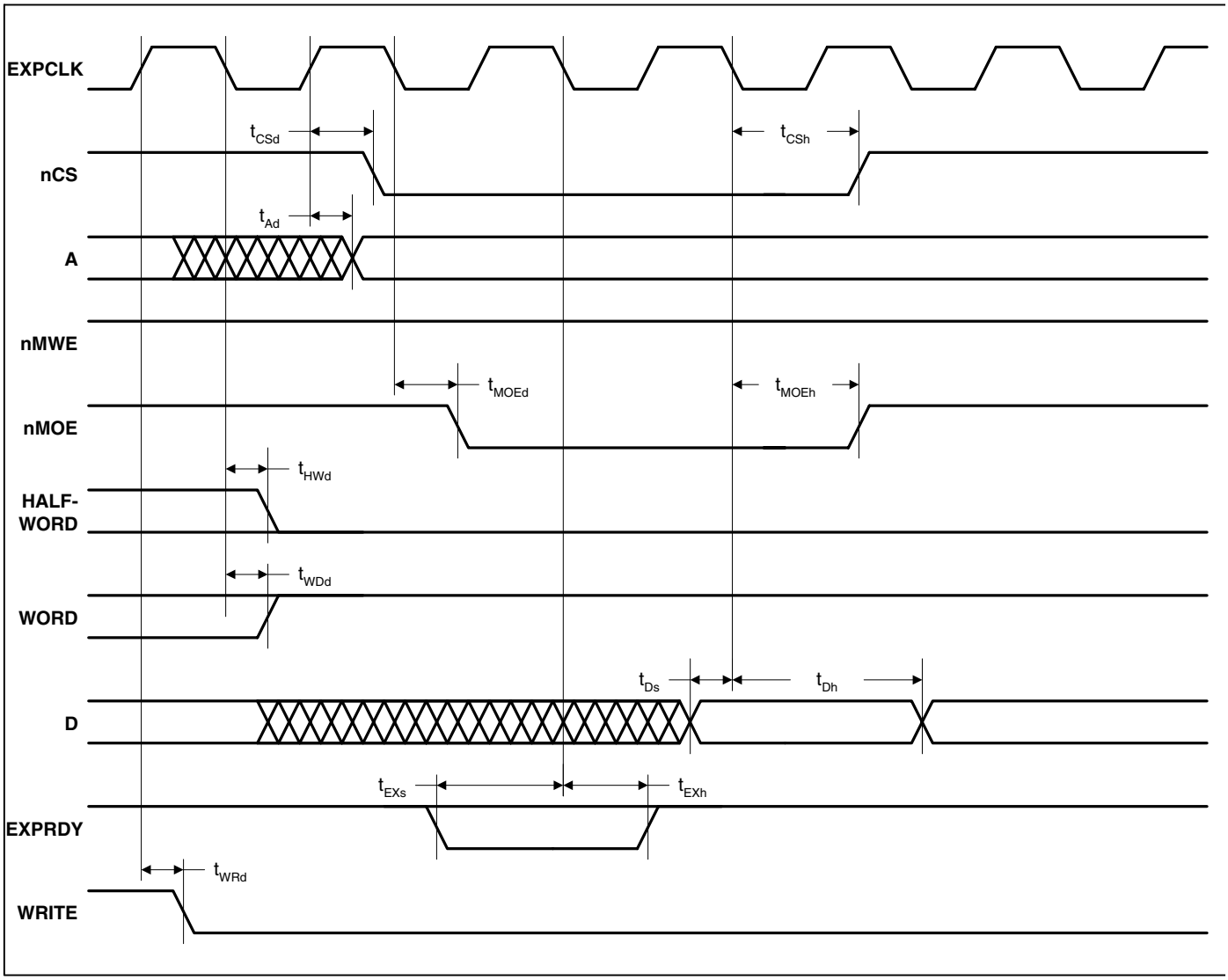


Figure 7. Static Memory Single Read Cycle Timing Measurement

Note: 1. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
2. Address, Halfword, Word, and Write hold state until next cycle.

Static Memory Burst Write Cycle

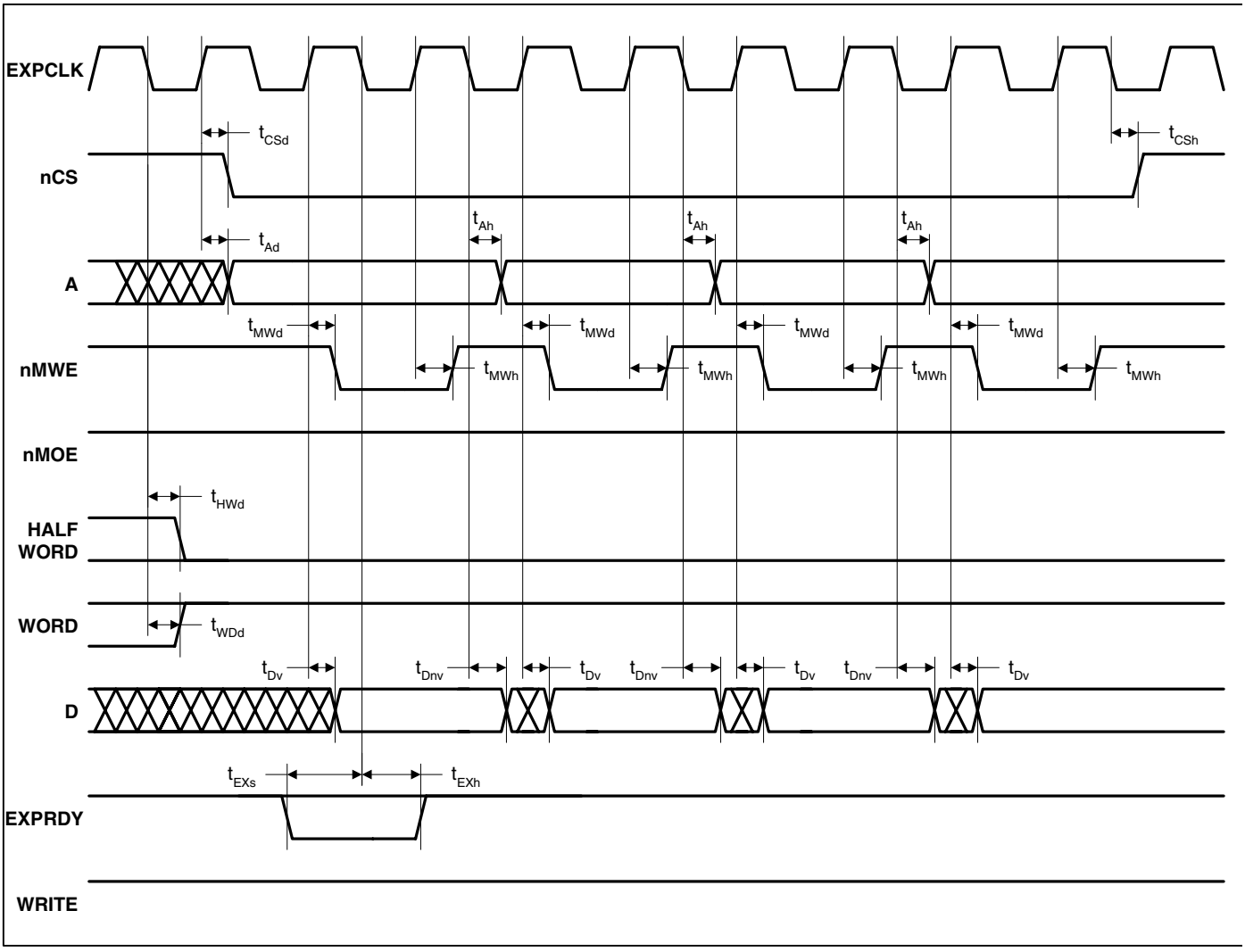


Figure 10. Static Memory Burst Write Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-1-1-1). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.
2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
3. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.
4. Address, Data, Halfword, Word, and Write hold state until next cycle.

SSI1 Interface

Parameter	Symbol	Min	Max	Unit
ADCCLK falling edge to nADCCSS deassert delay time	t_{Cd}	9	10	ms
ADCIN data setup to ADCCLK rising edge time	t_{INs}	-	15	ns
ADCIN data hold from ADCCLK rising edge time	t_{INh}	-	14	ns
ADCCLK falling edge to data valid delay time	t_{Ovd}	– 7	13	ns
ADCCLK falling edge to data invalid delay time	t_{Od}	– 2	3	ns

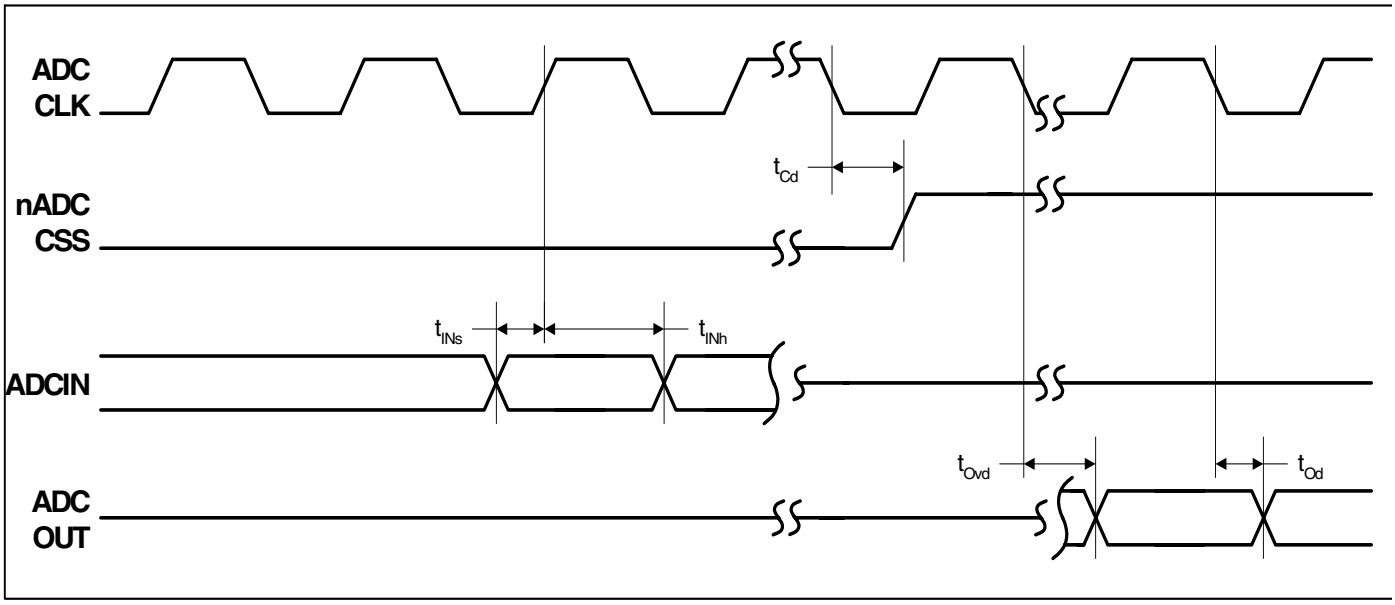


Figure 11. SSI1 Interface Timing Measurement

SSI2 Interface

Parameter	Symbol	Min	Max	Unit
SSICLK period (slave mode)	t_{clk_per}	185	2050	ns
SSICLK high time	t_{clk_high}	925	1025	ns
SSICLK low time	t_{clk_low}	925	1025	ns
SSICLK rise/fall time	t_{clkrf}	3	18	ns
SSICLK rising edge to RX and/or TX frame sync high time	t_{FRd}	-	3	ns
SSICLK rising edge to RX and/or TX frame sync low time	t_{FRa}	-	8	ns
SSIRXFR and/or SSITXFR period	t_{FR_per}	960	990	ns
SSIRXDA setup to SSICLK falling edge time	t_{RXs}	3	7	ns
SSIRXDA hold from SSICLK falling edge time	t_{RXh}	3	7	ns
SSICLK rising edge to SSITXDA data valid delay time	t_{TXd}	-	2	ns
SSITXDA valid time	t_{TXv}	960	990	ns

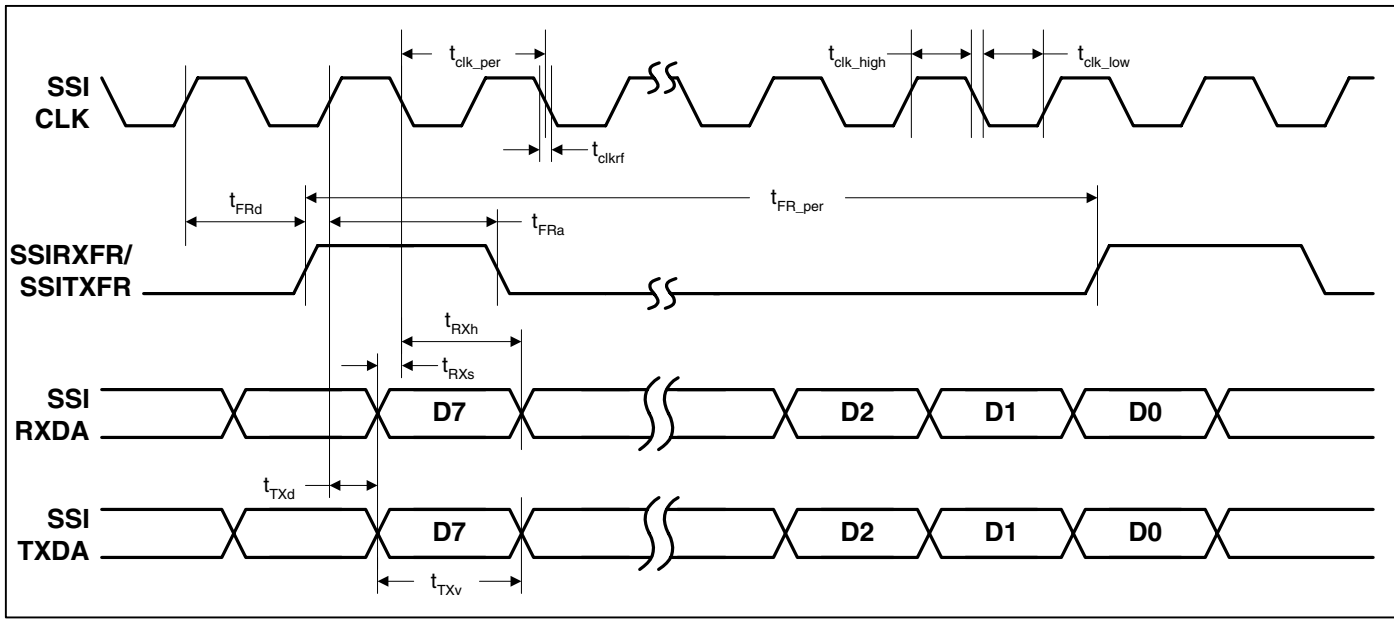


Figure 12. SSI2 Interface Timing Measurement

JTAG Interface

Parameter	Symbol	Min	Max	Units
TCK clock period	t_{clk_per}	2	-	ns
TCK clock high time	t_{clk_high}	1	-	ns
TCK clock low time	t_{clk_low}	1	-	ns
JTAG port setup time	t_{JPs}	-	0	ns
JTAG port hold time	t_{JPh}	-	3	ns
JTAG port clock to output	t_{JPco}	-	10	ns
JTAG port high impedance to valid output	t_{JPzx}	-	12	ns
JTAG port valid output to high impedance	t_{JPxz}	-	19	ns

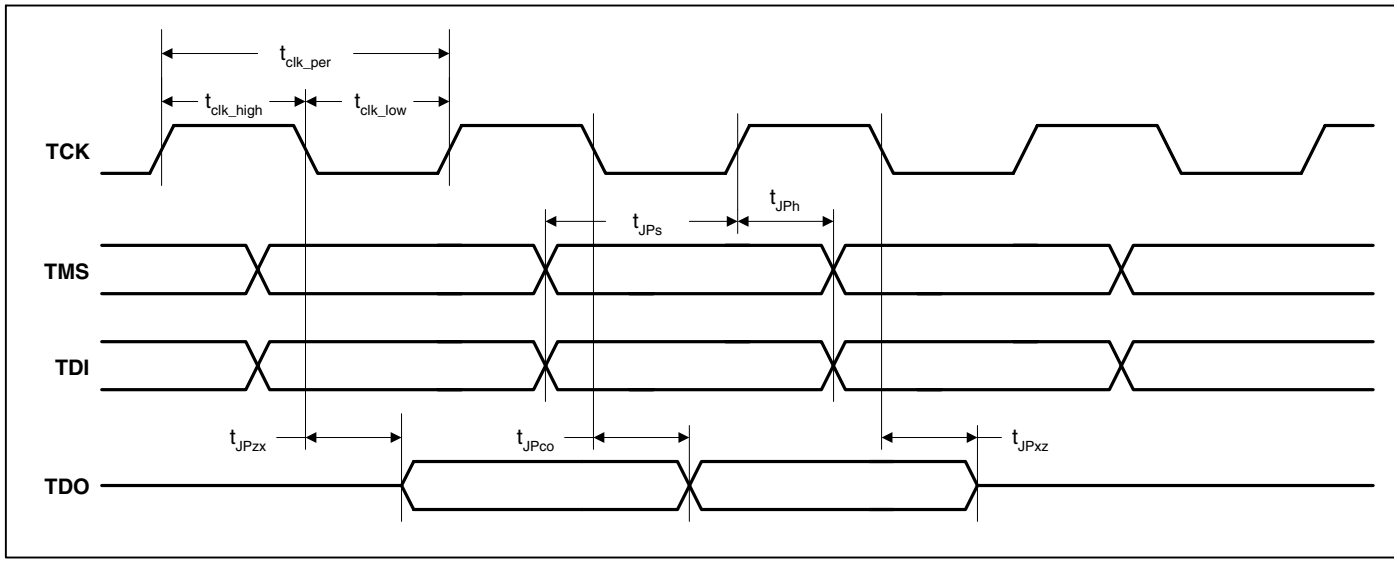


Figure 14. JTAG Timing Measurement

Packages

208-Pin LQFP Package Characteristics

208-Pin LQFP Package Specifications

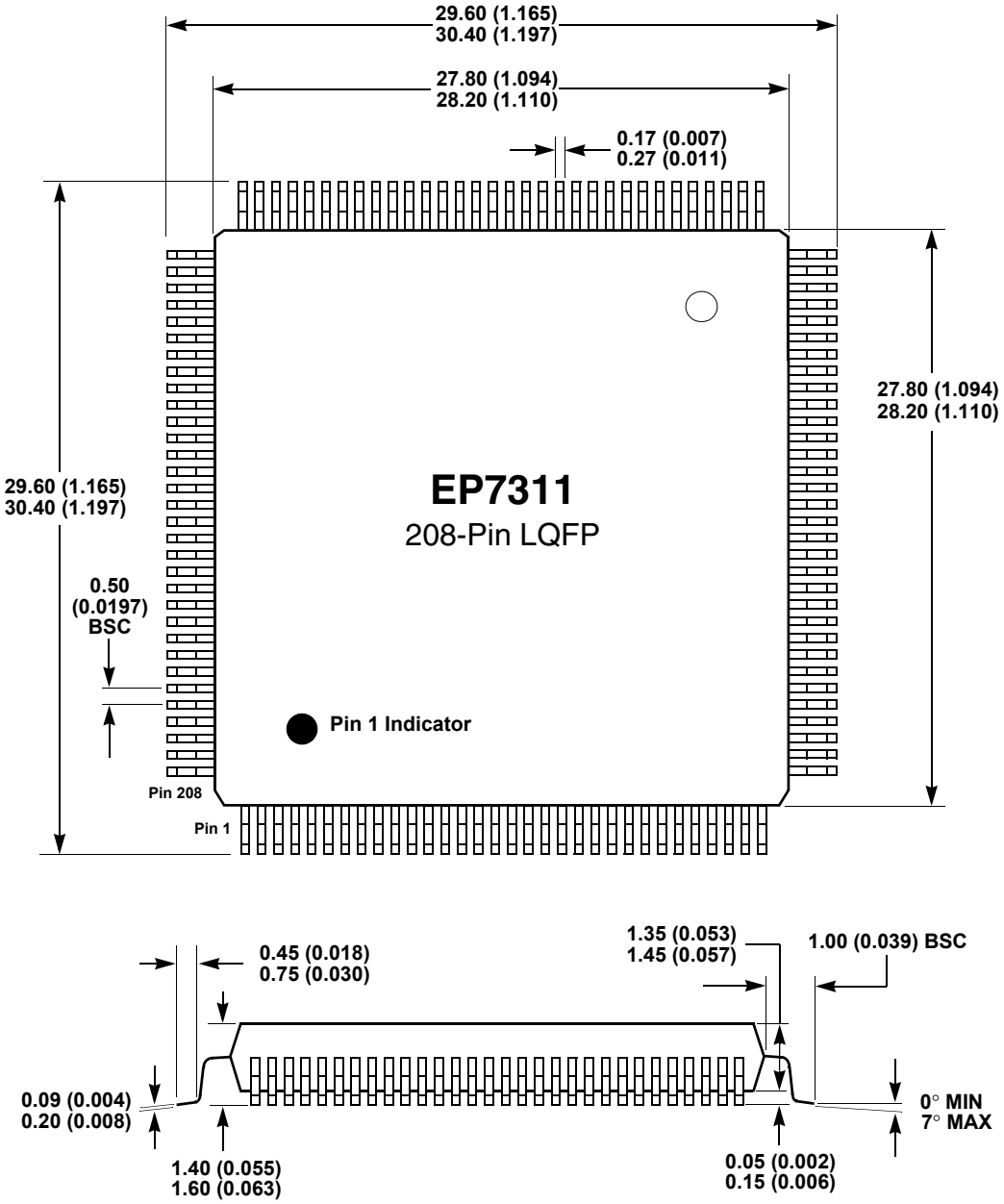


Figure 15. 208-Pin LQFP Package Outline Drawing

Note: 1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.
4) For pin locations, please see Figure 16. For pin descriptions see the EP7311 User's Manual.

Table T. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Type	Strength	Reset State
148	A[7]	O	1	Low
149	VSSIO	Pad Gnd		
150	D[7]	I/O	1	Low
151	nBATCHG	I		
152	nEXTPWR	I		
153	BATOK	I		
154	nPOR	I	Schmitt	
155	nMEDCHG/ nBROM	I		
156	nURESET	I	Schmitt	
157	VDDOSC	Osc Pwr		
158	MOSCIN	Osc		
159	MOSCOUT	Osc		
160	VSSOSC	Osc Gnd		
161	WAKEUP	I	Schmitt	
162	nPWRFL	I		
163	A[6]	O	1	Low
164	D[6]	I/O	1	Low
165	A[5]	Out	1	Low
166	D[5]	I/O	1	Low
167	VDDIO	Pad Pwr		
168	VSSIO	Pad Gnd		
169	A[4]	O	1	Low
170	D[4]	I/O	1	Low
171	A[3]	O	2	Low
172	D[3]	I/O	1	Low
173	A[2]	O	2	Low
174	VSSIO	Pad Gnd		
175	D[2]	I/O	1	Low
176	A[1]	O	2	Low
177	D[1]	I/O	1	Low
178	A[0]	O	2	Low
179	D[0]	I/O	1	Low
180	VSS CORE	Core Gnd		
181	VDD CORE	Core Pwr		
182	VSSIO	Pad Gnd		
183	VDDIO	Pad Pwr		
184	CL[2]	O	1	Low
185	CL[1]	O	1	Low

Table T. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Type	Strength	Reset State
186	FRM	O	1	Low
187	M	O	1	Low
188	DD[3]	I/O	1	Low
189	DD[2]	I/O	1	Low
190	VSSIO	Pad Gnd		
191	DD[1]	I/O	1	Low
192	DD[0]	I/O	1	Low
193	nSDCS[1]	O	1	High
194	nSDCS[0]	O	1	High
195	SDQM[3]	I/O	2	Low
196	SDQM[2]	I/O	2	Low
197	VDDIO	Pad Pwr		
198	VSSIO	Pad Gnd		
199	SDCKE	I/O	2	Low
200	SDCLK	I/O	2	Low
201	nMWE/nSDWE	O	1	High
202	nMOE/nSDCAS	O	1	High
203	VSSIO	Pad Gnd		
204	nCS[0]	O	1	High
205	nCS[1]	O	1	High
206	nCS[2]	O	1	High
207	nCS[3]	O	1	High
208	nCS[4]	O	1	High

*With p/u' means with internal pull-up on the pin.

204-Ball TFBGA Package Characteristics

204-Ball TFBGA Package Specifications

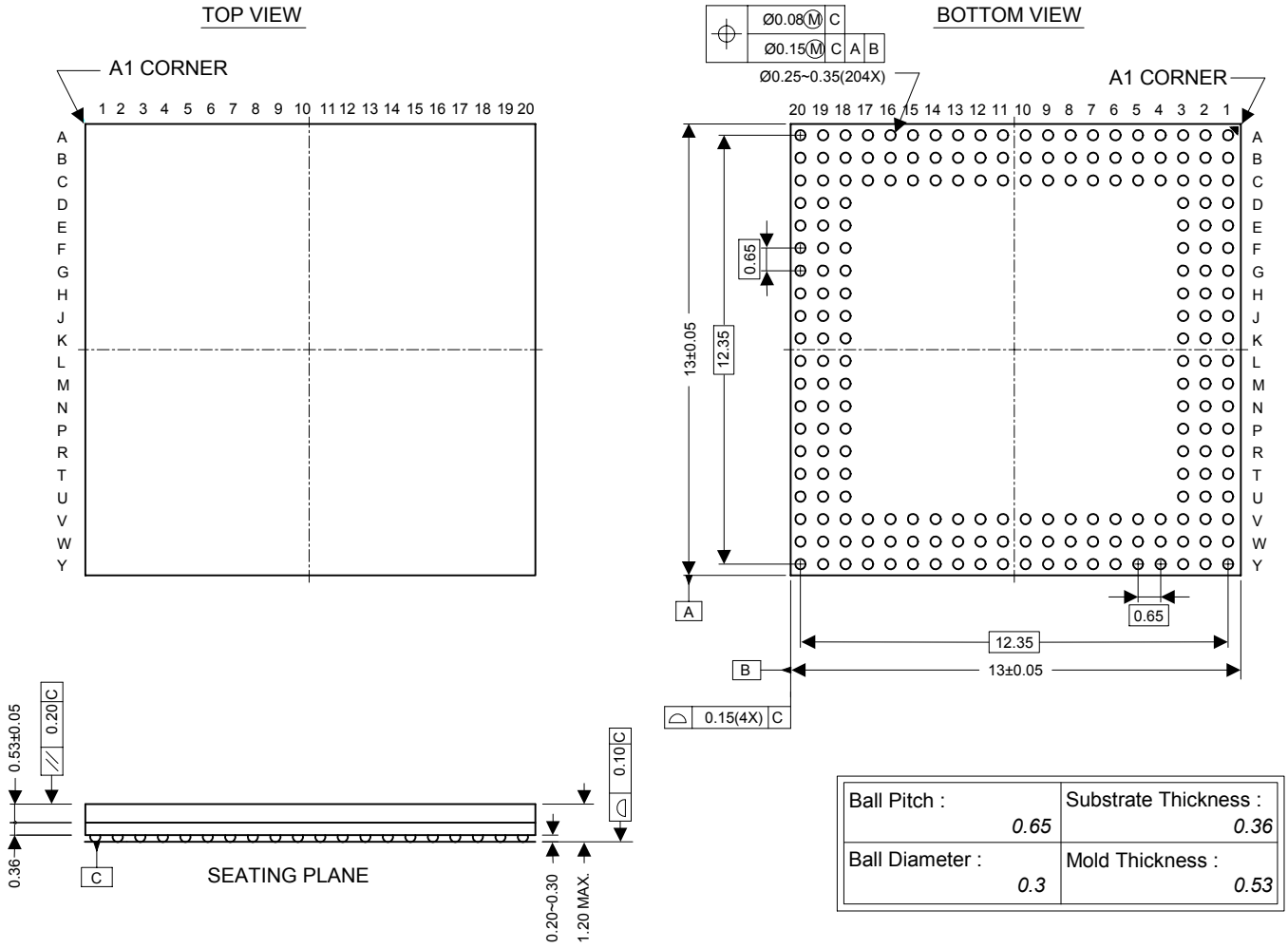


Figure 17. 204-Ball TFBGA Package

204-Ball TFBGA Ball Listing

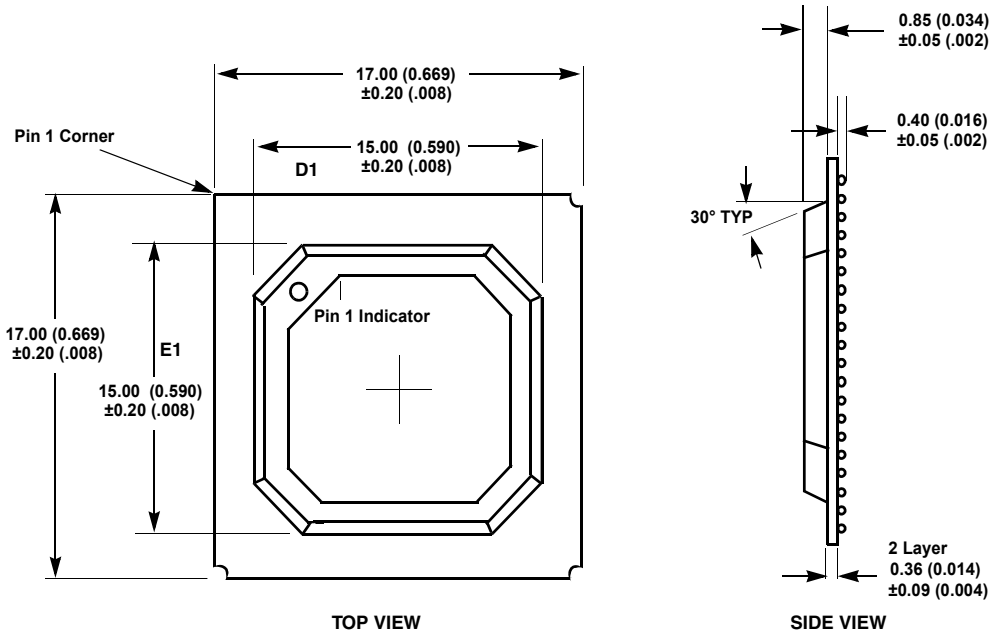
The list is ordered by ball location.

Table 21. 204-Ball TFBGA Ball Listing

Ball Location	Name	Strength†	Reset State	Type	Description
A1	VDDIO			Pad power	Digital I/O power, 3.3 V
A2	EXPCLK	1		I	Expansion clock input
A3	nCS[3]	1	High	O	Chip select 3
A4	nCS[1]	1	High	O	Chip select 1
A5	nMWE/nSDWE	1	High	O	ROM, expansion write enable/ SDRAM write enable control signal
A6	SDQM[2]	2	Low	O	SDRAM byte lane mask
A7	nSDCS[1]	1	High	O	SDRAM chip select 2
A8	DD[2]	1	Low	O	LCD serial display data
A9	FRM	1	Low	O	LCD frame synchronization pulse
A10	CL[1]	1	Low	O	LCD line clock
A11	VSSCORE			Core ground	Core ground
A12	D[1]	1	Low	I/O	Data I/O
A13	A[2]	2	Low	O	System byte address
A14	D[4]	1	Low	I/O	Data I/O
A15	A[5]	1	Low	O	System byte address
A16	nPWRFL			I	Power fail sense input
A17	MOSCOUT			O	Main oscillator out
A18	VSSIO			Pad ground	I/O ground
A19	VSSIO			Pad ground	I/O ground
A20	VSSIO			Pad ground	I/O ground
B1	WORD	1	Low	O	Word access select output
B2	VDDIO			Pad power	Digital I/O power, 3.3 V
B3	nCS[5]	1	Low	O	Chip select 5
B4	nCS[2]	1	High	O	Chip select 2
B5	nMOE/nSDCAS	1	High	O	ROM, expansion OP enable/SDRAM CAS control signal
B6	SDCKE	2	Low	O	SDRAM clock enable output
B7	nSDCS[0]	1	High	O	SDRAM chip select 0

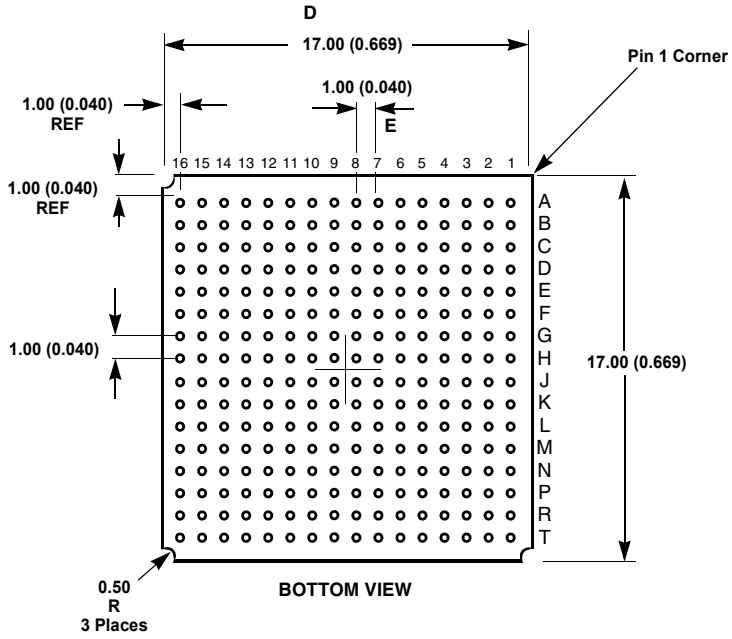
Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
V2	VSSIO			Pad ground	I/O ground
V3	VSSIO			Pad ground	I/O ground
V4	PD[7]/SDQM[1]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
V5	PD[4]	1	Low	I/O	GPIO port D
V6	PD[2]	1	Low	I/O	GPIO port D
V7	SSICLK	1	Input‡	I/O	DAI/CODEC/SSI2 serial clock
V8	SSIRXDA			I/O	DAI/CODEC/SSI2 serial data input
V9	nADCCS	1	High	O	SSI1 ADC chip select
V10	VDDIO			Pad power	Digital I/O power, 3.3V
V11	ADCCLK	1	Low	O	SSI1 ADC serial clock
V12	COL[7]	1	High	O	Keyboard scanner column drive
V13	COL[4]	1	High	O	Keyboard scanner column drive
V14	TCLK			I	JTAG clock
V15	BUZ	1	Low	O	Buzzer drive output
V16	D[29]	1	Low	I/O	Data I/O
V17	A[26]/DRA[1]	2	Low	O	System byte address / SDRAM address
V18	VDDIO			Pad power	Digital I/O power, 3.3 V
V19	VDDIO			Pad power	Digital I/O power, 3.3 V
V20	A[24]/DRA[3]	‘	Low	O	System byte address / SDRAM address
W1	VSSIO			Pad ground	I/O ground
W2	VSSIO			Pad ground	I/O ground
W3	VSSIO			Pad ground	I/O ground
W4	PD[6]/SDQM[0]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
W5	TMS	with p/u*		I	JTAG mode select
W6	PD[1]	1	Low	I/O	GPIO port D
W7	SSITXFR	1	Low	I/O	DAI/CODEC/SSI2 frame sync
W8	SSIRXFR	1	Input‡	I/O	DAI/CODEC/SSI2 frame sync
W9	VSSCORE			Core Ground	Core Ground
W10	DRIVE[1]	2	High / Low	I/O	PWM drive output



TOP VIEW

SIDE VIEW



BOTTOM VIEW

JEDEC #: MO-151
Ball Diameter: 0.50 mm ± 0.10 mm
17 ¥ 17 ¥ 1.61 mm body

Table V. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
M7	SSITXFR	I/O	MCP/CODEC/SSI2 frame sync
M8	DRIVE[1]	I/O	PWM drive output
M9	FB[0]	I	PWM feedback input
M10	COL[0]	O	Keyboard scanner column drive
M11	D[27]	I/O	Data I/O
M12	VSSIO	Pad ground	I/O ground
M13	A[23]/DRA[4]	O	System byte address / SDRAM address
M14	VDDIO	Pad power	Digital I/O power, 3.3V
M15	A[20]/DRA[7]	O	System byte address / SDRAM address
M16	D[21]	I/O	Data I/O
N1	nEXTFIQ	I	External fast interrupt input
N2	PE[1]/BOOTSEL[1]	I	GPIO port E / boot mode select
N3	VSSIO	Pad ground	I/O ground
N4	VDDIO	Pad power	Digital I/O power, 3.3V
N5	PD[5]	I/O	GPIO port D
N6	PD[2]	I/O	GPIO port D
N7	SSIRXDA	I/O	MCP/CODEC/SSI2 serial data input
N8	ADCCLK	O	SSI1 ADC serial clock
N9	SMPCLK	O	SSI1 ADC sample clock
N10	COL[2]	O	Keyboard scanner column drive
N11	D[29]	I/O	Data I/O
N12	D[26]	I/O	Data I/O
N13	HALFWORD	O	Halfword access select output
N14	VSSIO	Pad ground	I/O ground
N15	D[22]	I/O	Data I/O
N16	D[23]	I/O	Data I/O
P1	VSSRTC	RTC ground	Real time clock ground
P2	RTCOUT	O	Real time clock oscillator output
P3	VSSIO	Pad ground	I/O ground
P4	VSSIO	Pad ground	I/O ground
P5	VDDIO	Pad power	Digital I/O power, 3.3V
P6	VSSIO	Pad ground	I/O ground
P7	VSSIO	Pad ground	I/O ground
P8	VDDIO	Pad power	Digital I/O power, 3.3V
P9	VSSIO	Pad ground	I/O ground
P10	VDDIO	Pad power	Digital I/O power, 3.3V
P11	VSSIO	Pad ground	I/O ground
P12	VSSIO	Pad ground	I/O ground
P13	VDDIO	Pad power	Digital I/O power
P14	VSSIO	Pad ground	I/O ground
P15	D[24]	I/O	Data I/O
P16	VDDIO	Pad power	Digital I/O power, 3.3V
R1	RTCIN	I/O	Real time clock oscillator input
R2	VDDIO	Pad power	Digital I/O power, 3.3V
R3	PD[4]	I/O	GPIO port D
R4	PD[1]	I/O	GPIO port D
R5	SSITXDA	O	MCP/CODEC/SSI2 serial data output
R6	nADCCS	O	SSI1 ADC chip select

Table V. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
R7	VDDIO	Pad power	Digital I/O power, 3.3V
R8	ADCOUT	O	SSI1 ADC serial data output
R9	COL[7]	O	Keyboard scanner column drive
R10	COL[3]	O	Keyboard scanner column drive
R11	COL[1]	O	Keyboard scanner column drive
R12	D[30]	I/O	Data I/O
R13	A[27]/DRA[0]	O	System byte address / SDRAM address
R14	A[25]/DRA[2]	O	System byte address / SDRAM address
R15	VDDIO	Pad power	Digital I/O power, 3.3V
R16	A[24]/DRA[3]	O	System byte address / SDRAM address
T1	VDDRTC	RTC power	Real time clock power, 2.5V
T2	PD[7]/SDQM[1]	I/O	GPIO port D / SDRAM byte lane mask
T3	PD[6]/SDQM[0]	I/O	GPIO port D / SDRAM byte lane mask
T4	PD[3]	I/O	GPIO port D
T5	SSICLK	I/O	MCP/CODEC/SSI2 serial clock
T6	SSIRXFR	–	MCP/CODEC/SSI2 frame sync
T7	VDDCORE	Core power	Core power, 2.5V
T8	DRIVE[0]	I/O	PWM drive output
T9	FB[1]	I	PWM feedback input
T10	COL[5]	O	Keyboard scanner column drive
T11	VDDIO	Pad power	Digital I/O power, 3.3V
T12	BUZ	O	Buzzer drive output
T13	D[28]	I/O	Data I/O
T14	A[26]/DRA[1]	O	System byte address / SDRAM address
T15	D[25]	I/O	Data I/O
T16	VSSIO	Pad ground	I/O ground

Table W. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
44	T3	N1	nEXTFIQ	I	79
45	R1	L5	PE[2]/CLKSEL	I/O	80
46	R2	N2	PE[1]/BOOTSEL1	I/O	83
47	T1	M4	PE[0]/BOOTSEL0	I/O	86
53	T2	T2	PD[7]/SDQM[1]	I/O	89
54	V4	T3	PD[6/SDQM[0]]	I/O	92
55	W4	N5	PD[5]	I/O	95
56	Y4	R3	PD[4]	I/O	98
59	V5	T4	PD[3]	I/O	101
60	W5	N6	PD[2]	I/O	104
61	Y5	R4	PD[1]	I/O	107
62	V6	L7	PD[0]/LEDFLSH	O	110
68	W6	T6	SSIRXFR	I/O	122
69	Y6	K8	ADCIN	I	125
70	W8	R6	nADCCS	O	126
75	Y8	M8	DRIVE1	I/O	128
76	V9	T8	DRIVE0	I/O	131
77	W10	N8	ADCCLK	O	134
78	Y10	R8	ADCOUT	O	136
79	V11	N9	SMPCLK	O	138
80	W11	T9	FB1	I	140
82	Y11	M9	FB0	I	141
83	Y12	R9	COL7	O	142
84	W12	L9	COL6	O	144
85	V12	T10	COL5	O	146
86	Y13	K9	COL4	O	148
87	W13	R10	COL3	O	150
88	V13	N10	COL2	O	152
91	Y14	R11	COL1	O	154
92	W14	M10	COL0	O	156
93	A1	T12	BUZ	O	158
94	V14	L10	D[31]	I/O	160
95	Y15	R12	D[30]	I/O	163
96	W15	N11	D[29]	I/O	166
97	V15	T13	D[28]	I/O	169
99	Y16	R13	A[27]/DRA[0]	Out	172
100	W16	M11	D[27]	I/O	174
101	V16	T14	A[26]/DRA[1]	O	177

Table W. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
148	H18	G11	A[7]	O	274
150	F20	D15	D[7]	I/O	276
151	G19	F13	nBATCHG	I	279
152	E20	C16	nEXTPWR	I	280
153	F19	F12	BATOK	I	281
154	G18	C15	nPOR	I	282
155	D20	E13	nMEDCHG/nBROM	I	283
156	F18	B16	nURESET	I	284
161	D19	B14	WAKEUP	I	285
162	E19	D11	nPWRFL	I	286
163	C19	A13	A[6]	O	287
164	C20	F10	D[6]	I/O	289
165	E18	B13	A[5]	O	292
166	B20	E10	D[5]	I/O	294
169	B16	B12	A[4]	O	297
170	A16	D10	D[4]	I/O	299
171	C15	A11	A[3]	O	302
172	B15	G9	D[3]	I/O	304
173	A15	B11	A[2]	O	307
175	C14	A10	D[2]	I/O	309
176	B14	F9	A[1]	O	312
177	A14	B10	D[1]	I/O	314
178	C13	E9	A[0]	O	317
179	B13	A9	D[0]	I/O	319
184	A13	D8	CL2	O	322
185	C12	B8	CL1	O	324
186	B12	E8	FRM	O	326
187	A12	A7	M	O	328
188	C11	F8	DD[3]	I/O	330
189	B11	B7	DD[2]	I/O	333
191	B10	A6	DD[1]	I/O	336
192	A10	G8	DD[0]	I/O	339
193	A9	B6	nSDCS[1]	O	342
194	B9	D7	nSDCS[0]	O	344
195	C9	A5	SDQM[3]	I/O	346
196	A8	E7	SDQM[2]	I/O	349
199	B8	F7	SDCKE	I/O	352
200	C8	A4	SDCLK	I/O	355

CONVENTIONS

This section presents acronyms, abbreviations, units of measurement, and conventions used in this data sheet.

Acronyms and Abbreviations

Table X lists abbreviations and acronyms used in this data sheet.

Table X. Acronyms and Abbreviations

Acronym/ Abbreviation	Definition
A/D	analog-to-digital
ADC	analog-to-digital converter
CODEC	coder / decoder
D/A	digital-to-analog
DMA	direct-memory access
EPB	embedded peripheral bus
FCS	frame check sequence
FIFO	first in / first out
FIQ	fast interrupt request
GPIO	general purpose I/O
ICT	in circuit test
IR	infrared
IRQ	standard interrupt request
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	liquid crystal display
LED	light-emitting diode
LQFP	low profile quad flat pack
LSB	least significant bit
MIPS	millions of instructions per second
MMU	memory management unit
MSB	most significant bit
PBGA	plastic ball grid array
PCB	printed circuit board
PDA	personal digital assistant
PLL	phase locked loop
p/u	pull-up resistor
RISC	reduced instruction set computer
RTC	Real-Time Clock
SIR	slow (9600–115.2 kbps) infrared
SRAM	static random access memory
SSI	synchronous serial interface

Table X. Acronyms and Abbreviations (Continued)

Acronym/ Abbreviation	Definition
TAP	test access port
TLB	translation lookaside buffer
UART	universal asynchronous receiver

Units of Measurement

Table Y. Unit of Measurement

Symbol	Unit of Measure
°C	degree Celsius
fs	sample frequency
Hz	hertz (cycle per second)
kbps	kilobits per second
KB	kilobyte (1,024 bytes)
kHz	kilohertz
kΩ	kilohm
Mbps	megabits (1,048,576 bits) per second
MB	megabyte (1,048,576 bytes)
MBps	megabytes per second
MHz	megahertz (1,000 kilohertz)
µA	microampere
µF	microfarad
µW	microwatt
µs	microsecond (1,000 nanoseconds)
mA	milliampere
mW	milliwatt
ms	millisecond (1,000 microseconds)
ns	nanosecond
V	volt
W	watt

Ordering Information

Model	Temperature	Package
EP7311-CB	0 to +70 °C	256-pin PBGA, 17mm X 17mm
EP7311-CB-90 (90 MHz)		
EP7311-IB	-40 to +85 °C.	
EP7311-IB-90 (90 MHz)		
EP7311-CV	0 to +70 °C	208-pin LQFP.
EP7311-IV	-40 to +85 °C.	
EP7311-CR	0 to +70 °C	204-pin TFBGA, 13mm X 13mm.
EP7311-CR-90 (90 MHz)		

Environmental, Manufacturing, & Handling Information

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
EP7311-CB	225 °C	3	7 Days
EP7311-CB-90 (90 MHz)			
EP7311-IB			
EP7311-IB-90 (90 MHz)			
EP7311-CV			
EP7311-IV			
EP7311-CR			
EP7311-CR-90 (90 MHz)			

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.