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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM7TDMI
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	74MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	208-LQFP
Supplier Device Package	208-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep7311-cv

FEATURES *(cont)*

- LCD controller
  - — Interfaces directly to a single-scan panel monochrome STN LCD
  - — Interfaces to a single-scan panel color STN LCD with minimal external glue logic
- Full JTAG boundary scan and Embedded ICE® support
- Integrated Peripheral Interfaces
  - — 32-bit SDRAM Interface up to 2 external banks
  - — 8/32/16-bit SRAM/FLASH/ROM Interface
  - — Multimedia Codec Port
  - — Two Synchronous Serial Interfaces (SSI1, SSI2)
  - — CODEC Sound Interface
  - — 8×8 Keypad Scanner
  - — 27 General Purpose Input/Output pins
  - — Dedicated LED flasher pin from the RTC
- Internal Peripherals
  - — Two 16550 compatible UARTs
  - — IrDA Interface
  - — Two PWM Interfaces
  - — Real-time Clock
  - — Two general purpose 16-bit timers
  - — Interrupt Controller
  - — Boot ROM
- Package
  - — 208-Pin LQFP
  - — 256-Ball PBGA
  - — 204-Ball TFBGA
- The fully static EP7311 is optimized for low power dissipation and is fabricated on a 0.25 micron CMOS process
- Development Kits
  - — EDB7312: Development Kit with color STN LCD on board.
  - — EDB7312-LW: EDB7312 with Lynuxworks' BlueCat Linux Tools and software for Windows host (free 30 day BlueCat support from Lynuxworks).
  - — EDB7312-LL: EDB7312 with Lynuxworks' BlueCat Linux Tools and software for Linux host (free 30 day BlueCat support from Lynuxworks).

*Note: * BlueCat available separately through Lynuxworks only.*
** Use the EDB7312 Development Kit for all the EP73xx devices.*

OVERVIEW *(cont.)*

The EP7311 is designed for low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states: operating, idle and standby.

One of its notable features is MaverickKey unique IDs. These are factory programmed IDs in response to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs consist of two registers, one 32-bit series register and one random 128-bit register that may be used by an OEM for an authentication mechanism.

Simply by adding desired memory and peripherals to the highly integrated EP7311 completes a low-power system solution. All necessary interface logic is integrated on-chip.

Processor Core - ARM720T

The EP7311 incorporates an ARM 32-bit RISC microcontroller that controls a wide range of on-chip peripherals. The processor utilizes a three-stage pipeline consisting of fetch, decode and execute stages. Key features include:

- ARM (32-bit) and Thumb (16-bit compressed) instruction sets
- Enhanced MMU for Microsoft Windows CE and other operating systems
- 8 KB of 4-way set-associative cache.
- Translation Look Aside Buffers with 64 Translated Entries

Power Management

The EP7311 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V allowing the device to achieve a performance level equivalent to 60 MIPS. The device has three basic power states:

- Operating — This state is the full performance state. All the clocks and peripheral logic are enabled.
- Idle — This state is the same as the Operating State, except the CPU clock is halted while waiting for an event such as a key press.
- Standby — This state is equivalent to the computer being switched off (no display), and the main oscillator shut down. An event such as a key press can wake-up the processor.

Pin Mnemonic	I/O	Pin Description
BATOK	I	Battery ok input
nEXTPWR	I	External power supply sense input
nPWRFL	I	Power fail sense input
nBATCHG	I	Battery changed sense input

Table A. Power Management Pin Assignments

MaverickKey™ Unique ID

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

Both a specific 32-bit ID as well as a 128-bit random ID is programmed into the EP7311 through the use of laser probing technology. These IDs can then be used to match secure copyrighted content with the ID of the target device the EP7311 is powering, and then deliver the copyrighted information over a secure connection. In addition, secure transactions can benefit by also matching device IDs to server IDs. MaverickKey IDs provide a level of hardware security required for today's Internet appliances.

Memory Interfaces

There are two main external memory interfaces. The first one is the ROM/SRAM/FLASH-style interface that has programmable wait-state timings and includes burst-mode capability, with six chip selects decoding six 256 MB sections of addressable space. For maximum flexibility, each bank can be specified to be 8-, 16-, or 32-bits wide. This allows the use of 8-bit-wide boot ROM options to minimize overall system cost. The on-chip boot ROM can be used in product manufacturing to serially download system code into system FLASH memory. To further minimize system memory requirements and cost, the ARM Thumb instruction set is supported, providing for the use of high-speed 32-bit operations in 16-bit op-codes and yielding industry-leading code density.

Pin Mnemonic		I/O	Pin Description
nCS[5:0]		O	Chip select out
A[27:0]		O	Address output
D[31:0]		I/O	Data I/O
nMOE/nSDCAS	(Note)	O	ROM expansion OP enable
nMWE/nSDWE	(Note)	O	ROM expansion write enable
HALFWORD		O	Halfword access select output
WORD		O	Word access select output
WRITE/nSDRAS	(Note)	O	Transfer direction

Table B. Static Memory Interface Pin Assignments

Note: Pins are multiplexed. See Table S on page 11 for more information.

The second is the programmable 16- or 32-bit-wide SDRAM interface that allows direct connection of up to two banks of SDRAM, totaling 512 Mb. To assure the lowest possible power consumption, the EP7311 supports self-refresh SDRAMs, which are placed in a low-power state by the device when it enters the low-power Standby State.

Pin Mnemonic	I/O	Pin Description
SDCLK	O	SDRAM clock output
SDCKE	O	SDRAM clock enable output
nSDCS[1:0]	O	SDRAM chip select out
WRITE/nSDRAS (Note 2)	O	SDRAM RAS signal output
nMOE/nSDCAS (Note 2)	O	SDRAM CAS control signal
nMWE/nSDWE (Note 2)	O	SDRAM write enable control signal
A[27:15]/DRA[0:12] (Note 1)	O	SDRAM address
A[14:13]/DRA[12:14]	O	SDRAM internal bank select
PD[7:6]/SDQM[1:0] (Note 2)	I/O	SDRAM byte lane mask
SDQM[3:2]	O	SDRAM byte lane mask
D[31:0]	I/O	Data I/O

Table C. SDRAM Interface Pin Assignments

Note: 1. Pins A[27:13] map to DRA[0:14] respectively. (i.e. A[27}/DRA[0}, A[26}/DRA[1], etc.) This is to balance the load for large memory systems.
2. Pins are multiplexed. See Table S on page 11 for more information.

Digital Audio Capability

The EP7311 uses its powerful 32-bit RISC processing engine to implement audio decompression algorithms in software. The nature of the on-board RISC processor, and the availability of efficient C-compilers and other software development tools, ensures that a wide range of audio decompression algorithms can easily be ported to and run on the EP7311

Universal Asynchronous Receiver/Transmitters (UARTs)

The EP7311 includes two 16550-type UARTs for RS-232 serial communications, both of which have two 16-byte FIFOs for receiving and transmitting data. The UARTs support bit rates up to 115.2 kbps. An IrDA SIR protocol encoder/decoder can be optionally switched into the RX/TX signals to/from UART 1 to enable these signals to drive an infrared communication interface directly.

Pin Mnemonic	I/O	Pin Description
TXD[1]	O	UART 1 transmit
RXD[1]	I	UART 1 receive
CTS	I	UART 1 clear to send
DCD	I	UART 1 data carrier detect
DSR	I	UART 1 data set ready
TXD[2]	O	UART 2 transmit
RXD[2]	I	UART 2 receive
LEDDRV	O	Infrared LED drive output
PHDIN	I	Photo diode input

Table D. Universal Asynchronous Receiver/Transmitters Pin Assignments

Multimedia Codec Port (MCP)

The Multimedia Codec Port provides access to an audio codec, a telecom codec, a touchscreen interface, four general purpose analog-to-digital converter inputs, and ten programmable digital I/O lines.

Pin Mnemonic	I/O	Pin Description
SIBCLK	O	Serial bit clock
SIBDOUT	O	Serial data out
SIBDIN	I	Serial data in
SIBSYNC	O	Sample clock

Table E. MCP Interface Pin Assignments

Note: See Table R on page 11 for information on pin multiplexes.

CODEC Interface

The EP7311 includes an interface to telephony-type CODECs for easy integration into voice-over-IP and other voice communications systems. The CODEC interface is multiplexed to the same pins as the MCP and SSI2.

Pin Mnemonic	I/O	Pin Description
PCMCLK	O	Serial bit clock
PCMOUT	O	Serial data out
PCMIN	I	Serial data in
PCMSYNC	O	Frame sync

Table F. CODEC Interface Pin Assignments

Note: See Table R on page 11 for information on pin multiplexes.

SSI2 Interface

An additional SPI/Microwire1-compatible interface is available for both master and slave mode communications. The SSI2 unit shares the same pins as the MCP and CODEC interfaces through a multiplexer.

- Synchronous clock speeds of up to 512 kHz
- Separate 16 entry TX and RX half-word wide FIFOs
- Half empty/full interrupts for FIFOs
- Separate RX and TX frame sync signals for asymmetric traffic

Pin Mnemonic	I/O	Pin Description
SSICLK	I/O	Serial bit clock
SSITXDA	O	Serial data out
SSIRXDA	I	Serial data in
SSITXFR	I/O	Transmit frame sync
SSIRXFR	I/O	Receive frame sync

Table G. SSI2 Interface Pin Assignments

Note: See Table R on page 11 for information on pin multiplexes.

Synchronous Serial Interface

- ADC (SSI) Interface: Master mode only; SPI and Microwire1-compatible (128 kbps operation)
- Selectable serial clock polarity

Pin Mnemonic	I/O	Pin Description
ADCLK	O	SSI1 ADC serial clock
ADCIN	I	SSI1 ADC serial input
ADCOUT	O	SSI1 ADC serial output
nADCCS	O	SSI1 ADC chip select
SMPCLK	O	SSI1 ADC sample clock

Table H. Serial Interface Pin Assignments

LCD Controller

A DMA address generator is provided that fetches video display data for the LCD controller from memory. The display frame buffer start address is programmable, allowing the LCD frame buffer to be in SDRAM, internal SRAM or external SRAM.

- Interfaces directly to a single-scan panel monochrome STN LCD
- Interfaces to a single-scan panel color STN LCD with minimal external glue logic
- Panel width size is programmable from 32 to 1024 pixels in 16-pixel increments
- Video frame buffer size programmable up to 128 KB
- Bits per pixel of 1, 2, or 4 bits

Pin Mnemonic	I/O	Pin Description
CL1	O	LCD line clock
CL2	O	LCD pixel clock out
DD[3:0]	O	LCD serial display data bus
FRM	O	LCD frame synchronization pulse
M	O	LCD AC bias drive

Table I. LCD Interface Pin Assignments

Pin Multiplexing

The following table shows the pin multiplexing of the MCP, SSI2 and the CODEC. The selection between SSI2 and the CODEC is controlled by the state of the SERSEL bit in SYSCON2. The choice between the SSI2, CODEC, and the MCP is controlled by the MCPSEL bit in SYSCON3 (see the EP73xx User's Manual for more information).

Pin Mnemonic	I/O	MCP	SSI2	CODEC
SSICLK	I/O	SIBCLK	SSICLK	PCMCLK
SSITXDA	O	SIBDOUT	SSITXDA	PCMOUT
SSIRXDA	I	SIBDIN	SSIRXDA	PCMIN
SSITXFR	I/O	SIBSYNC	SSITXFR	PCMSYNC
SSIRXFR	I	p/u	SSIRXFR	p/u
BUZ	O			

Table R. MCP/SSI2/CODEC Pin Multiplexing

The following table shows the pins that have been multiplexed in the EP7311.

Signal	Block	Signal	Block
nMOE	Static Memory	nSDCAS	SDRAM
nMWE	Static Memory	nSDWE	SDRAM
WRITE	Static Memory	nSDRAS	SDRAM
A[27:15]	Static Memory	DRA[0:12]	SDRAM
A[14:13]	Static Memory	DRA[13:14]	SDRAM
PD[7:6]	GPIO	SDQM[1:0]	SDRAM
RUN	System Configuration	CLKEN	System Configuration
nMEDCHG	Interrupt Controller	nBROM	Boot ROM select
PD[0]	GPIO	LEDFLSH	LED Flasher
PE[1:0]	GPIO	BOOTSEL[1:0]	System Configuration
PE[2]	GPIO	CLKSEL	System Configuration

Table S. Pin Multiplexing

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

DC Core, PLL, and RTC Supply Voltage	2.9 V
DC I/O Supply Voltage (Pad Ring)	3.6 V
DC Pad Input Current	±10 mA/pin; ±100 mA cumulative
Storage Temperature, No Power	–40°C to +125°C

Recommended Operating Conditions

DC core, PLL, and RTC Supply Voltage	2.5 V ± 0.2 V
DC I/O Supply Voltage (Pad Ring)	2.3 V - 3.5 V
DC Input / Output Voltage	O–I/O supply voltage
Operating Temperature	Extended -20°C to +70°C; Commercial 0°C to +70°C; Industrial -40°C to +85°C

DC Characteristics

All characteristics are specified at V_{DDCORE} = 2.5 V, V_{DDIO} = 3.3 V and V_{SS} = 0 V over an operating temperature of 0°C to +70°C for all frequencies of operation. The current consumption figures have test conditions specified per parameter."

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIH	CMOS input high voltage	$0.65 \times V_{DDIO}$	-	V_{DDIO} + 0.3	V	V_{DDIO} = 2.5 V
VIL	CMOS input low voltage	V_{SS} – 0.3	-	$0.25 \times V_{DDIO}$	V	V_{DDIO} = 2.5 V
VT+	Schmitt trigger positive going threshold	-	-	2.1	V	
VT-	Schmitt trigger negative going threshold	0.8	-	-	V	
Vhst	Schmitt trigger hysteresis	0.1	-	0.4	V	VIL to VIH
VOH	CMOS output high voltage[a] Output drive 1[a] Output drive 2[a]	V_{DD} – 0.2 2.5 2.5	- - -	- - -	V V V	IOH = 0.1 mA IOH = 4 mA IOH = 12 mA
VOL	CMOS output low voltage[a] Output drive 1[a] Output drive 2[a]	- - -	- - -	0.3 0.5 0.5	V V V	IOL = –0.1 mA IOL = –4 mA IOL = –12 mA
IIN	Input leakage current	-	-	1.0	µA	VIN = V_{DD} or GND
IOZ	Bidirectional 3-state leakage current[b c]	25	-	100	µA	VOUT = V_{DD} or GND
CIN	Input capacitance	8	-	10.0	pF	
COUT	Output capacitance	8	-	10.0	pF	

Timings

Timing Diagram Conventions

This data sheet contains timing diagrams. The following key explains the components used in these diagrams. Any variations are clearly labelled when they occur. Therefore, no additional meaning should be attached unless specifically stated.

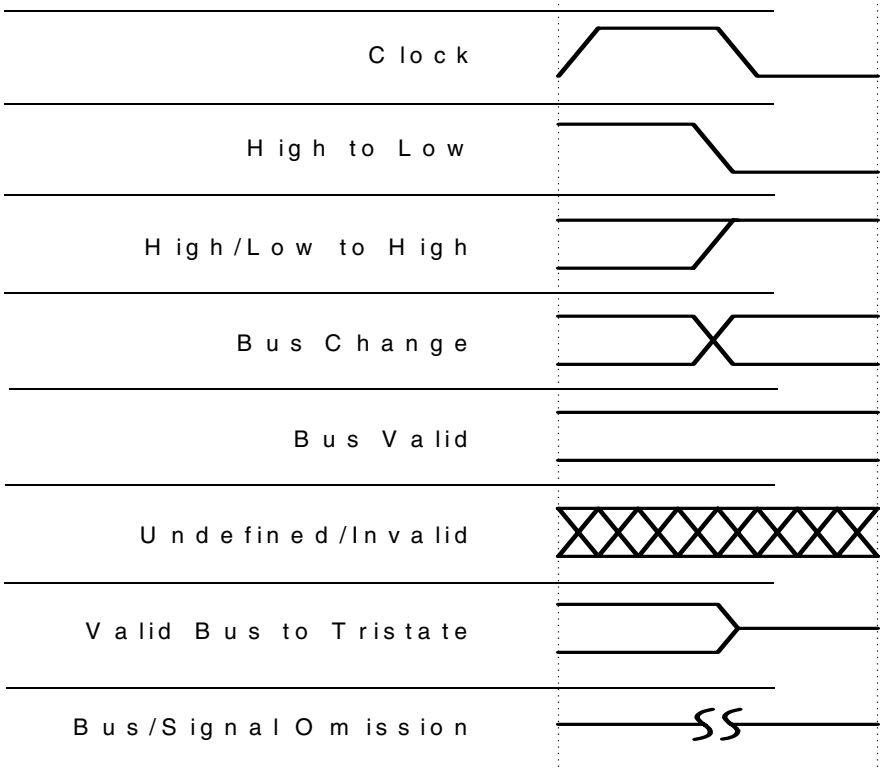

Figure 2. Legend for Timing Diagrams

Timing Conditions

Unless specified otherwise, the following conditions are true for all timing measurements. All characteristics are specified at V_{DDIO} = 3.1 - 3.5 V and V_{SS} = 0 V over an operating temperature of -40°C to +85°C. Pin loadings is 50 pF. The timing values are referenced to 1/2 V_{DD}.

Static Memory

Figure 7 through Figure 10 define the timings associated with all phases of the Static Memory. The following table contains the values for the timings of each of the Static Memory modes.

Parameter	Symbol	Min	Typ	Max	Unit
EXPCLK rising edge to nCS assert delay time	t_{CSd}	2	8	20	ns
EXPCLK falling edge to nCS deassert hold time	t_{CSh}	2	7	20	ns
EXPCLK rising edge to A assert delay time	t_{Ad}	4	9	16	ns
EXPCLK falling edge to A deassert hold time	t_{Ah}	3	10	19	ns
EXPCLK rising edge to nMWE assert delay time	t_{MWd}	3	6	10	ns
EXPCLK rising edge to nMWE deassert hold time	t_{MWh}	3	6	10	ns
EXPCLK falling edge to nMOE assert delay time	t_{MOEd}	3	7	10	ns
EXPCLK falling edge to nMOE deassert hold time	t_{MOEh}	2	7	10	ns
EXPCLK falling edge to HALFWORD deassert delay time	t_{HWd}	2	8	20	ns
EXPCLK falling edge to WORD assert delay time	t_{WDd}	2	8	16	ns
EXPCLK rising edge to data valid delay time	t_{Dv}	8	13	21	ns
EXPCLK falling edge to data invalid delay time	t_{Dnv}	6	15	30	ns
Data setup to EXPCLK falling edge time	t_{Ds}	-	-	1	ns
EXPCLK falling edge to data hold time	t_{Dh}	-	-	3	ns
EXPCLK rising edge to WRITE assert delay time	t_{WRd}	5	11	23	ns
EXPREADY setup to EXPCLK falling edge time	t_{EXs}	-	-	0	ns
EXPCLK falling edge to EXPREADY hold time	t_{EXh}	-	-	0	ns

Static Memory Single Write Cycle

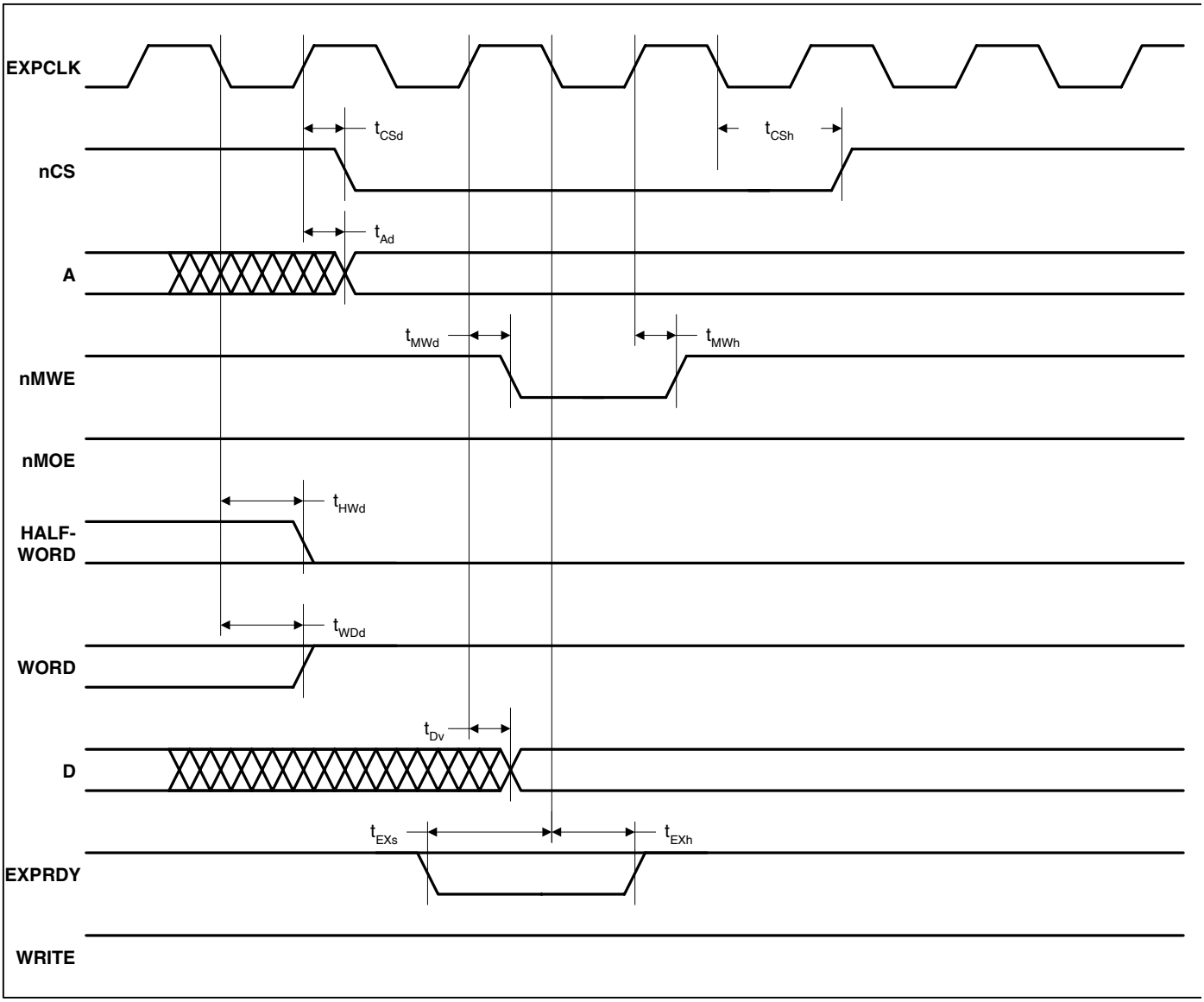

Figure 8. Static Memory Single Write Cycle Timing Measurement

Note: 1. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.

2. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.

3. Address, Data, Halfword, Word, and Write hold state until next cycle.

Static Memory Burst Read Cycle

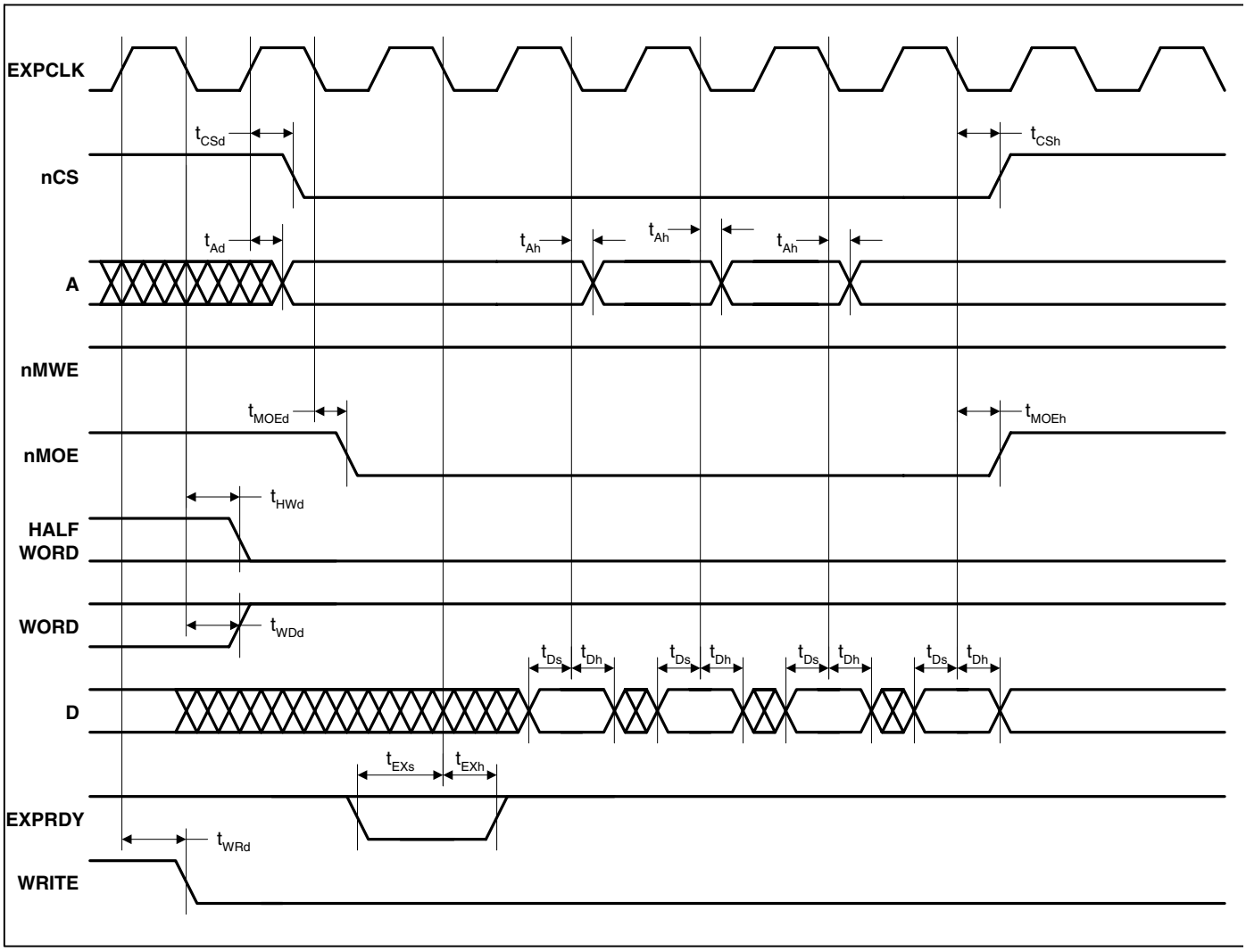

Figure 9. Static Memory Burst Read Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-0-0-0). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.
2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
3. Consecutive reads with sequential access enabled are identical except that the sequential access wait state field is used to determine the number of wait states, and no idle cycles are inserted between successive non-sequential ROM/expansion cycles. This improves performance so the SQAEN bit should always be set where possible.
4. Address, Halfword, Word, and Write hold state until next cycle.

SSI2 Interface

Parameter	Symbol	Min	Max	Unit
SSICLK period (slave mode)	t_{clk_per}	185	2050	ns
SSICLK high time	t_{clk_high}	925	1025	ns
SSICLK low time	t_{clk_low}	925	1025	ns
SSICLK rise/fall time	t_{clkrf}	3	18	ns
SSICLK rising edge to RX and/or TX frame sync high time	t_{FRd}	-	3	ns
SSICLK rising edge to RX and/or TX frame sync low time	t_{FRa}	-	8	ns
SSIRXFR and/or SSITXFR period	t_{FR_per}	960	990	ns
SSIRXDA setup to SSICLK falling edge time	t_{RXs}	3	7	ns
SSIRXDA hold from SSICLK falling edge time	t_{RXh}	3	7	ns
SSICLK rising edge to SSITXDA data valid delay time	t_{TXd}	-	2	ns
SSITXDA valid time	t_{TXv}	960	990	ns

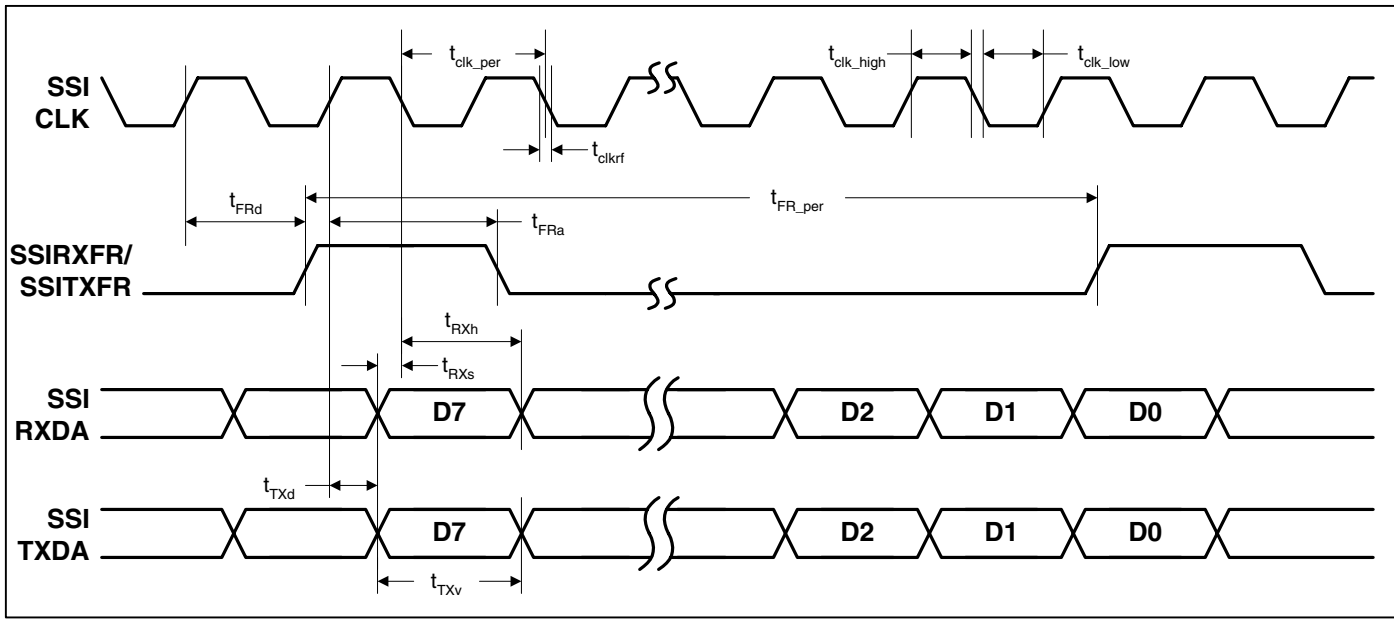

Figure 12. SSI2 Interface Timing Measurement

208-Pin LQFP Pin Diagram

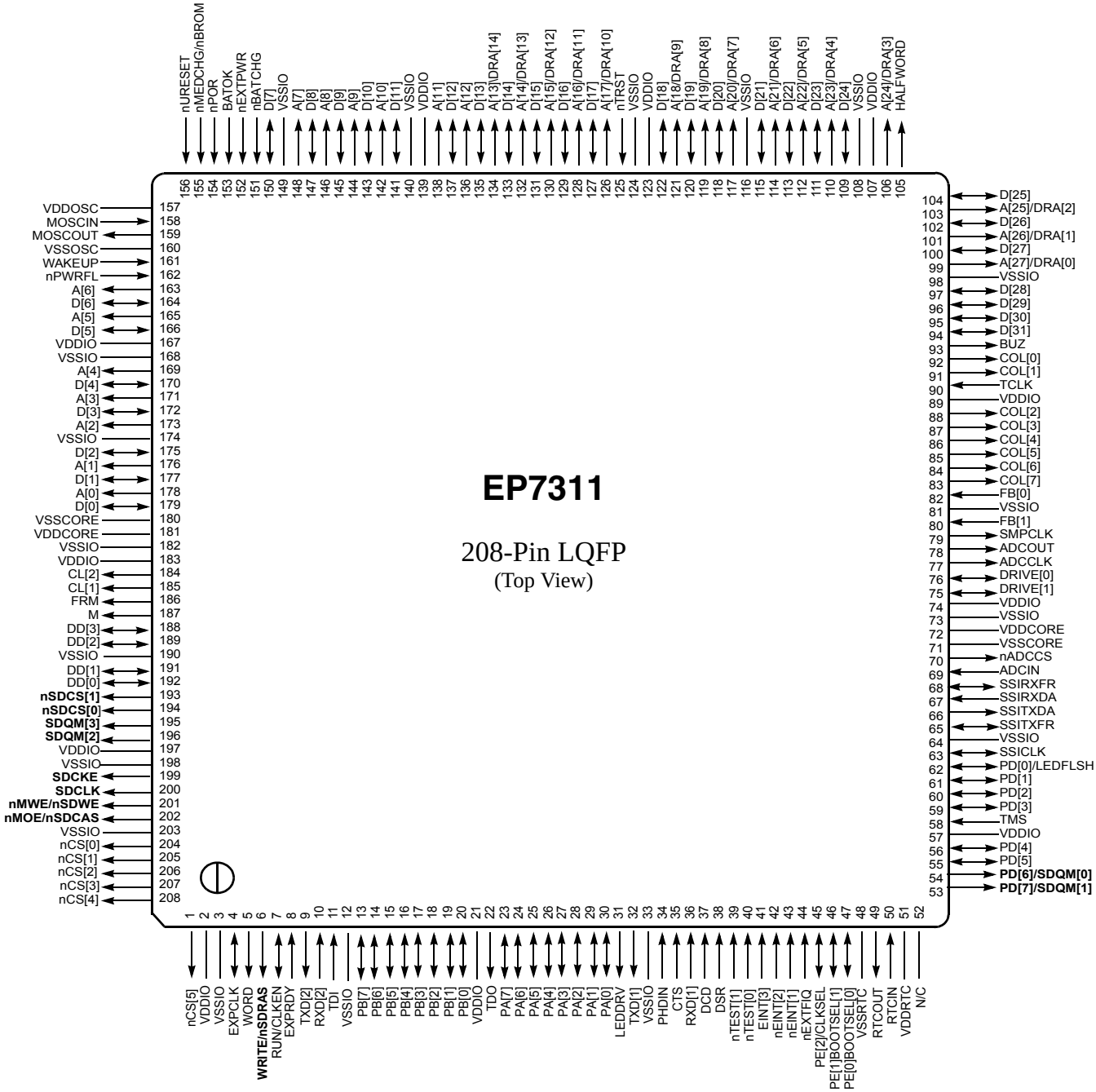

Figure 16. 208-Pin LQFP (Low Profile Quad Flat Pack) Pin Diagram

Note: 1. N/C should not be grounded but left as no connects.
2. Pin differences between the EP7211 and the EP7311 are bolded.

204-Ball TFBGA Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VDDIO	EXPCLK	nCS3	nCS1	nMWE/ nSDWE	SDQM2	nSDCS1	DD2	FRM	CL1	GNDCORE	D1	A2	D4	A5	nPWRFL	MOSCOUT	GNDIO	GNDIO	GNDIO	A
B	WORD	VDDIO	nCS5	nCS2	nMOE/ nSDCAS	SDCKE	nSDCS0	DD1	M	CL2	D0	A1	D3	A4	D6	WAKEUP	MOSCIN	GNDIO	GNDIO	nURESET	B
C	RUN/ CLKEN	EXPRDY	VDDIO	nCS4	nCS0	SDCLK	SDQM3	DD0	DD3	VDDCORE	A0	D2	A3	D5	A6	GNDOSC	VDDOSC	GNDIO	BATOK	nPOR	C
D	PB7	RXD2	VDDIO															GNDIO	nBATCHG	A7	D
E	PB4	TXD2	WRITE/ nSDRAS															nMEDCHG /nBROM	nEXTPWR	D9	E
F	PB3	PB6	TDI															D7	A8	D10	F
G	PB1/ PRDY2	PB2	PB5															D8	A9	D11	G
H	PA7	TDO	PB0/ PRDY1															A10	D12	A12	H
J	PA4	PA5	PA6															A11	D13	A13/ DRA14	J
K	PA1	PA2	VDDIO															D14	A14/ DRA13	D15	K
L	TXD1	LEDDRV	PA3															VDDIO	D16	A16/ DRA11	L
M	RXD1	CTS	PA0															A15/ DRA12	A17/ DRA10	nTRST	M
N	DSR	nTEST1	PHDIN															D17	D19	A18/ DRA9	N
P	EINT3	nEINT2	DCD															D18	A20/ DRA7	D20	P
R	nEXTFIQ	PE2/ CLKSEL	nTEST0															A19/ DRA8	D22	A21/ DRA6	R
T	PE1/ BOOT SEL1	PE0/ BOOT SEL0	nEINT1															D21	D23	A22/ DRA5	T
U	GNDRTC	RTCOUT	RTCIN															HALF WORD	D24	A23/ DRA4	U
V	VDDRTC	GNDIO	GNDIO	PD7/ SDQM1	PD4	PD2	SSICLK	SSIRXDA	nADCCS	VDDIO	ADCCLK	COL7	COL4	TCLK	BUZ	D29	A26/ DRA1	VDDIO	VDDIO	A24/ DRA3	V
W	GNDIO	GNDIO	GNDIO	PD6/SD QM0	TMS	PD1	SSITXFR	SSIRXFR	GNDCORE	DRIVE1	ADCOUT	FB0	COL5	COL2	COL0	D30	A27/ DRA0	D26	VDDIO	D25	W
Y	GNDIO	GNDIO	GNDIO	PD5	PD3	PD0/ LED FLSH	SSITXDA	ADCIN	VDDCORE	DRIVE0	SMPLCK	FB1	COL6	COL3	COL1	D31	D28	D27	A25/ DRA2	VDDIO	Y

204-Ball TFBGA Ball Listing

The list is ordered by ball location.

Table 21. 204-Ball TFBGA Ball Listing

Ball Location	Name	Strength†	Reset State	Type	Description
A1	VDDIO			Pad power	Digital I/O power, 3.3 V
A2	EXPCLK	1		I	Expansion clock input
A3	nCS[3]	1	High	O	Chip select 3
A4	nCS[1]	1	High	O	Chip select 1
A5	nMWE/nSDWE	1	High	O	ROM, expansion write enable/ SDRAM write enable control signal
A6	SDQM[2]	2	Low	O	SDRAM byte lane mask
A7	nSDCS[1]	1	High	O	SDRAM chip select 2
A8	DD[2]	1	Low	O	LCD serial display data
A9	FRM	1	Low	O	LCD frame synchronization pulse
A10	CL[1]	1	Low	O	LCD line clock
A11	VSSCORE			Core ground	Core ground
A12	D[1]	1	Low	I/O	Data I/O
A13	A[2]	2	Low	O	System byte address
A14	D[4]	1	Low	I/O	Data I/O
A15	A[5]	1	Low	O	System byte address
A16	nPWRFL			I	Power fail sense input
A17	MOSCOUT			O	Main oscillator out
A18	VSSIO			Pad ground	I/O ground
A19	VSSIO			Pad ground	I/O ground
A20	VSSIO			Pad ground	I/O ground
B1	WORD	1	Low	O	Word access select output
B2	VDDIO			Pad power	Digital I/O power, 3.3 V
B3	nCS[5]	1	Low	O	Chip select 5
B4	nCS[2]	1	High	O	Chip select 2
B5	nMOE/nSDCAS	1	High	O	ROM, expansion OP enable/SDRAM CAS control signal
B6	SDCKE	2	Low	O	SDRAM clock enable output
B7	nSDCS[0]	1	High	O	SDRAM chip select 0

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
W11	ADCOUT	1	Low	O	SSI1 ADC serial data output
W12	FB[0]			I	PWM feedback input
W13	COL[5]	1	High	O	Keyboard scanner column drive
W14	COL[2]	1	High	O	Keyboard scanner column drive
W15	COL[0]	1	High	O	Keyboard scanner column drive
W16	D[30]	1	Low	I/O	Data I/O
W17	A[27]/DRA[0]	2	Low	O	System byte address / SDRAM address
W18	D[26]	1	Low	I/O	Data I/O
W19	VDDIO			Pad power	Digital I/O power, 3.3V
W20	D[25]	1	Low	I/O	Data I/O
Y1	VSSIO			Pad ground	I/O ground
Y2	VSSIO			Pad ground	I/O ground
Y3	VSSIO			Pad ground	I/O ground
Y4	PD[5]	1	Low	I/O	GPIO port D
Y5	PD[3]	1	Low	I/O	GPIO port D
Y6	PD[0]/LEDFLSH	1	Low	I/O	GPIO port D / LED blinker output
Y7	SSITXDA	1	Low	O	DAI/CODEC/SSI2 serial data output
Y8	ADCIN			I	SSI1 ADC serial input
Y9	VDDCORE			Core power	Digital core power, 2.5V
Y10	DRIVE[0]	2	Input‡	I/O	PWM drive output
Y11	SMPCLK	1	Low	O	SSI1 ADC sample clock
Y12	FB[1]			I	PWM feedback input
Y13	COL[6]	1	High	O	Keyboard scanner column drive
Y14	COL[3]	1	High	O	Keyboard scanner column drive
Y15	COL[1]	1	High	O	Keyboard scanner column drive
Y16	D[31]	1	Low	I/O	Data I/O
Y17	D[28]	1	Low	I/O	Data I/O
Y18	D[27]	1	Low	I/O	Data I/O
Y19	A[25]/DRA[2]	2	Low	O	System byte address / SDRAM address

256-Ball PBGA Ball Listing

The list is ordered by ball location.

Table V. 256-Ball PBGA Ball Listing

Ball Location	Name	Type	Description
A1	VDDIO	Pad power	Digital I/O power, 3.3V
A2	nCS[4]	O	Chip select out
A3	nCS[1]	O	Chip select out
A4	SDCLK	O	SDRAM clock out
A5	SDQM[3]	O	SDRAM byte lane mask
A6	DD[1]	O	LCD serial display data
A7	M	O	LCD AC bias drive
A8	VDDIO	Pad power	Digital I/O power, 3.3V
A9	D[0]	I/O	Data I/O
A10	D[2]	I/O	Data I/O
A11	A[3]	O	System byte address
A12	VDDIO	Pad power	Digital I/O power, 3.3V
A13	A[6]	O	System byte address
A14	MOSCOUT	O	Main oscillator out
A15	VDDOSC	Oscillator power	Oscillator power in, 2.5V
A16	VSSIO	Pad ground	I/O ground
B1	nCS[5]	O	Chip select out
B2	VDDIO	Pad power	I/O ground
B3	nCS[3]	O	Chip select out
B4	nMOE/nSDCAS	O	ROM, expansion OP enable/SDRAM CAS control signal
B5	VDDIO	Pad power	Digital I/O power, 3.3V
B6	nSDCS[1]	O	SDRAM chip select out
B7	DD[2]	O	LCD serial display data
B8	CL[1]	O	LCD line clock
B9	VDDCORE	Core power	Digital core power, 2.5V
B10	D[1]	I/O	Data I/O
B11	A[2]	O	System byte address
B12	A[4]	O	System byte address
B13	A[5]	O	System byte address
B14	WAKEUP	I	System wake up input
B15	VDDIO	Pad power	Digital I/O power, 3.3V
B16	nURESET	I	User reset input
C1	VDDIO	Pad power	Digital I/O power, 3.3V
C2	EXPCLK	I	Expansion clock input
C3	VSSIO	Pad ground	I/O ground
C4	VDDIO	Pad power	Digital I/O power, 3.3V
C5	VSSIO	Pad ground	I/O ground
C6	VSSIO	Pad ground	I/O ground
C7	VSSIO	Pad ground	I/O ground
C8	VDDIO	Pad power	Digital I/O power, 3.3V
C9	VSSIO	Pad ground	I/O ground
C10	VSSIO	Pad ground	I/O ground
C11	VSSIO	Pad ground	I/O ground

Table V. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
C12	VDDIO	Pad power	Digital I/O power, 3.3V
C13	VSSIO	Pad ground	I/O ground
C14	VSSIO	Pad ground	I/O ground
C15	nPOR	I	Power-on reset input
C16	nEXTPWR	I	External power supply sense input
D1	WRITE/nSDRAS	O	Transfer direction / SDRAM RAS signal output
D2	EXPRDY	I	Expansion port ready input
D3	VSSIO	Pad ground	I/O ground
D4	VDDIO	Pad power	Digital I/O power, 3.3V
D5	nCS[2]	O	Chip select out
D6	nMWE/nSDWE	O	ROM, expansion write enable/ SDRAM write enable control signal
D7	nSDCS[0]	O	SDRAM chip select out
D8	CL[2]	O	LCD pixel clock out
D9	VSSRTC	Core ground	Real time clock ground
D10	D[4]	I/O	Data I/O
D11	nPWRFL	I	Power fail sense input
D12	MOSCIN	I	Main oscillator input
D13	VDDIO	Pad power	Digital I/O power, 3.3V
D14	VSSIO	Pad ground	I/O ground
D15	D[7]	I/O	Data I/O
D16	D[8]	I/O	Data I/O
E1	RXD[2]	I	UART 2 receive data input
E2	PB[7]	I	GPIO port B
E3	TDI	I	JTAG data input
E4	WORD	O	Word access select output
E5	VSSIO	Pad ground	I/O ground
E6	nCS[0]	O	Chip select out
E7	SDQM[2]	O	SDRAM byte lane mask
E8	FRM	O	LCD frame synchronization pulse
E9	A[0]	O	System byte address
E10	D[5]	I/O	Data I/O
E11	VSSOSC	Oscillator ground	PLL ground
E12	VSSIO	Pad ground	I/O ground
E13	nMEDCHG/nBROM	I	Media change interrupt input / internal ROM boot enable
E14	VDDIO	Pad power	Digital I/O power, 3.3V
E15	D[9]	I/O	Data I/O
E16	D[10]	I/O	Data I/O
F1	PB[5]	I	GPIO port B
F2	PB[3]	I	GPIO port B
F3	VSSIO	Pad ground	I/O ground
F4	TXD[2]	O	UART 2 transmit data output
F5	RUN/CLKEN	O	Run output / clock enable output
F6	VSSIO	Pad ground	I/O ground

JTAG Boundary Scan Signal Ordering

Table W. JTAG Boundary Scan Signal Ordering

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
1	B3	B1	nCS[5]	O	1
4	A2	C2	EXPCLK	I/O	3
5	B1	E4	WORD	O	6
6	E3	D1	WRITE/nSDRAS	O	8
7	C1	F5	RUN/CLKEN	O	10
8	C2	D2	EXPRDY	I	13
9	E2	F4	TXD2	O	14
10	D2	E1	RXD2	I	16
13	F3	E2	PB[7]	I/O	17
14	D1	G5	PB[6]	I/O	20
15	F2	F1	PB[5]	I/O	23
16	G3	G4	PB[4]	I/O	26
17	E1	F2	PB[3]	I/O	29
18	F1	H7	PB[2]	I/O	32
19	G2	G1	PB[1]/PRDY2	I/O	35
20	G1	H6	PB[0]/PRDY1	I/O	38
23	H3	H1	PA[7]	I/O	41
24	H1	H5	PA[6]	I/O	44
25	J3	H2	PA[5]	I/O	47
26	J2	H4	PA[4]	I/O	50
27	J1	J1	PA[3]	I/O	53
28	L3	J4	PA[2]	I/O	56
29	K2	J2	PA[1]	I/O	59
30	K1	J5	PA[0]	I/O	62
31	M3	K1	LEDDRV	O	65
32	L2	J6	TXD1	O	67
34	L1	K2	PHDIN	I	69
35	N3	J7	CTS	I	70
36	M2	L1	RXD1	I	71
37	M1	K4	DCD	I	72
38	P3	L2	DSR	I	73
39	N1	K5	nTEST1	I	74
40	N2	M1	nTEST0	I	75
41	R3	K6	EINT3	I	76
42	P1	M2	nEINT2	I	77
43	P2	L4	nEINT1	I	78

CONVENTIONS

This section presents acronyms, abbreviations, units of measurement, and conventions used in this data sheet.

Acronyms and Abbreviations

Table X lists abbreviations and acronyms used in this data sheet.

Table X. Acronyms and Abbreviations

Acronym/ Abbreviation	Definition
A/D	analog-to-digital
ADC	analog-to-digital converter
CODEC	coder / decoder
D/A	digital-to-analog
DMA	direct-memory access
EPB	embedded peripheral bus
FCS	frame check sequence
FIFO	first in / first out
FIQ	fast interrupt request
GPIO	general purpose I/O
ICT	in circuit test
IR	infrared
IRQ	standard interrupt request
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	liquid crystal display
LED	light-emitting diode
LQFP	low profile quad flat pack
LSB	least significant bit
MIPS	millions of instructions per second
MMU	memory management unit
MSB	most significant bit
PBGA	plastic ball grid array
PCB	printed circuit board
PDA	personal digital assistant
PLL	phase locked loop
p/u	pull-up resistor
RISC	reduced instruction set computer
RTC	Real-Time Clock
SIR	slow (9600–115.2 kbps) infrared
SRAM	static random access memory
SSI	synchronous serial interface

Table X. Acronyms and Abbreviations (Continued)

Acronym/ Abbreviation	Definition
TAP	test access port
TLB	translation lookaside buffer
UART	universal asynchronous receiver

Units of Measurement

Table Y. Unit of Measurement

Symbol	Unit of Measure
°C	degree Celsius
fs	sample frequency
Hz	hertz (cycle per second)
kbps	kilobits per second
KB	kilobyte (1,024 bytes)
kHz	kilohertz
kΩ	kilohm
Mbps	megabits (1,048,576 bits) per second
MB	megabyte (1,048,576 bytes)
MBps	megabytes per second
MHz	megahertz (1,000 kilohertz)
µA	microampere
µF	microfarad
µW	microwatt
µs	microsecond (1,000 nanoseconds)
mA	milliampere
mW	milliwatt
ms	millisecond (1,000 microseconds)
ns	nanosecond
V	volt
W	watt

Revision History

Revision	Date	Changes
PP1	NOV 2003	First preliminary release.
F1	AUG 2005	Updated SDRAM timing. Added MSL data.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

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