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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM7TDMI
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	74MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Hardware ID
Package / Case	256-LFBGA
Supplier Device Package	256-PBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep7311-ib

Processor Core - ARM720T

The EP7311 incorporates an ARM 32-bit RISC microcontroller that controls a wide range of on-chip peripherals. The processor utilizes a three-stage pipeline consisting of fetch, decode and execute stages. Key features include:

- ARM (32-bit) and Thumb (16-bit compressed) instruction sets
- Enhanced MMU for Microsoft Windows CE and other operating systems
- 8 KB of 4-way set-associative cache.
- Translation Look Aside Buffers with 64 Translated Entries

Power Management

The EP7311 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V allowing the device to achieve a performance level equivalent to 60 MIPS. The device has three basic power states:

- Operating — This state is the full performance state. All the clocks and peripheral logic are enabled.
- Idle — This state is the same as the Operating State, except the CPU clock is halted while waiting for an event such as a key press.
- Standby — This state is equivalent to the computer being switched off (no display), and the main oscillator shut down. An event such as a key press can wake-up the processor.

Pin Mnemonic	I/O	Pin Description
BATOK	I	Battery ok input
nEXTPWR	I	External power supply sense input
nPWRFL	I	Power fail sense input
nBATCHG	I	Battery changed sense input

Table A. Power Management Pin Assignments

MaverickKey™ Unique ID

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

Both a specific 32-bit ID as well as a 128-bit random ID is programmed into the EP7311 through the use of laser probing technology. These IDs can then be used to match secure copyrighted content with the ID of the target device the EP7311 is powering, and then deliver the copyrighted information over a secure connection. In addition, secure transactions can benefit by also matching device IDs to server IDs. MaverickKey IDs provide a level of hardware security required for today's Internet appliances.

Memory Interfaces

There are two main external memory interfaces. The first one is the ROM/SRAM/FLASH-style interface that has programmable wait-state timings and includes burst-mode capability, with six chip selects decoding six 256 MB sections of addressable space. For maximum flexibility, each bank can be specified to be 8-, 16-, or 32-bits wide. This allows the use of 8-bit-wide boot ROM options to minimize overall system cost. The on-chip boot ROM can be used in product manufacturing to serially download system code into system FLASH memory. To further minimize system memory requirements and cost, the ARM Thumb instruction set is supported, providing for the use of high-speed 32-bit operations in 16-bit op-codes and yielding industry-leading code density.

Pin Mnemonic		I/O	Pin Description
nCS[5:0]		O	Chip select out
A[27:0]		O	Address output
D[31:0]		I/O	Data I/O
nMOE/nSDCAS	(Note)	O	ROM expansion OP enable
nMWE/nSDWE	(Note)	O	ROM expansion write enable
HALFWORD		O	Halfword access select output
WORD		O	Word access select output
WRITE/nSDRAS	(Note)	O	Transfer direction

Table B. Static Memory Interface Pin Assignments

Note: Pins are multiplexed. See Table S on page 11 for more information.

CODEC Interface

The EP7311 includes an interface to telephony-type CODECs for easy integration into voice-over-IP and other voice communications systems. The CODEC interface is multiplexed to the same pins as the MCP and SSI2.

Pin Mnemonic	I/O	Pin Description
PCMCLK	O	Serial bit clock
PCMOUT	O	Serial data out
PCMIN	I	Serial data in
PCMSYNC	O	Frame sync

Table F. CODEC Interface Pin Assignments

Note: See Table R on page 11 for information on pin multiplexes.

SSI2 Interface

An additional SPI/Microwire1-compatible interface is available for both master and slave mode communications. The SSI2 unit shares the same pins as the MCP and CODEC interfaces through a multiplexer.

- Synchronous clock speeds of up to 512 kHz
- Separate 16 entry TX and RX half-word wide FIFOs
- Half empty/full interrupts for FIFOs
- Separate RX and TX frame sync signals for asymmetric traffic

Pin Mnemonic	I/O	Pin Description
SSICLK	I/O	Serial bit clock
SSITXDA	O	Serial data out
SSIRXDA	I	Serial data in
SSITXFR	I/O	Transmit frame sync
SSIRXFR	I/O	Receive frame sync

Table G. SSI2 Interface Pin Assignments

Note: See Table R on page 11 for information on pin multiplexes.

Synchronous Serial Interface

- ADC (SSI) Interface: Master mode only; SPI and Microwire1-compatible (128 kbps operation)
- Selectable serial clock polarity

Pin Mnemonic	I/O	Pin Description
ADCLK	O	SSI1 ADC serial clock
ADCIN	I	SSI1 ADC serial input
ADCOUT	O	SSI1 ADC serial output
nADCCS	O	SSI1 ADC chip select
SMPCLK	O	SSI1 ADC sample clock

Table H. Serial Interface Pin Assignments

LCD Controller

A DMA address generator is provided that fetches video display data for the LCD controller from memory. The display frame buffer start address is programmable, allowing the LCD frame buffer to be in SDRAM, internal SRAM or external SRAM.

- Interfaces directly to a single-scan panel monochrome STN LCD
- Interfaces to a single-scan panel color STN LCD with minimal external glue logic
- Panel width size is programmable from 32 to 1024 pixels in 16-pixel increments
- Video frame buffer size programmable up to 128 KB
- Bits per pixel of 1, 2, or 4 bits

Pin Mnemonic	I/O	Pin Description
CL1	O	LCD line clock
CL2	O	LCD pixel clock out
DD[3:0]	O	LCD serial display data bus
FRM	O	LCD frame synchronization pulse
M	O	LCD AC bias drive

Table I. LCD Interface Pin Assignments

64-Keypad Interface

Matrix keyboards and keypads can be easily read by the EP7311. A dedicated 8-bit column driver output generates strobes for each keyboard column signal. The pins of Port A, when configured as inputs, can be selectively OR'ed together to provide a keyboard interrupt that is capable of waking the system from a STANDBY or IDLE state.

- Column outputs can be individually set high with the remaining bits left at high-impedance
- Column outputs can be driven all-low, all-high, or all-high-impedance
- Keyboard interrupt driven by OR'ing together all Port A bits
- Keyboard interrupt can be used to wake up the system
- 8×8 keyboard matrix usable with no external logic, extra keys can be added with minimal glue logic

Pin Mnemonic	I/O	Pin Description
COL[7:0]	O	Keyboard scanner column drive

Table J. Keypad Interface Pin Assignments

Interrupt Controller

When unexpected events arise during the execution of a program (i.e., interrupt or memory fault) an exception is usually generated. When these exceptions occur at the same time, a fixed priority system determines the order in which they are handled. The EP7311 interrupt controller has two interrupt types: interrupt request (IRQ) and fast interrupt request (FIQ). The interrupt controller has the ability to control interrupts from 22 different FIQ and IRQ sources.

- Supports 22 interrupts from a variety of sources (such as UARTs, SSI1, and key matrix.)
- Routes interrupt sources to the ARM720T's IRQ or FIQ (Fast IRQ) inputs
- Five dedicated off-chip interrupt lines operate as level sensitive interrupts

.

Pin Mnemonic	I/O	Pin Description
nEINT[2:1]	I	External interrupt
EINT[3]	I	External interrupt
nEXTFIQ	I	External Fast Interrupt input
nMEDCHG/nBROM (Note)	I	Media change interrupt input

Table K. Interrupt Controller Pin Assignments

Note: Pins are multiplexed. See Table S on page 11 for more information.

Real-Time Clock

The EP7311 contains a 32-bit Real Time Clock (RTC) that can be written to and read from in the same manner as the timer counters. It also contains a 32-bit output match register which can be programmed to generate an interrupt.

- Driven by an external 32.768 kHz crystal oscillator

Pin Mnemonic	Pin Description
RTCIN	Real-Time Clock Oscillator Input
RTCOUT	Real-Time Clock Oscillator Output
VDDRTC	Real-Time Clock Oscillator Power
VSSRTC	Real-Time Clock Oscillator Ground

Table L. Real-Time Clock Pin Assignments

PLL and Clocking

- Processor and Peripheral Clocks operate from a single 3.6864 MHz crystal or external 13 MHz clock
- Programmable clock speeds allow the peripheral bus to run at 18 MHz when the processor is set to 18 MHz and at 36 MHz when the processor is set to 36, 49 or 74 MHz

Pin Mnemonic	Pin Description
MOSCIN	Main Oscillator Input
MOSCOUT	Main Oscillator Output
VDDOSC	Main Oscillator Power
VSSOSC	Main Oscillator Ground

Table M. PLL and Clocking Pin Assignments

System Design

As shown in system block diagram, simply adding desired memory and peripherals to the highly integrated EP7311 completes a low-power system solution. All necessary interface logic is integrated on-chip.

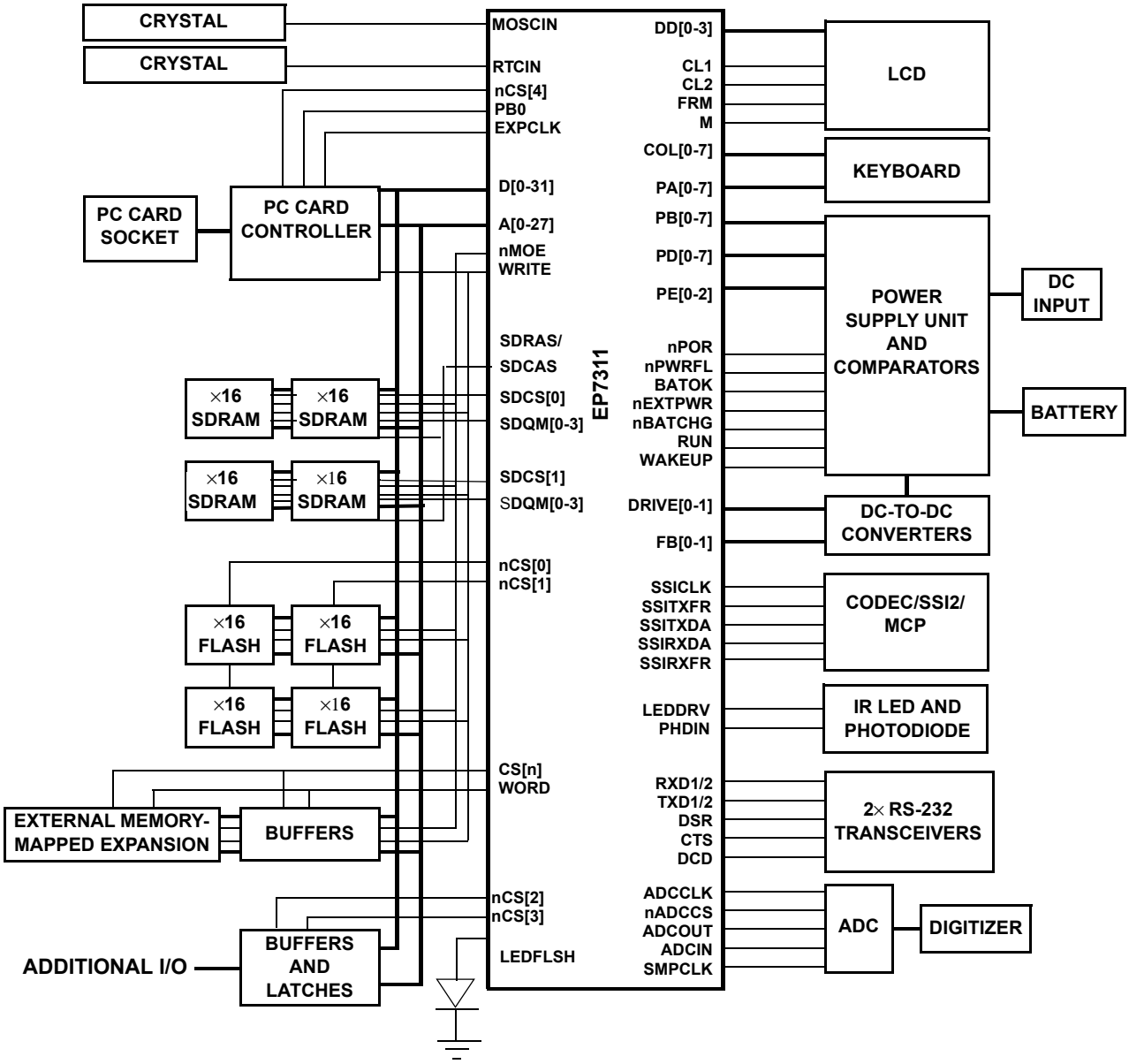


Figure 1. A Maximum EP7311 Based System

Note: A system can only use one of the following peripheral interfaces at any given time: SSI2,CODEC or MCP.

SDRAM Burst Read Cycle

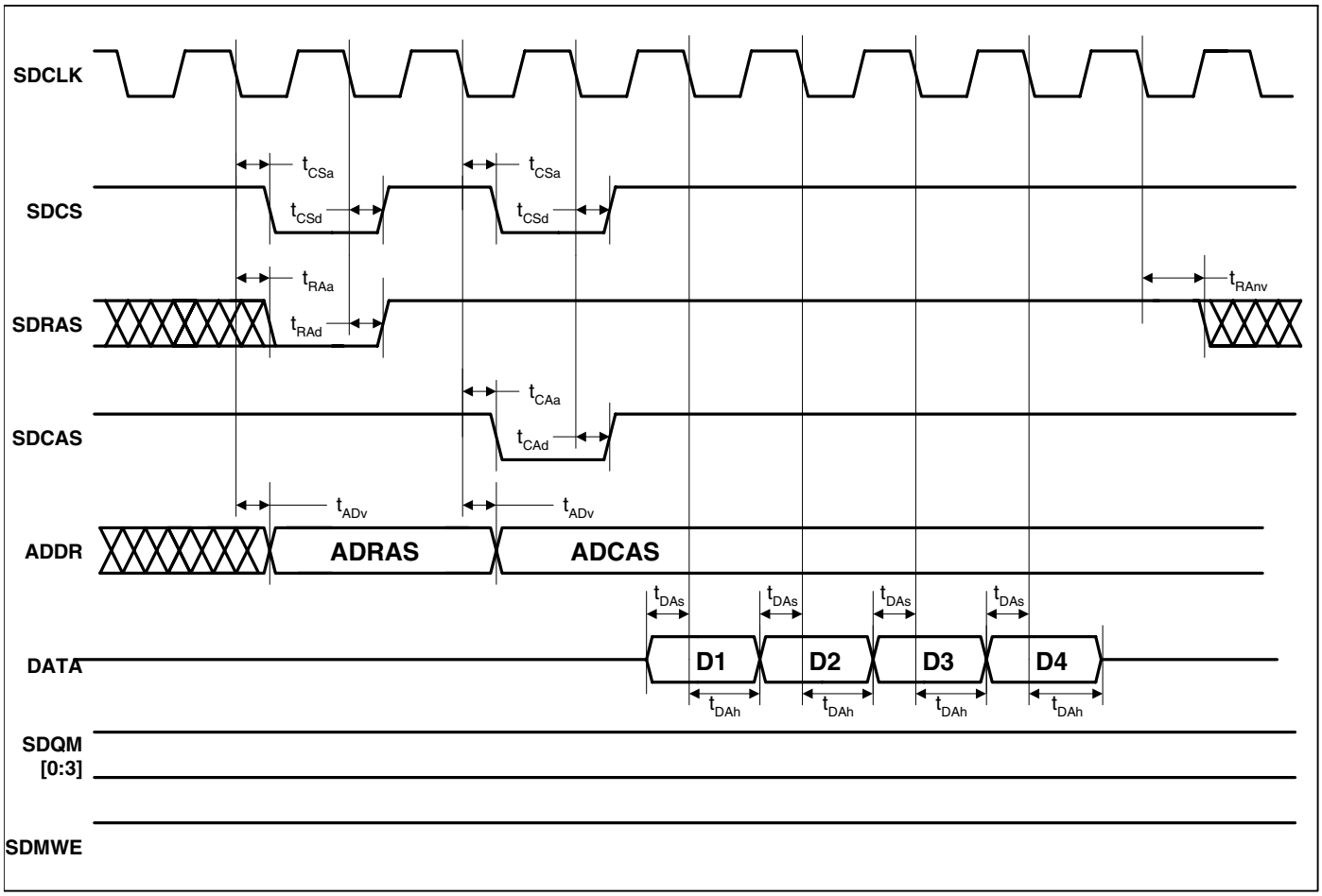


Figure 4. SDRAM Burst Read Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM control and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM control and data signals are approximately equal.

SDRAM Refresh Cycle

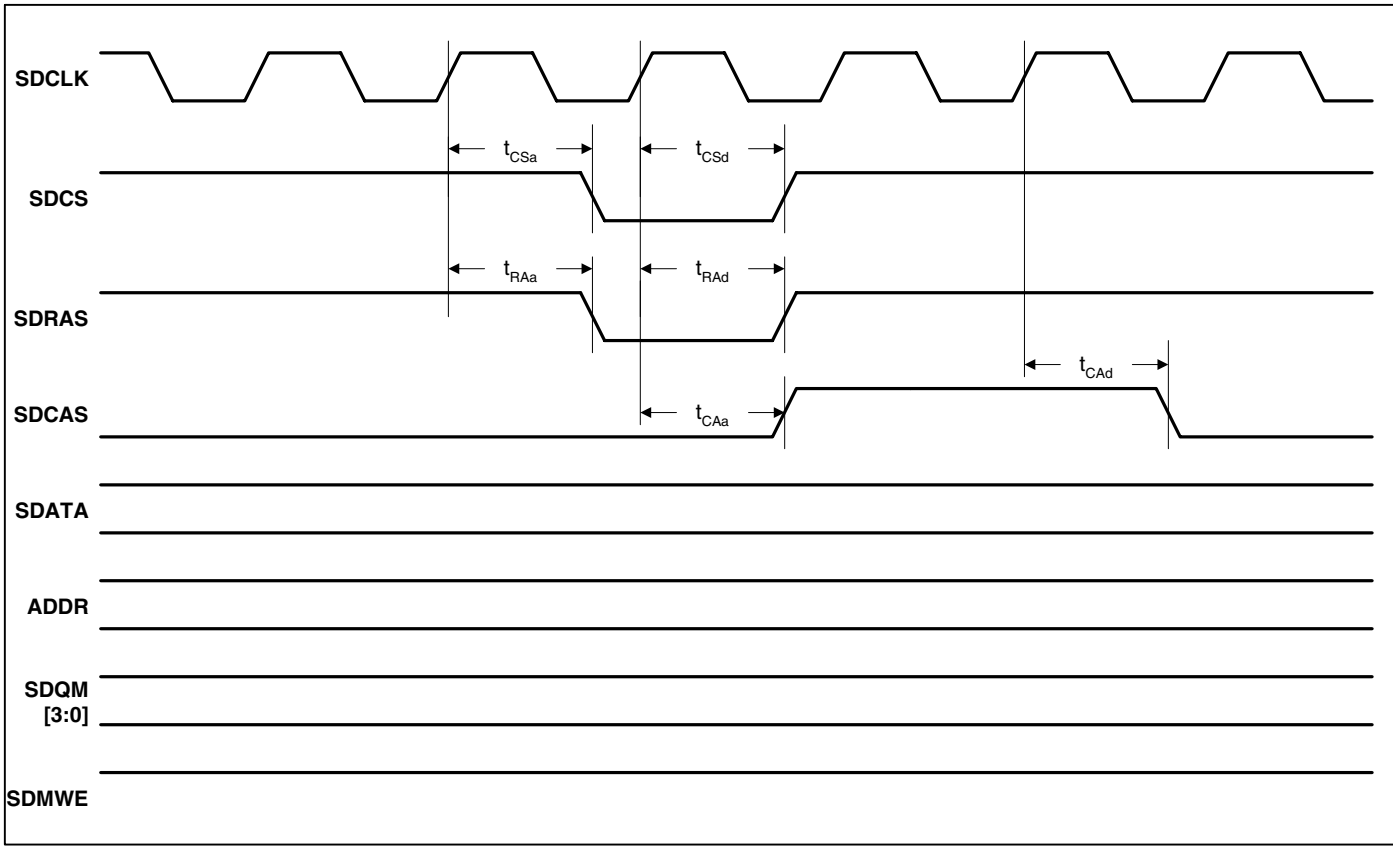


Figure 6. SDRAM Refresh Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM control and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM control and data signals are approximately equal

Static Memory

Figure 7 through Figure 10 define the timings associated with all phases of the Static Memory. The following table contains the values for the timings of each of the Static Memory modes.

Parameter	Symbol	Min	Typ	Max	Unit
EXPCLK rising edge to nCS assert delay time	t_{CSd}	2	8	20	ns
EXPCLK falling edge to nCS deassert hold time	t_{CSh}	2	7	20	ns
EXPCLK rising edge to A assert delay time	t_{Ad}	4	9	16	ns
EXPCLK falling edge to A deassert hold time	t_{Ah}	3	10	19	ns
EXPCLK rising edge to nMWE assert delay time	t_{MWd}	3	6	10	ns
EXPCLK rising edge to nMWE deassert hold time	t_{MWh}	3	6	10	ns
EXPCLK falling edge to nMOE assert delay time	t_{MOEd}	3	7	10	ns
EXPCLK falling edge to nMOE deassert hold time	t_{MOEh}	2	7	10	ns
EXPCLK falling edge to HALFWORD deassert delay time	t_{HWd}	2	8	20	ns
EXPCLK falling edge to WORD assert delay time	t_{WDd}	2	8	16	ns
EXPCLK rising edge to data valid delay time	t_{Dv}	8	13	21	ns
EXPCLK falling edge to data invalid delay time	t_{Dnv}	6	15	30	ns
Data setup to EXPCLK falling edge time	t_{Ds}	-	-	1	ns
EXPCLK falling edge to data hold time	t_{Dh}	-	-	3	ns
EXPCLK rising edge to WRITE assert delay time	t_{WRd}	5	11	23	ns
EXPREADY setup to EXPCLK falling edge time	t_{EXs}	-	-	0	ns
EXPCLK falling edge to EXPREADY hold time	t_{EXh}	-	-	0	ns

SSI1 Interface

Parameter	Symbol	Min	Max	Unit
ADCCLK falling edge to nADCCSS deassert delay time	t_{Cd}	9	10	ms
ADCIN data setup to ADCCLK rising edge time	t_{INs}	-	15	ns
ADCIN data hold from ADCCLK rising edge time	t_{INh}	-	14	ns
ADCCLK falling edge to data valid delay time	t_{Ovd}	– 7	13	ns
ADCCLK falling edge to data invalid delay time	t_{Od}	– 2	3	ns

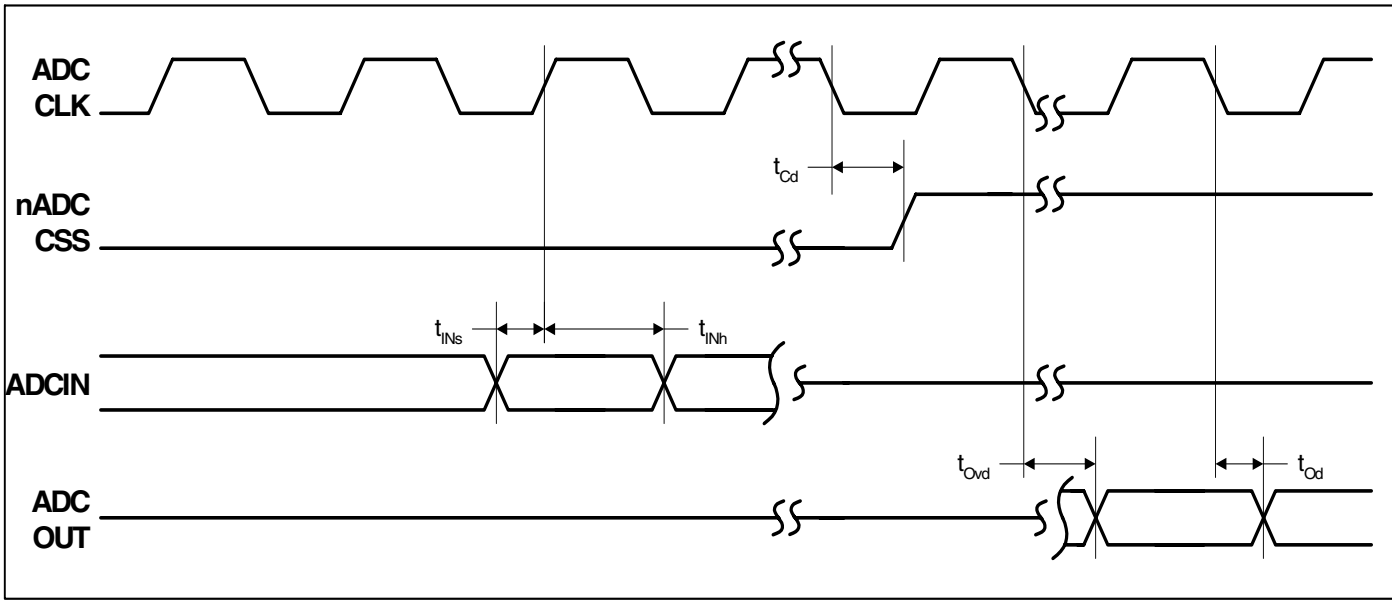


Figure 11. SSI1 Interface Timing Measurement

204-Ball TFBGA Package Characteristics

204-Ball TFBGA Package Specifications

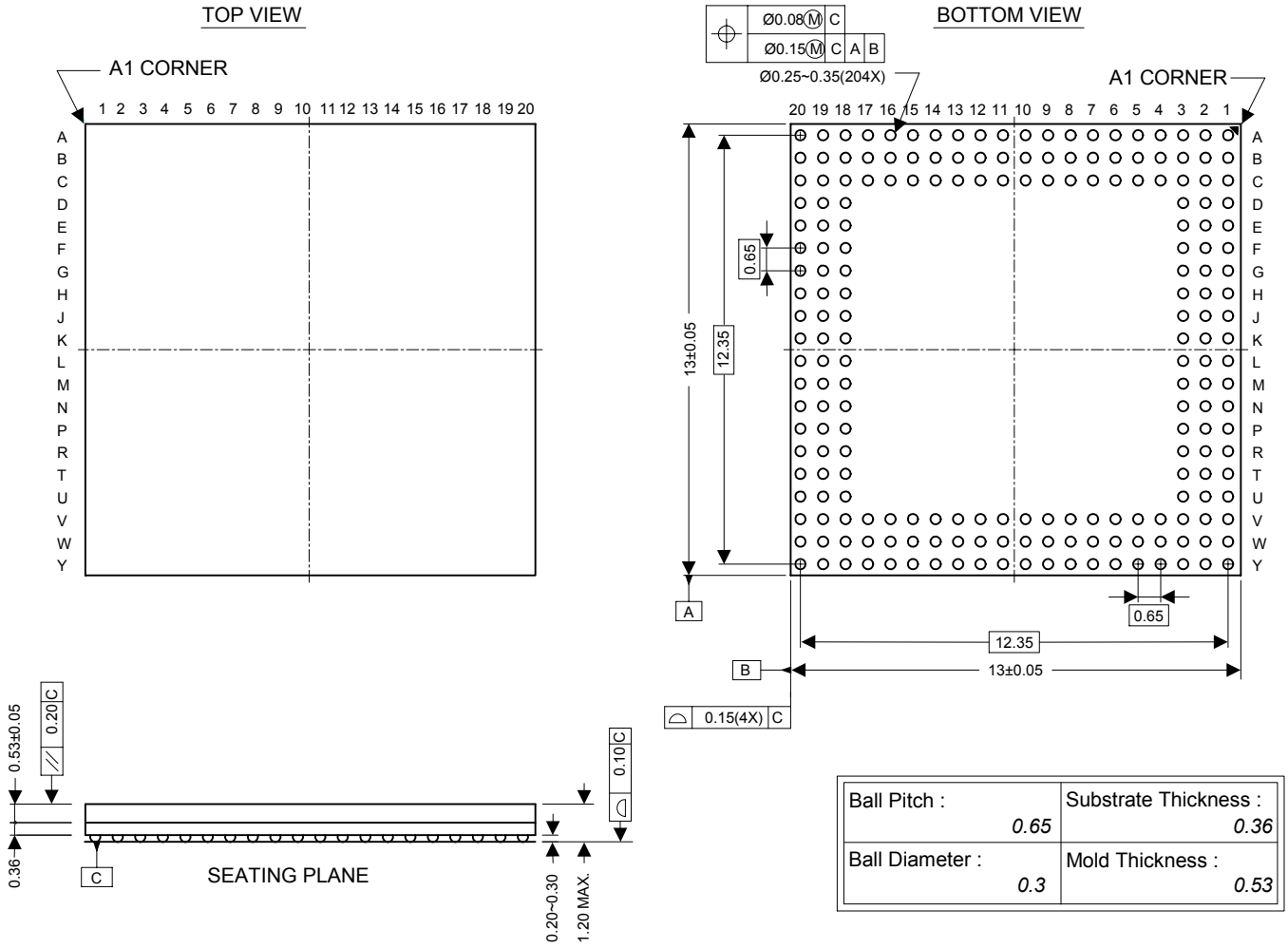


Figure 17. 204-Ball TFBGA Package

Table 21. 204-Ball TFBGA Ball Listing (Continued)

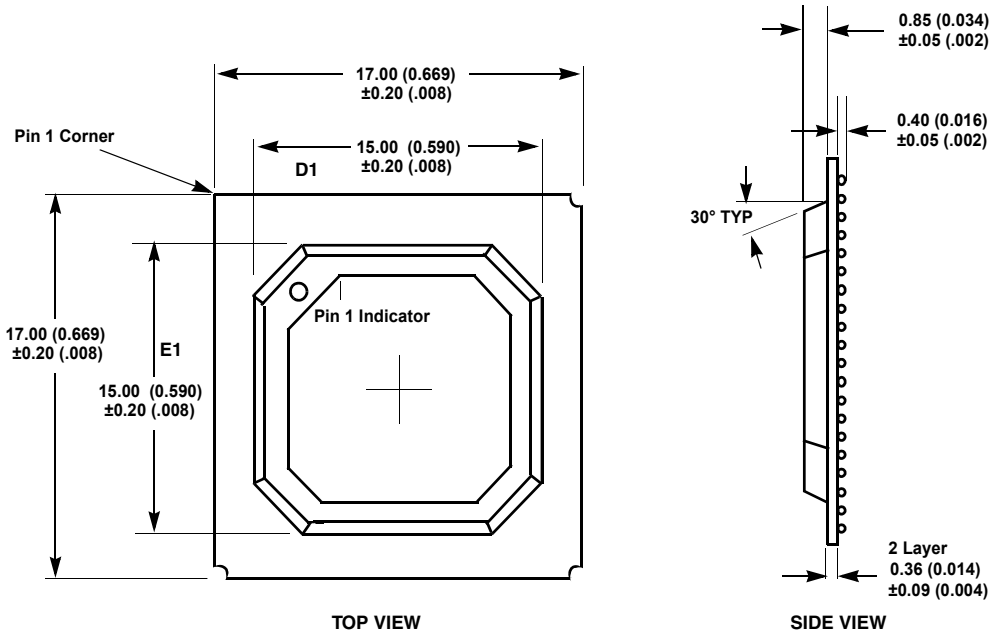
Ball Location	Name	Strength†	Reset State	Type	Description
C20	nPOR	Schmitt		I	Power-on reset input
D1	PB[7]	1	Input‡	I	GPIO port B
D2	RXD[2]			I	UART 2 receive data input
D3	VDDIO			Pad power	Digital I/O power, 3.3V
D18	VSSIO			Pad ground	I/O ground
D19	nBATCHG			I	Battery changed sense input
D20	A[7]	1	Low	O	System byte address
E1	PB[4]	1	Input‡	I	GPIO port B
E2	TXD[2]	1	High	O	UART 2 transmit data output
E3	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
E18	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
E19	nEXTPWR			I	External power supply sense input
E20	D[9]	1	Low	I/O	Data I/O
F1	PB[3]	1	Input‡	I/O	GPIO port B
F2	PB[6]	1	Input‡	I/O	GPIO port B
F3	TDI	with p/u*		I	JTAG data input
F18	D[7]	1	Low	I/O	Data I/O
F19	A[8]	1	Low	O	System byte address
F20	D[10]	1	Low	I/O	Data I/O
G1	PB[1]	1	Input‡	I/O	
G2	PB[2]	1	Input‡	I/O	GPIO port B
G3	PB[5]	1	Input‡	I/O	GPIO port B
G18	D[8]	1	Input‡	I/O	Data I/O
G19	A[9]	1	Low	O	System byte address
G20	D[11]	1	Low	I/O	Data I/O
H1	PA[7]	1	Input‡	I/O	GPIO port A
H[2]	TDO	1	Input‡	O	JTAG data out
H[3]	PB[0]	1	Input‡	I/O	GPIO port B
H[18]	A[10]	1	Low	O	System byte address

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
H19	D[12]	1	Low	I/O	Data I/O
H20	A[12]	1	Low	O	System byte address
J1	PA[4]	1	Input‡	I/O	GPIO port A
J2	PA[5]	1	Input‡	I/O	GPIO port A
J3	PA[6]	1	Input‡	I/O	GPIO port A
J18	A[11]	1	Low	O	System byte address
J19	D[13]	1	Low	I/O	Data I/O
J20	A[13]/DRA[14]	1	Low	O	System byte address / SDRAM address
K1	PA[1]	1	Input‡	I/O	GPIO port A
K2	PA[2]	1	Input‡	I/O	GPIO port A
K3	VDDIO			Pad power	Digital I/O power, 3.3V
K18	D[14]	1	Low	I/O	Data I/O
K19	A[14]/DRA[13]	1	Low	O	System byte address / SDRAM address
K20	D[15]	1	Low	I/O	Data I/O
L1	TXD[1]	1	High	O	UART 1 transmit data out
L2	LEDDRV	1	Low	O	IR LED drive
L3	PA[3]	1	Input‡	I/O	GPIO port A
L18	VDDIO			Pad power	Digital I/O power, 3.3V
L19	D[16]	1	Low	I/O	Data I/O
L20	A[16]/DRA[11]	1	Low	O	System byte address / SDRAM address
M1	RXD[1]			I	UART 1 receive data input
M2	CTS			I	UART 1 clear to send input
M3	PA[0]	1	Input‡	I/O	GPIO port A
M18	A[15]/DRA[12]	1	Low	O	System byte address / SDRAM address
M19	A[17]/DRA[10]	1	Low	O	System byte address / SDRAM address
M20	nTRST			I	JTAG async reset input
N1	DSR			I	UART 1 data set ready input
N2	nTEST[1]	With p/u*		I	Test mode select input
N3	PHDIN			I	Photodiode input

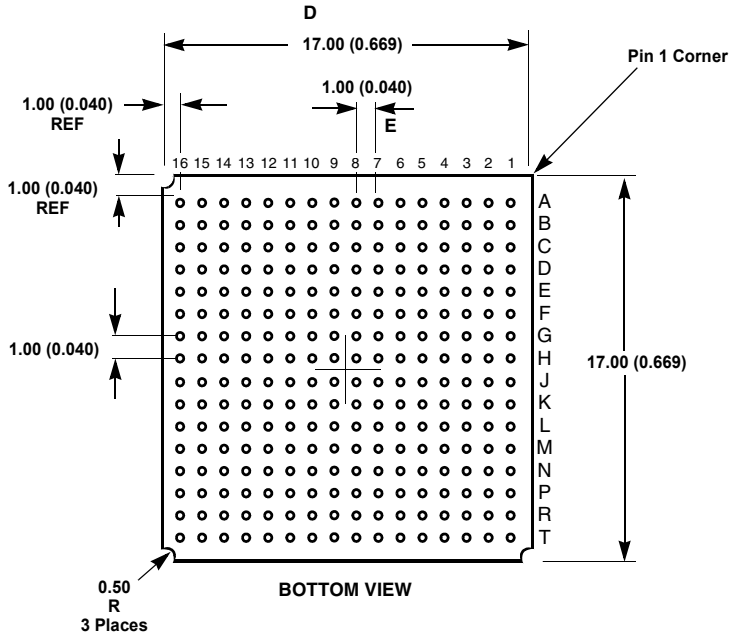
Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
N18	D[17]	1	Low	I/O	Data I/O
N19	D[19]	1	Low	I/O	Data I/O
N20	A[18]/DRA[9]	1	Low	O	System byte address / SDRAM address
P1	EINT[3]			I	External interrupt
P2	nEINT[2]			I	External interrupt input
P3	DCD			I	UART 1 data carrier detect
P18	D[18]	1	Low	I/O	Data I/O
P19	A[20]/DRA[7]	1	Low	O	System byte address / SDRAM address
P20	D[20]	1	Low	I/O	Data I/O
R1	nEXTFIQ			I	External fast interrupt input
R2	PE[2]/CLKSEL	1	Input‡	I/O	GPIO port E / clock input mode select
R3	nTEST[0]	With p/u*		I	Test mode select input
R18	A[19]/DRA[8]	1	Low	O	System byte address / SDRAM address
R19	D[22]	1	Low	I/O	Data I/O
R20	A[21]/DRA[6]	1	Low	O	System byte address / SDRAM address
T1	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
T2	PE[0]/BOOTSEL[0]	1	Input‡	I/O	GPIO port E / boot mode select
T3	nEINT[1]			I	External interrupt input
T18	D[21]	1	Low	I/O	Data I/O
T19	D[23]	1	Low	I/O	Data I/O
T20	A[22]/DRA[5]	1	Low	O	System byte address / SDRAM address
U1	VSSRTC			RTC ground	Real time clock ground
U2	RTCOUT			O	Real time clock oscillator output
U3	RTCIN			I/O	Real time clock oscillator input
U18	HALFWORD	1	Low	O	Halfword access select output
U19	D[24]	1	Low	I/O	Data I/O
U20	A[23]/DRA[4]	1	Low	O	System byte address / SDRAM address
V1	VDDRTC			RTC power	Real time clock power, 2.5V



TOP VIEW

SIDE VIEW



BOTTOM VIEW

JEDEC #: MO-151
Ball Diameter: 0.50 mm ± 0.10 mm
17 ¥ 17 ¥ 1.61 mm body

256-Ball PBGA Ball Listing

The list is ordered by ball location.

Table V. 256-Ball PBGA Ball Listing

Ball Location	Name	Type	Description
A1	VDDIO	Pad power	Digital I/O power, 3.3V
A2	nCS[4]	O	Chip select out
A3	nCS[1]	O	Chip select out
A4	SDCLK	O	SDRAM clock out
A5	SDQM[3]	O	SDRAM byte lane mask
A6	DD[1]	O	LCD serial display data
A7	M	O	LCD AC bias drive
A8	VDDIO	Pad power	Digital I/O power, 3.3V
A9	D[0]	I/O	Data I/O
A10	D[2]	I/O	Data I/O
A11	A[3]	O	System byte address
A12	VDDIO	Pad power	Digital I/O power, 3.3V
A13	A[6]	O	System byte address
A14	MOSCOUT	O	Main oscillator out
A15	VDDOSC	Oscillator power	Oscillator power in, 2.5V
A16	VSSIO	Pad ground	I/O ground
B1	nCS[5]	O	Chip select out
B2	VDDIO	Pad power	I/O ground
B3	nCS[3]	O	Chip select out
B4	nMOE/nSDCAS	O	ROM, expansion OP enable/SDRAM CAS control signal
B5	VDDIO	Pad power	Digital I/O power, 3.3V
B6	nSDCS[1]	O	SDRAM chip select out
B7	DD[2]	O	LCD serial display data
B8	CL[1]	O	LCD line clock
B9	VDDCORE	Core power	Digital core power, 2.5V
B10	D[1]	I/O	Data I/O
B11	A[2]	O	System byte address
B12	A[4]	O	System byte address
B13	A[5]	O	System byte address
B14	WAKEUP	I	System wake up input
B15	VDDIO	Pad power	Digital I/O power, 3.3V
B16	nURESET	I	User reset input
C1	VDDIO	Pad power	Digital I/O power, 3.3V
C2	EXPCLK	I	Expansion clock input
C3	VSSIO	Pad ground	I/O ground
C4	VDDIO	Pad power	Digital I/O power, 3.3V
C5	VSSIO	Pad ground	I/O ground
C6	VSSIO	Pad ground	I/O ground
C7	VSSIO	Pad ground	I/O ground
C8	VDDIO	Pad power	Digital I/O power, 3.3V
C9	VSSIO	Pad ground	I/O ground
C10	VSSIO	Pad ground	I/O ground
C11	VSSIO	Pad ground	I/O ground

Table V. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
C12	VDDIO	Pad power	Digital I/O power, 3.3V
C13	VSSIO	Pad ground	I/O ground
C14	VSSIO	Pad ground	I/O ground
C15	nPOR	I	Power-on reset input
C16	nEXTPWR	I	External power supply sense input
D1	WRITE/nSDRAS	O	Transfer direction / SDRAM RAS signal output
D2	EXPRDY	I	Expansion port ready input
D3	VSSIO	Pad ground	I/O ground
D4	VDDIO	Pad power	Digital I/O power, 3.3V
D5	nCS[2]	O	Chip select out
D6	nMWE/nSDWE	O	ROM, expansion write enable/ SDRAM write enable control signal
D7	nSDCS[0]	O	SDRAM chip select out
D8	CL[2]	O	LCD pixel clock out
D9	VSSRTC	Core ground	Real time clock ground
D10	D[4]	I/O	Data I/O
D11	nPWRFL	I	Power fail sense input
D12	MOSCIN	I	Main oscillator input
D13	VDDIO	Pad power	Digital I/O power, 3.3V
D14	VSSIO	Pad ground	I/O ground
D15	D[7]	I/O	Data I/O
D16	D[8]	I/O	Data I/O
E1	RXD[2]	I	UART 2 receive data input
E2	PB[7]	I	GPIO port B
E3	TDI	I	JTAG data input
E4	WORD	O	Word access select output
E5	VSSIO	Pad ground	I/O ground
E6	nCS[0]	O	Chip select out
E7	SDQM[2]	O	SDRAM byte lane mask
E8	FRM	O	LCD frame synchronization pulse
E9	A[0]	O	System byte address
E10	D[5]	I/O	Data I/O
E11	VSSOSC	Oscillator ground	PLL ground
E12	VSSIO	Pad ground	I/O ground
E13	nMEDCHG/nBROM	I	Media change interrupt input / internal ROM boot enable
E14	VDDIO	Pad power	Digital I/O power, 3.3V
E15	D[9]	I/O	Data I/O
E16	D[10]	I/O	Data I/O
F1	PB[5]	I	GPIO port B
F2	PB[3]	I	GPIO port B
F3	VSSIO	Pad ground	I/O ground
F4	TXD[2]	O	UART 2 transmit data output
F5	RUN/CLKEN	O	Run output / clock enable output
F6	VSSIO	Pad ground	I/O ground

Table V. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
F7	SDCKE	O	SDRAM clock enable output
F8	DD[3]	O	LCD serial display data
F9	A[1]	O	System byte address
F10	D[6]	I/O	Data I/O
F11	VSSRTC	RTC ground	Real time clock ground
F12	BATOK	I	Battery ok input
F13	nBATCHG	I	Battery changed sense input
F14	VSSIO	Pad ground	I/O ground
F15	D[11]	I/O	Data I/O
F16	VDDIO	Pad power	Digital I/O power, 3.3V
G1	PB[1]	I	GPIO port B
G2	VDDIO	Pad power	Digital I/O power, 3.3V
G3	TDO	O	JTAG data out
G4	PB[4]	I	GPIO port B
G5	PB[6]	I	GPIO port B
G6	VSSRTC	Core ground	Real time clock ground
G7	VSSRTC	RTC ground	Real time clock ground
G8	DD[0]	O	LCD serial display data
G9	D[3]	I/O	Data I/O
G10	VSSRTC	RTC ground	Real time clock ground
G11	A[7]	O	System byte address
G12	A[8]	O	System byte address
G13	A[9]	O	System byte address
G14	VSSIO	Pad ground	I/O ground
G15	D[12]	I/O	Data I/O
G16	D[13]	I/O	Data I/O
H1	PA[7]	I	GPIO port A
H2	PA[5]	I	GPIO port A
H3	VSSIO	Pad ground	I/O ground
H4	PA[4]	I	GPIO port A
H5	PA[6]	I	GPIO port A
H6	PB[0]	I	GPIO port B
H7	PB[2]	I	GPIO port B
H8	VSSRTC	RTC ground	Real time clock ground
H9	VSSRTC	RTC ground	Real time clock ground
H10	A[10]	O	System byte address
H11	A[11]	O	System byte address
H12	A[12]	O	System byte address
H13	A[13]/DRA[14]	O	System byte address / SDRAM address
H14	VSSIO	Pad ground	I/O ground
H15	D[14]	I/O	Data I/O
H16	D[15]	I/O	Data I/O
J1	PA[3]	I	GPIO port A
J2	PA[1]	I	GPIO port A
J3	VSSIO	Pad ground	I/O ground
J4	PA[2]	I	GPIO port A
J5	PA[0]	I	GPIO port A
J6	TXD[1]	O	UART 1 transmit data out

Table V. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
J7	CTS	I	UART 1 clear to send input
J8	VSSRTC	RTC ground	Real time clock ground
J9	VSSRTC	RTC ground	Real time clock ground
J10	A[17]/DRA[10]	O	System byte address / SDRAM address
J11	A[16]/DRA[11]	O	System byte address / SDRAM address
J12	A[15]/DRA[12]	O	System byte address / SDRAM address
J13	A[14]/DRA[13]	O	System byte address / SDRAM address
J14	nTRST	I	JTAG async reset input
J15	D[16]	I/O	Data I/O
J16	D[17]	I/O	Data I/O
K1	LEDDRV	O	IR LED drivet
K2	PHDIN	I	Photodiode input
K3	VSSIO	Pad ground	I/O ground
K4	DCD	I	UART 1 data carrier detect
K5	nTEST[1]	I	Test mode select input
K6	EINT[3]	I	External interrupt
K7	VSSRTC	RTC ground	Real time clock ground
K8	ADCIN	I	SSI1 ADC serial input
K9	COL[4]	O	Keyboard scanner column drive
K10	TCLK	I	JTAG clock
K11	D[20]	I/O	Data I/O
K12	D[19]	I/O	Data I/O
K13	D[18]	I/O	Data I/O
K14	VSSIO	Pad ground	I/O ground
K15	VDDIO	Pad power	Digital I/O power, 3.3V
K16	VDDIO	Pad power	Digital I/O power, 3.3V
L1	RXD[1]	I	UART 1 receive data input
L2	DSR	I	UART 1 data set ready input
L3	VDDIO	Pad power	Digital I/O power, 3.3V
L4	nEINT[1]	I	External interrupt input
L5	PE[2]/CLKSEL	I	GPIO port E / clock input mode select
L6	VSSRTC	RTC ground	Real time clock ground
L7	PD[0]/LEDFLSH	I/O	GPIO port D / LED blinker output
L8	VSSRTC	Core ground	Real time clock ground
L9	COL[6]	O	Keyboard scanner column drive
L10	D[31]	I/O	Data I/O
L11	VSSRTC	RTC ground	Real time clock ground
L12	A[22]/DRA[5]	O	System byte address / SDRAM address
L13	A[21]/DRA[6]	O	System byte address / SDRAM address
L14	VSSIO	Pad ground	I/O ground
L15	A[18]/DRA[9]	O	System byte address / SDRAM address
L16	A[19]/DRA[8]	O	System byte address / SDRAM address
M1	nTEST[0]	I	Test mode select input
M2	nEINT[2]	I	External interrupt input
M3	VDDIO	Pad power	Digital I/O power, 3.3V
M4	PE[0]/BOOTSEL[0]	I	GPIO port E / Boot mode select
M5	TMS	I	JTAG mode select
M6	VDDIO	Pad power	Digital I/O power, 3.3V

Table V. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
M7	SSITXFR	I/O	MCP/CODEC/SSI2 frame sync
M8	DRIVE[1]	I/O	PWM drive output
M9	FB[0]	I	PWM feedback input
M10	COL[0]	O	Keyboard scanner column drive
M11	D[27]	I/O	Data I/O
M12	VSSIO	Pad ground	I/O ground
M13	A[23]/DRA[4]	O	System byte address / SDRAM address
M14	VDDIO	Pad power	Digital I/O power, 3.3V
M15	A[20]/DRA[7]	O	System byte address / SDRAM address
M16	D[21]	I/O	Data I/O
N1	nEXTFIQ	I	External fast interrupt input
N2	PE[1]/BOOTSEL[1]	I	GPIO port E / boot mode select
N3	VSSIO	Pad ground	I/O ground
N4	VDDIO	Pad power	Digital I/O power, 3.3V
N5	PD[5]	I/O	GPIO port D
N6	PD[2]	I/O	GPIO port D
N7	SSIRXDA	I/O	MCP/CODEC/SSI2 serial data input
N8	ADCCLK	O	SSI1 ADC serial clock
N9	SMPCLK	O	SSI1 ADC sample clock
N10	COL[2]	O	Keyboard scanner column drive
N11	D[29]	I/O	Data I/O
N12	D[26]	I/O	Data I/O
N13	HALFWORD	O	Halfword access select output
N14	VSSIO	Pad ground	I/O ground
N15	D[22]	I/O	Data I/O
N16	D[23]	I/O	Data I/O
P1	VSSRTC	RTC ground	Real time clock ground
P2	RTCOUT	O	Real time clock oscillator output
P3	VSSIO	Pad ground	I/O ground
P4	VSSIO	Pad ground	I/O ground
P5	VDDIO	Pad power	Digital I/O power, 3.3V
P6	VSSIO	Pad ground	I/O ground
P7	VSSIO	Pad ground	I/O ground
P8	VDDIO	Pad power	Digital I/O power, 3.3V
P9	VSSIO	Pad ground	I/O ground
P10	VDDIO	Pad power	Digital I/O power, 3.3V
P11	VSSIO	Pad ground	I/O ground
P12	VSSIO	Pad ground	I/O ground
P13	VDDIO	Pad power	Digital I/O power
P14	VSSIO	Pad ground	I/O ground
P15	D[24]	I/O	Data I/O
P16	VDDIO	Pad power	Digital I/O power, 3.3V
R1	RTCIN	I/O	Real time clock oscillator input
R2	VDDIO	Pad power	Digital I/O power, 3.3V
R3	PD[4]	I/O	GPIO port D
R4	PD[1]	I/O	GPIO port D
R5	SSITXDA	O	MCP/CODEC/SSI2 serial data output
R6	nADCCS	O	SSI1 ADC chip select

Table V. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
R7	VDDIO	Pad power	Digital I/O power, 3.3V
R8	ADCOUT	O	SSI1 ADC serial data output
R9	COL[7]	O	Keyboard scanner column drive
R10	COL[3]	O	Keyboard scanner column drive
R11	COL[1]	O	Keyboard scanner column drive
R12	D[30]	I/O	Data I/O
R13	A[27]/DRA[0]	O	System byte address / SDRAM address
R14	A[25]/DRA[2]	O	System byte address / SDRAM address
R15	VDDIO	Pad power	Digital I/O power, 3.3V
R16	A[24]/DRA[3]	O	System byte address / SDRAM address
T1	VDDRTC	RTC power	Real time clock power, 2.5V
T2	PD[7]/SDQM[1]	I/O	GPIO port D / SDRAM byte lane mask
T3	PD[6]/SDQM[0]	I/O	GPIO port D / SDRAM byte lane mask
T4	PD[3]	I/O	GPIO port D
T5	SSICLK	I/O	MCP/CODEC/SSI2 serial clock
T6	SSIRXFR	–	MCP/CODEC/SSI2 frame sync
T7	VDDCORE	Core power	Core power, 2.5V
T8	DRIVE[0]	I/O	PWM drive output
T9	FB[1]	I	PWM feedback input
T10	COL[5]	O	Keyboard scanner column drive
T11	VDDIO	Pad power	Digital I/O power, 3.3V
T12	BUZ	O	Buzzer drive output
T13	D[28]	I/O	Data I/O
T14	A[26]/DRA[1]	O	System byte address / SDRAM address
T15	D[25]	I/O	Data I/O
T16	VSSIO	Pad ground	I/O ground

Table W. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
102	Y17	N12	D[26]	I/O	179
103	W17	R14	A[25]/DRA[2]	O	182
104	Y18	T15	D[25]	I/O	184
105	V17	N13	HALFWORD	O	187
106	W18	R16	A[24]/DRA[3]	O	189
109	Y19	P15	D[24]	I/O	191
110	W20	M13	A[23]/DRA[4]	O	194
111	U18	N16	D[23]	I/O	196
112	V20	L12	A[22]/DRA[5]	O	199
113	U19	N15	D[22]	I/O	201
114	U20	L13	A[21]/DRA[6]	O	204
115	T19	M16	D[21]	I/O	206
117	T20	M15	A[20]/DRA[7]	O	209
118	R19	K11	D[20]	I/O	211
119	R20	L16	A[19]/DRA[8]	O	214
120	T18	K12	D[19]	I/O	216
121	P19	L15	A[18]/DRA[9]	O	219
122	P20	K13	D[18]	I/O	221
126	R18	J10	A[17]/DRA[10]	O	224
127	N19	J16	D[17]	I/O	226
128	N20	J11	A[16]/DRA[11]	O	229
129	P18	J15	D[16]	I/O	231
130	M19	J12	A[15]/DRA[12]	O	234
131	N18	H16	D[15]	I/O	236
132	L20	J13	A[14]/DRA[13]	O	239
133	L19	H15	D[14]	I/O	241
134	M18	H13	A[13]/DRA[14]	O	244
135	K20	G16	D[13]	I/O	246
136	K19	H12	A[12]	O	249
137	K18	G15	D[12]	I/O	251
138	J20	H11	A[11]	O	254
141	J19	F15	D[11]	I/O	256
142	H20	H10	A[10]	O	259
143	H19	E16	D[10]	I/O	261
144	J18	G13	A[9]	O	264
145	K3	E15	D[9]	I/O	266
146	Y3	G12	A[8]	O	269
147	G20	D16	D[8]	I/O	271

CONVENTIONS

This section presents acronyms, abbreviations, units of measurement, and conventions used in this data sheet.

Acronyms and Abbreviations

Table X lists abbreviations and acronyms used in this data sheet.

Table X. Acronyms and Abbreviations

Acronym/ Abbreviation	Definition
A/D	analog-to-digital
ADC	analog-to-digital converter
CODEC	coder / decoder
D/A	digital-to-analog
DMA	direct-memory access
EPB	embedded peripheral bus
FCS	frame check sequence
FIFO	first in / first out
FIQ	fast interrupt request
GPIO	general purpose I/O
ICT	in circuit test
IR	infrared
IRQ	standard interrupt request
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	liquid crystal display
LED	light-emitting diode
LQFP	low profile quad flat pack
LSB	least significant bit
MIPS	millions of instructions per second
MMU	memory management unit
MSB	most significant bit
PBGA	plastic ball grid array
PCB	printed circuit board
PDA	personal digital assistant
PLL	phase locked loop
p/u	pull-up resistor
RISC	reduced instruction set computer
RTC	Real-Time Clock
SIR	slow (9600–115.2 kbps) infrared
SRAM	static random access memory
SSI	synchronous serial interface

Table X. Acronyms and Abbreviations (Continued)

Acronym/ Abbreviation	Definition
TAP	test access port
TLB	translation lookaside buffer
UART	universal asynchronous receiver

Units of Measurement

Table Y. Unit of Measurement

Symbol	Unit of Measure
°C	degree Celsius
fs	sample frequency
Hz	hertz (cycle per second)
kbps	kilobits per second
KB	kilobyte (1,024 bytes)
kHz	kilohertz
kΩ	kilohm
Mbps	megabits (1,048,576 bits) per second
MB	megabyte (1,048,576 bytes)
MBps	megabytes per second
MHz	megahertz (1,000 kilohertz)
µA	microampere
µF	microfarad
µW	microwatt
µs	microsecond (1,000 nanoseconds)
mA	milliampere
mW	milliwatt
ms	millisecond (1,000 microseconds)
ns	nanosecond
V	volt
W	watt

Revision History

Revision	Date	Changes
PP1	NOV 2003	First preliminary release.
F1	AUG 2005	Updated SDRAM timing. Added MSL data.

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