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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM7TDMI
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	74MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Hardware ID
Package / Case	204-TFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep7311-ir

FEATURES *(cont)*

- LCD controller
  - — Interfaces directly to a single-scan panel monochrome STN LCD
  - — Interfaces to a single-scan panel color STN LCD with minimal external glue logic
- Full JTAG boundary scan and Embedded ICE® support
- Integrated Peripheral Interfaces
  - — 32-bit SDRAM Interface up to 2 external banks
  - — 8/32/16-bit SRAM/FLASH/ROM Interface
  - — Multimedia Codec Port
  - — Two Synchronous Serial Interfaces (SSI1, SSI2)
  - — CODEC Sound Interface
  - — 8×8 Keypad Scanner
  - — 27 General Purpose Input/Output pins
  - — Dedicated LED flasher pin from the RTC
- Internal Peripherals
  - — Two 16550 compatible UARTs
  - — IrDA Interface
  - — Two PWM Interfaces
  - — Real-time Clock
  - — Two general purpose 16-bit timers
  - — Interrupt Controller
  - — Boot ROM
- Package
  - — 208-Pin LQFP
  - — 256-Ball PBGA
  - — 204-Ball TFBGA
- The fully static EP7311 is optimized for low power dissipation and is fabricated on a 0.25 micron CMOS process
- Development Kits
  - — EDB7312: Development Kit with color STN LCD on board.
  - — EDB7312-LW: EDB7312 with Lynuxworks' BlueCat Linux Tools and software for Windows host (free 30 day BlueCat support from Lynuxworks).
  - — EDB7312-LL: EDB7312 with Lynuxworks' BlueCat Linux Tools and software for Linux host (free 30 day BlueCat support from Lynuxworks).

*Note: * BlueCat available separately through Lynuxworks only.*
** Use the EDB7312 Development Kit for all the EP73xx devices.*

OVERVIEW *(cont.)*

The EP7311 is designed for low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states: operating, idle and standby.

One of its notable features is MaverickKey unique IDs. These are factory programmed IDs in response to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs consist of two registers, one 32-bit series register and one random 128-bit register that may be used by an OEM for an authentication mechanism.

Simply by adding desired memory and peripherals to the highly integrated EP7311 completes a low-power system solution. All necessary interface logic is integrated on-chip.

Table of Contents

FEATURES 1

OVERVIEW 1

- Processor Core - ARM720T 6
- Power Management 6
- MaverickKey™ Unique ID 6
- Memory Interfaces 6
- Digital Audio Capability 6
- Universal Asynchronous Receiver/Transmitters (UARTs) 6
- Digital Audio Interface (DAI) 7
- CODEC Interface 7
- SSI2 Interface 7
- Synchronous Serial Interface 8
- LCD Controller 8
- Interrupt Controller 8
- Real-Time Clock 8
- PLL and Clocking 9
- DC-to-DC converter interface (PWM) 9
- Timers 9
- General Purpose Input/Output (GPIO) 9
- Hardware debug Interface 9
- Internal Boot ROM 10
- Packaging 10
- Pin Multiplexing 10
- System Design 11

ELECTRICAL SPECIFICATIONS 12

- Absolute Maximum Ratings 12
- Recommended Operating Conditions 12
- DC Characteristics 12

Timings 14

- Timing Diagram Conventions 14
- Timing Conditions 14
- Static Memory 15
  - Static Memory Single Read Cycle 16
  - Static Memory Single Write Cycle 17
  - Static Memory Burst Read Cycle 18
  - Static Memory Burst Write Cycle 19
- SSI1 Interface 20
- SSI2 Interface 21
- LCD Interface 22
- JTAG Interface 23

Packages 24

- 208-Pin LQFP Package Characteristics 24
  - 208-Pin LQFP Package Specifications 24
  - 208-Pin LQFP Pin Diagram 25
  - 208-Pin LQFP Numeric Pin Listing 26
- 204-Ball TFBGA Package Characteristics 29
  - 204-Ball TFBGA Package Specifications 29
  - 204-Ball TFBGA Pinout (Top View) 30

List of Figures

Figure 1. A Maximum EP7309 Based System 11
Figure 2. Legend for Timing Diagrams 14
Figure 3. Static Memory Single Read Cycle Timing Measurement 16
Figure 4. Static Memory Single Write Cycle Timing Measurement 17
Figure 5. Static Memory Burst Read Cycle Timing Measurement 18
Figure 6. Static Memory Burst Write Cycle Timing Measurement 19
Figure 7. SSI1 Interface Timing Measurement 20
Figure 8. SSI2 Interface Timing Measurement 21
Figure 9. LCD Controller Timing Measurement 22
Figure 10. JTAG Timing Measurement 23
Figure 11. 208-Pin LQFP Package Outline Drawing 24
Figure 12. 208-Pin LQFP (Low Profile Quad Flat Pack) Pin Diagram 25
Figure 13. 204-Ball TFBGA Package 29
Figure 14. 256-Ball PBGA Package 38

List of Tables

Table 1. Power Management Pin Assignments 6
Table 2. Static Memory Interface Pin Assignments 6
Table 3. Universal Asynchronous Receiver/Transmitters Pin Assignments 7
Table 4. DAI Interface Pin Assignments 7
Table 5. CODEC Interface Pin Assignments 7
Table 6. SSI2 Interface Pin Assignments 7
Table 7. Serial Interface Pin Assignments 8
Table 8. LCD Interface Pin Assignments 8
Table 9. Keypad Interface Pin Assignments 8
Table 10. Interrupt Controller Pin Assignments 8
Table 11. Real-Time Clock Pin Assignments 9
Table 12. PLL and Clocking Pin Assignments 9
Table 13. DC-to-DC Converter Interface Pin Assignments 9
Table 14. General Purpose Input/Output Pin Assignments 9
Table 15. Hardware Debug Interface Pin Assignments 9
Table 16. LED Flasher Pin Assignments 9
Table 17. DAI/SSI2/CODEC Pin Multiplexing 10
Table 18. Pin Multiplexing 10
Table 19. 208-Pin LQFP Numeric Pin Listing 26
Table 20. 204-Ball TFBGA Ball Listing 31
Table 21. 256-Ball PBGA Ball Listing 39
Table 22. JTAG Boundary Scan Signal Ordering 43
Table 23. Acronyms and Abbreviations 48
Table 24. Unit of Measurement 48
Table 25. Pin Description Conventions 49

64-Keypad Interface

Matrix keyboards and keypads can be easily read by the EP7311. A dedicated 8-bit column driver output generates strobes for each keyboard column signal. The pins of Port A, when configured as inputs, can be selectively OR'ed together to provide a keyboard interrupt that is capable of waking the system from a STANDBY or IDLE state.

- Column outputs can be individually set high with the remaining bits left at high-impedance
- Column outputs can be driven all-low, all-high, or all-high-impedance
- Keyboard interrupt driven by OR'ing together all Port A bits
- Keyboard interrupt can be used to wake up the system
- 8×8 keyboard matrix usable with no external logic, extra keys can be added with minimal glue logic

Pin Mnemonic	I/O	Pin Description
COL[7:0]	O	Keyboard scanner column drive

Table J. Keypad Interface Pin Assignments

Interrupt Controller

When unexpected events arise during the execution of a program (i.e., interrupt or memory fault) an exception is usually generated. When these exceptions occur at the same time, a fixed priority system determines the order in which they are handled. The EP7311 interrupt controller has two interrupt types: interrupt request (IRQ) and fast interrupt request (FIQ). The interrupt controller has the ability to control interrupts from 22 different FIQ and IRQ sources.

- Supports 22 interrupts from a variety of sources (such as UARTs, SSI1, and key matrix.)
- Routes interrupt sources to the ARM720T's IRQ or FIQ (Fast IRQ) inputs
- Five dedicated off-chip interrupt lines operate as level sensitive interrupts

.

Pin Mnemonic	I/O	Pin Description
nEINT[2:1]	I	External interrupt
EINT[3]	I	External interrupt
nEXTFIQ	I	External Fast Interrupt input
nMEDCHG/nBROM (Note)	I	Media change interrupt input

Table K. Interrupt Controller Pin Assignments

Note: Pins are multiplexed. See Table S on page 11 for more information.

Real-Time Clock

The EP7311 contains a 32-bit Real Time Clock (RTC) that can be written to and read from in the same manner as the timer counters. It also contains a 32-bit output match register which can be programmed to generate an interrupt.

- Driven by an external 32.768 kHz crystal oscillator

Pin Mnemonic	Pin Description
RTCIN	Real-Time Clock Oscillator Input
RTCOUT	Real-Time Clock Oscillator Output
VDDRTC	Real-Time Clock Oscillator Power
VSSRTC	Real-Time Clock Oscillator Ground

Table L. Real-Time Clock Pin Assignments

PLL and Clocking

- Processor and Peripheral Clocks operate from a single 3.6864 MHz crystal or external 13 MHz clock
- Programmable clock speeds allow the peripheral bus to run at 18 MHz when the processor is set to 18 MHz and at 36 MHz when the processor is set to 36, 49 or 74 MHz

Pin Mnemonic	Pin Description
MOSCIN	Main Oscillator Input
MOSCOUT	Main Oscillator Output
VDDOSC	Main Oscillator Power
VSSOSC	Main Oscillator Ground

Table M. PLL and Clocking Pin Assignments

DC-to-DC converter interface (PWM)

- Provides two 96 kHz clock outputs with programmable duty ratio (from 1-in-16 to 15-in-16) that can be used to drive a positive or negative DC to DC converter

Pin Mnemonic	I/O	Pin Description
DRIVE[1:0]	I/O	PWM drive output
FB[1:0]	I	PWM feedback input

Table N. DC-to-DC Converter Interface Pin Assignments

Timers

- Internal (RTC) timer
- Two internal 16-bit programmable hardware count-down timers

General Purpose Input/Output (GPIO)

- Three 8-bit and one 3-bit GPIO ports
- Supports scanning keyboard matrix

Pin Mnemonic		I/O	Pin Description
PA[7:0]		I/O	GPIO port A
PB[7:0]		I/O	GPIO port B
PD[0]/LEDFLSH	(Note)	I/O	GPIO port D
PD[5:1]		I/O	GPIO port D
PD[7:6]/SDQM[1:0]	(Note)	I/O	GPIO port D
PE[1:0]/BOOTSEL[1:0]	(Note)	I/O	GPIO port E
PE[2]/CLKSEL	(Note)	I/O	GPIO port E

Table O. General Purpose Input/Output Pin Assignments

Note: Pins are multiplexed. See Table S on page 11 for more information.

Hardware debug Interface

- Full JTAG boundary scan and Embedded ICE® support

Pin Mnemonic	I/O	Pin Description
TCLK	I	JTAG clock
TDI	I	JTAG data input
TDO	O	JTAG data output
nTRST	I	JTAG async reset input
TMS	I	JTAG mode select

Table P. Hardware Debug Interface Pin Assignments

LED Flasher

A dedicated LED flasher module can be used to generate a low frequency signal on Port D pin 0 for the purpose of blinking an LED without CPU intervention. The LED flasher feature is ideal as a visual annunciator in battery powered applications, such as a voice mail indicator on a portable phone or an appointment reminder on a PDA.

- Software adjustable flash period and duty cycle
- Operates from 32 kHz RTC clock
- Will continue to flash in IDLE and STANDBY states
- 4 mA drive current

Pin Mnemonic		I/O	Pin Description
PD[0]/LEDFLSH	(Note)	O	LED flasher driver

Table Q. LED Flasher Pin Assignments

Note: Pins are multiplexed. See Table S on page 11 for more information.

Internal Boot ROM

The internal 128 byte Boot ROM facilitates download of saved code to the on-board SRAM/FLASH.

Packaging

The EP7311 is available in a 208-pin LQFP package, 256-ball PBGA package or a 204-ball TFBGA package.

Pin Multiplexing

The following table shows the pin multiplexing of the MCP, SSI2 and the CODEC. The selection between SSI2 and the CODEC is controlled by the state of the SERSEL bit in SYSCON2. The choice between the SSI2, CODEC, and the MCP is controlled by the MCPSEL bit in SYSCON3 (see the EP73xx User's Manual for more information).

Pin Mnemonic	I/O	MCP	SSI2	CODEC
SSICLK	I/O	SIBCLK	SSICLK	PCMCLK
SSITXDA	O	SIBDOUT	SSITXDA	PCMOUT
SSIRXDA	I	SIBDIN	SSIRXDA	PCMIN
SSITXFR	I/O	SIBSYNC	SSITXFR	PCMSYNC
SSIRXFR	I	p/u	SSIRXFR	p/u
BUZ	O			

Table R. MCP/SSI2/CODEC Pin Multiplexing

The following table shows the pins that have been multiplexed in the EP7311.

Signal	Block	Signal	Block
nMOE	Static Memory	nSDCAS	SDRAM
nMWE	Static Memory	nSDWE	SDRAM
WRITE	Static Memory	nSDRAS	SDRAM
A[27:15]	Static Memory	DRA[0:12]	SDRAM
A[14:13]	Static Memory	DRA[13:14]	SDRAM
PD[7:6]	GPIO	SDQM[1:0]	SDRAM
RUN	System Configuration	CLKEN	System Configuration
nMEDCHG	Interrupt Controller	nBROM	Boot ROM select
PD[0]	GPIO	LEDFLSH	LED Flasher
PE[1:0]	GPIO	BOOTSEL[1:0]	System Configuration
PE[2]	GPIO	CLKSEL	System Configuration

Table S. Pin Multiplexing

System Design

As shown in system block diagram, simply adding desired memory and peripherals to the highly integrated EP7311 completes a low-power system solution. All necessary interface logic is integrated on-chip.

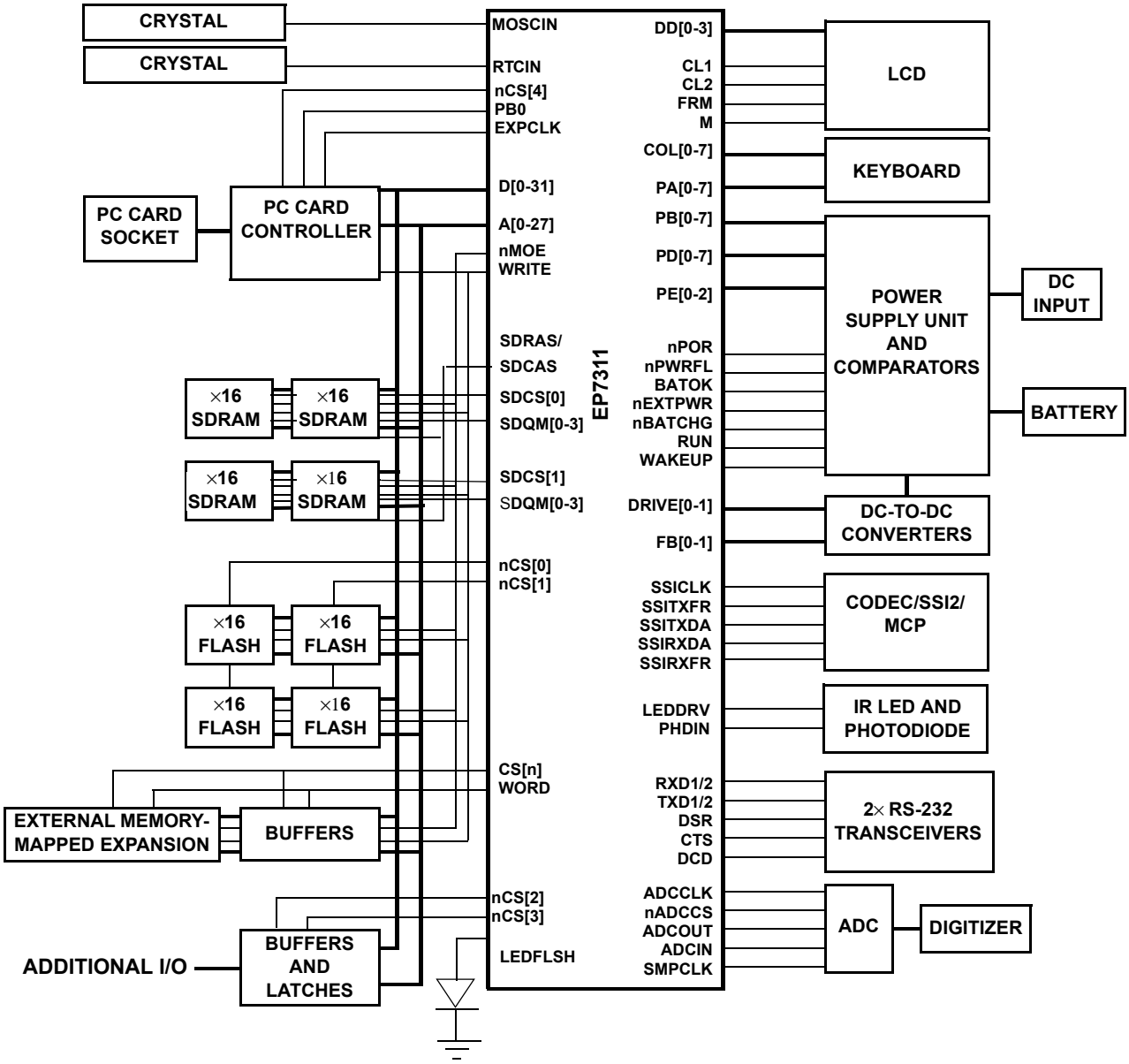


Figure 1. A Maximum EP7311 Based System

Note: A system can only use one of the following peripheral interfaces at any given time: SSI2,CODEC or MCP.

Timings

Timing Diagram Conventions

This data sheet contains timing diagrams. The following key explains the components used in these diagrams. Any variations are clearly labelled when they occur. Therefore, no additional meaning should be attached unless specifically stated.

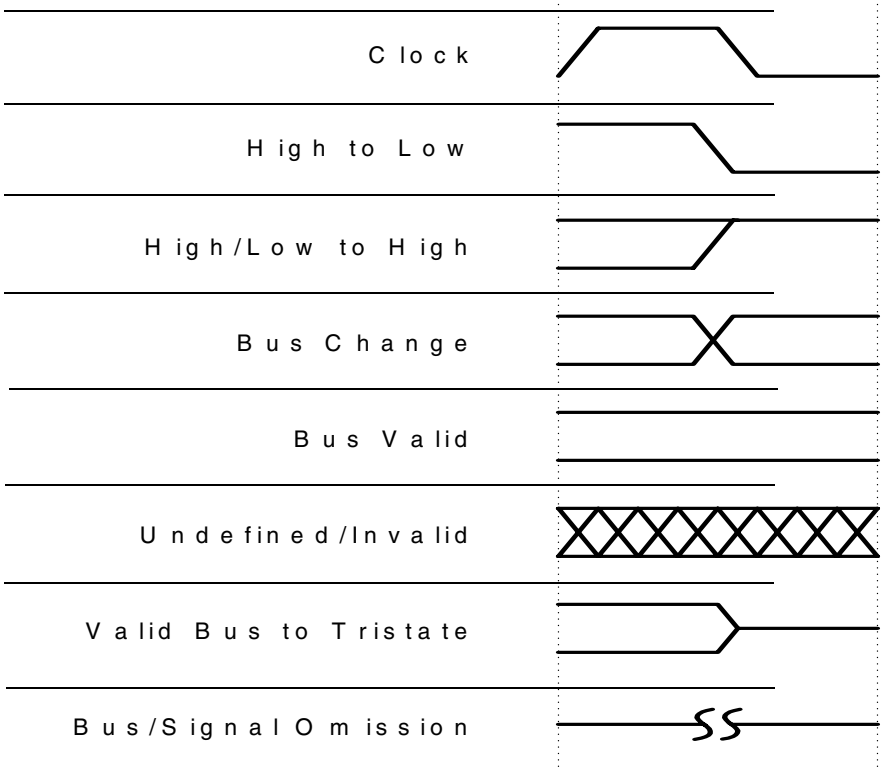


Figure 2. Legend for Timing Diagrams

Timing Conditions

Unless specified otherwise, the following conditions are true for all timing measurements. All characteristics are specified at V_{DDIO} = 3.1 - 3.5 V and V_{SS} = 0 V over an operating temperature of -40°C to +85°C. Pin loadings is 50 pF. The timing values are referenced to 1/2 V_{DD}.

SDRAM Interface

Figure 3 through Figure 6 define the timings associated with all phases of the SDRAM. The following table contains the values for the timings of each of the SDRAM modes.

Parameter	Symbol	Min	Typ	Max	Unit
SDCLK rising edge to SDCS assert delay time	t_{CSa}	0	2	4	ns
SDCLK rising edge to SDCS deassert delay time	t_{CSd}	– 3	2	10	ns
SDCLK rising edge to SDRAS assert delay time	t_{RAa}	1	3	7	ns
SDCLK rising edge to SDRAS deassert delay time	t_{RAd}	– 3	1	10	ns
SDCLK rising edge to SDRAS invalid delay time	t_{RAnv}	2	4	7	ns
SDCLK rising edge to SDCAS assert delay time	t_{CAa}	– 2	2	5	ns
SDCLK rising edge to SDCAS deassert delay time	t_{CAd}	– 5	0	3	ns
SDCLK rising edge to ADDR transition time	t_{ADv}	– 3	1	5	ns
SDCLK rising edge to ADDR invalid delay time	t_{ADx}	– 2	2	5	ns
SDCLK rising edge to SDMWE assert delay time	t_{MWa}	– 3	1	5	ns
SDCLK rising edge to SDMWE deassert delay time	t_{MWd}	– 4	0	4	ns
DATA transition to SDCLK rising edge time	t_{DAs}	2	-	-	ns
SDCLK rising edge to DATA transition hold time	t_{DAh}	1	-	-	ns
SDCLK rising edge to DATA transition delay time	t_{DAd}	0	-	15	ns

SDRAM Load Mode Register Cycle

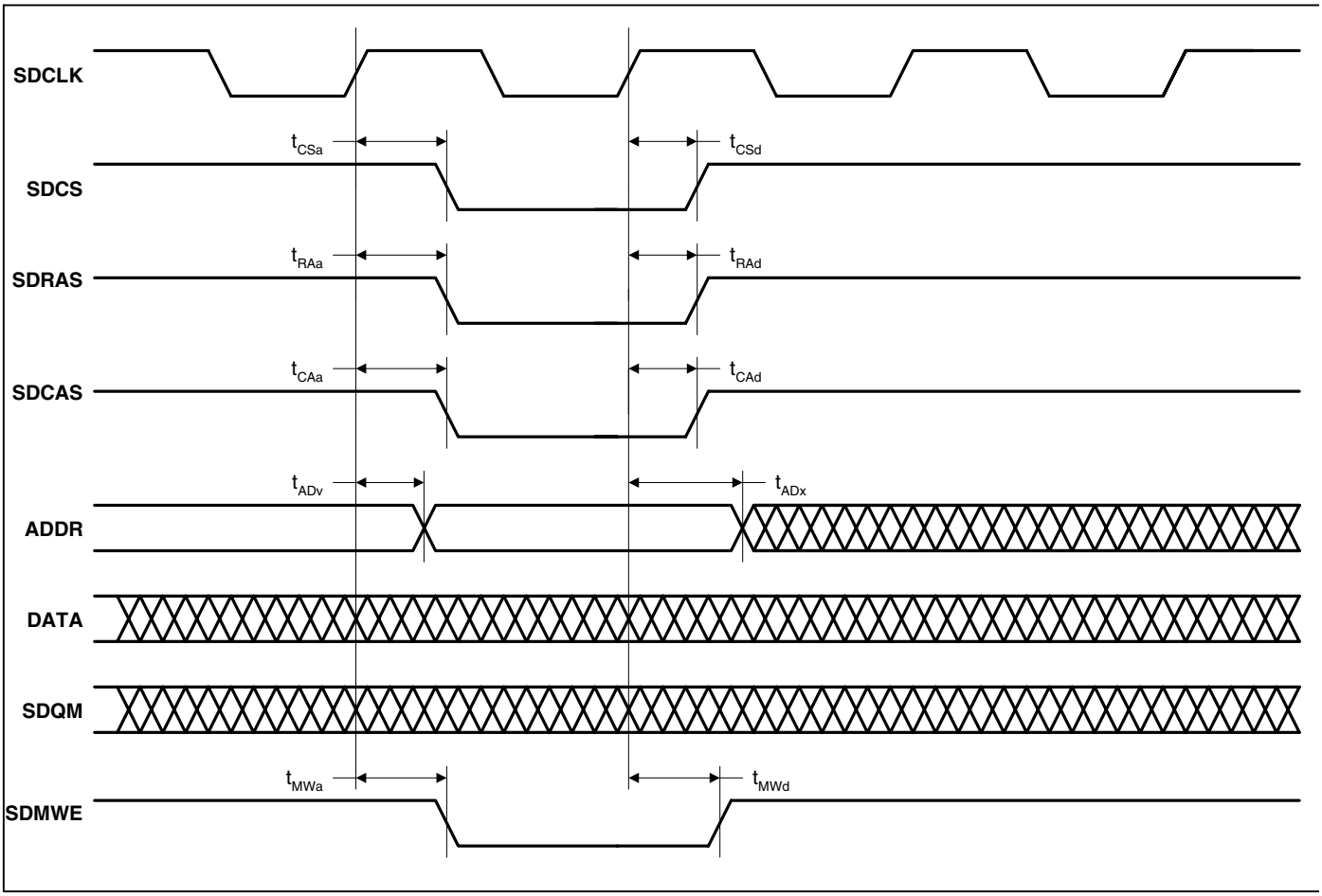


Figure 3. SDRAM Load Mode Register Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM control and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM control and data signals are approximately equal

Static Memory

Figure 7 through Figure 10 define the timings associated with all phases of the Static Memory. The following table contains the values for the timings of each of the Static Memory modes.

Parameter	Symbol	Min	Typ	Max	Unit
EXPCLK rising edge to nCS assert delay time	t_{CSd}	2	8	20	ns
EXPCLK falling edge to nCS deassert hold time	t_{CSh}	2	7	20	ns
EXPCLK rising edge to A assert delay time	t_{Ad}	4	9	16	ns
EXPCLK falling edge to A deassert hold time	t_{Ah}	3	10	19	ns
EXPCLK rising edge to nMWE assert delay time	t_{MWd}	3	6	10	ns
EXPCLK rising edge to nMWE deassert hold time	t_{MWh}	3	6	10	ns
EXPCLK falling edge to nMOE assert delay time	t_{MOEd}	3	7	10	ns
EXPCLK falling edge to nMOE deassert hold time	t_{MOEh}	2	7	10	ns
EXPCLK falling edge to HALFWORD deassert delay time	t_{HWd}	2	8	20	ns
EXPCLK falling edge to WORD assert delay time	t_{WDd}	2	8	16	ns
EXPCLK rising edge to data valid delay time	t_{Dv}	8	13	21	ns
EXPCLK falling edge to data invalid delay time	t_{Dnv}	6	15	30	ns
Data setup to EXPCLK falling edge time	t_{Ds}	-	-	1	ns
EXPCLK falling edge to data hold time	t_{Dh}	-	-	3	ns
EXPCLK rising edge to WRITE assert delay time	t_{WRd}	5	11	23	ns
EXPREADY setup to EXPCLK falling edge time	t_{EXs}	-	-	0	ns
EXPCLK falling edge to EXPREADY hold time	t_{EXh}	-	-	0	ns

Static Memory Single Read Cycle

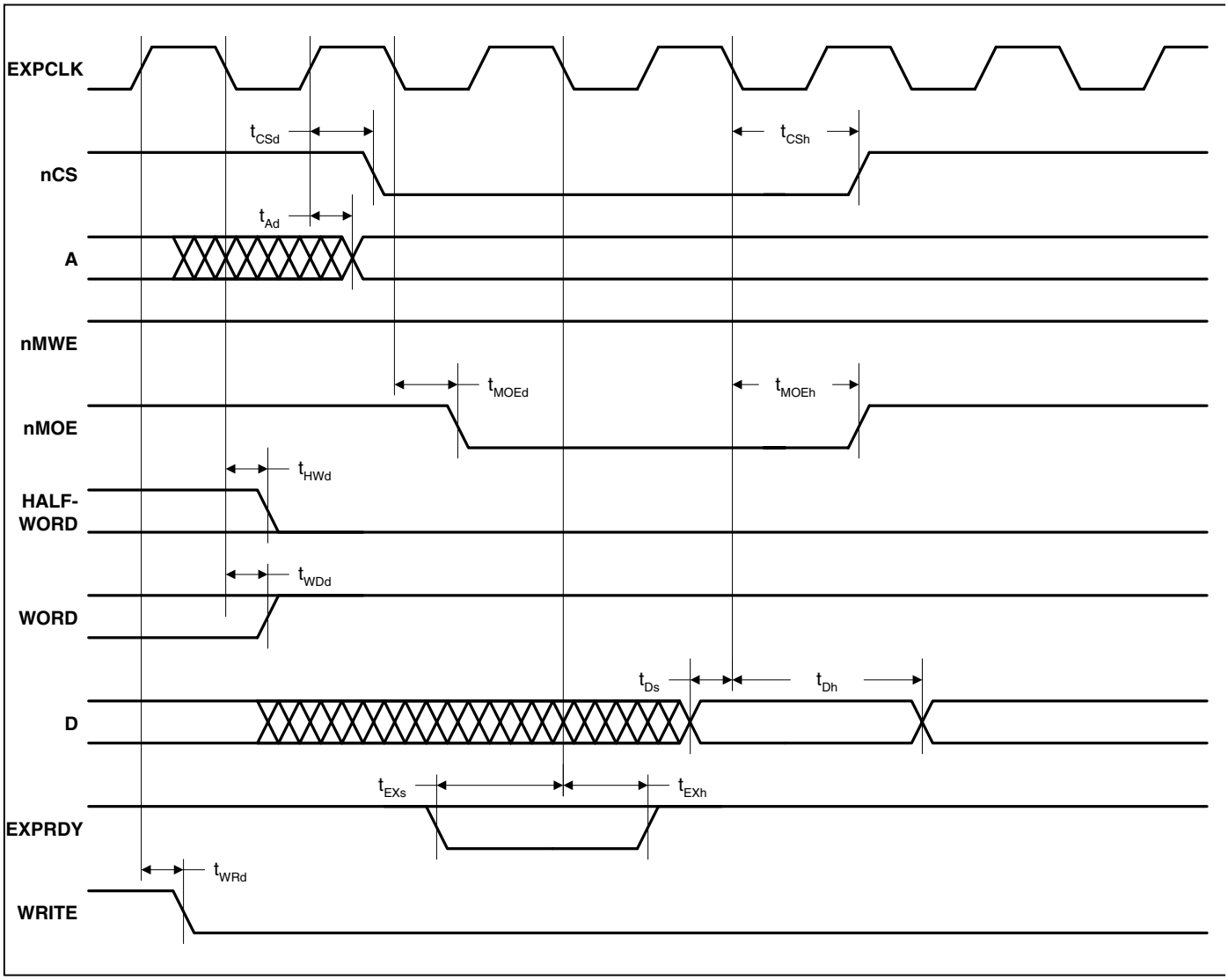


Figure 7. Static Memory Single Read Cycle Timing Measurement

Note: 1. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
2. Address, Halfword, Word, and Write hold state until next cycle.

204-Ball TFBGA Ball Listing

The list is ordered by ball location.

Table 21. 204-Ball TFBGA Ball Listing

Ball Location	Name	Strength†	Reset State	Type	Description
A1	VDDIO			Pad power	Digital I/O power, 3.3 V
A2	EXPCLK	1		I	Expansion clock input
A3	nCS[3]	1	High	O	Chip select 3
A4	nCS[1]	1	High	O	Chip select 1
A5	nMWE/nSDWE	1	High	O	ROM, expansion write enable/ SDRAM write enable control signal
A6	SDQM[2]	2	Low	O	SDRAM byte lane mask
A7	nSDCS[1]	1	High	O	SDRAM chip select 2
A8	DD[2]	1	Low	O	LCD serial display data
A9	FRM	1	Low	O	LCD frame synchronization pulse
A10	CL[1]	1	Low	O	LCD line clock
A11	VSSCORE			Core ground	Core ground
A12	D[1]	1	Low	I/O	Data I/O
A13	A[2]	2	Low	O	System byte address
A14	D[4]	1	Low	I/O	Data I/O
A15	A[5]	1	Low	O	System byte address
A16	nPWRFL			I	Power fail sense input
A17	MOSCOUT			O	Main oscillator out
A18	VSSIO			Pad ground	I/O ground
A19	VSSIO			Pad ground	I/O ground
A20	VSSIO			Pad ground	I/O ground
B1	WORD	1	Low	O	Word access select output
B2	VDDIO			Pad power	Digital I/O power, 3.3 V
B3	nCS[5]	1	Low	O	Chip select 5
B4	nCS[2]	1	High	O	Chip select 2
B5	nMOE/nSDCAS	1	High	O	ROM, expansion OP enable/SDRAM CAS control signal
B6	SDCKE	2	Low	O	SDRAM clock enable output
B7	nSDCS[0]	1	High	O	SDRAM chip select 0

Table 21. 204-Ball TFBGA Ball Listing (Continued)

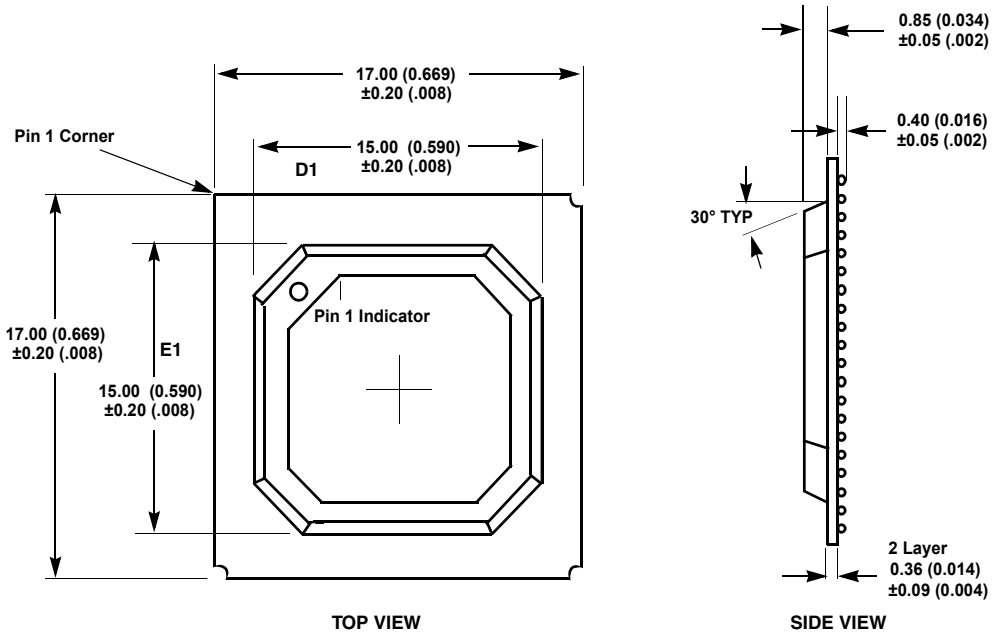
Ball Location	Name	Strength†	Reset State	Type	Description
C20	nPOR	Schmitt		I	Power-on reset input
D1	PB[7]	1	Input‡	I	GPIO port B
D2	RXD[2]			I	UART 2 receive data input
D3	VDDIO			Pad power	Digital I/O power, 3.3V
D18	VSSIO			Pad ground	I/O ground
D19	nBATCHG			I	Battery changed sense input
D20	A[7]	1	Low	O	System byte address
E1	PB[4]	1	Input‡	I	GPIO port B
E2	TXD[2]	1	High	O	UART 2 transmit data output
E3	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
E18	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
E19	nEXTPWR			I	External power supply sense input
E20	D[9]	1	Low	I/O	Data I/O
F1	PB[3]	1	Input‡	I/O	GPIO port B
F2	PB[6]	1	Input‡	I/O	GPIO port B
F3	TDI	with p/u*		I	JTAG data input
F18	D[7]	1	Low	I/O	Data I/O
F19	A[8]	1	Low	O	System byte address
F20	D[10]	1	Low	I/O	Data I/O
G1	PB[1]	1	Input‡	I/O	
G2	PB[2]	1	Input‡	I/O	GPIO port B
G3	PB[5]	1	Input‡	I/O	GPIO port B
G18	D[8]	1	Input‡	I/O	Data I/O
G19	A[9]	1	Low	O	System byte address
G20	D[11]	1	Low	I/O	Data I/O
H1	PA[7]	1	Input‡	I/O	GPIO port A
H[2]	TDO	1	Input‡	O	JTAG data out
H[3]	PB[0]	1	Input‡	I/O	GPIO port B
H[18]	A[10]	1	Low	O	System byte address

Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
N18	D[17]	1	Low	I/O	Data I/O
N19	D[19]	1	Low	I/O	Data I/O
N20	A[18]/DRA[9]	1	Low	O	System byte address / SDRAM address
P1	EINT[3]			I	External interrupt
P2	nEINT[2]			I	External interrupt input
P3	DCD			I	UART 1 data carrier detect
P18	D[18]	1	Low	I/O	Data I/O
P19	A[20]/DRA[7]	1	Low	O	System byte address / SDRAM address
P20	D[20]	1	Low	I/O	Data I/O
R1	nEXTFIQ			I	External fast interrupt input
R2	PE[2]/CLKSEL	1	Input‡	I/O	GPIO port E / clock input mode select
R3	nTEST[0]	With p/u*		I	Test mode select input
R18	A[19]/DRA[8]	1	Low	O	System byte address / SDRAM address
R19	D[22]	1	Low	I/O	Data I/O
R20	A[21]/DRA[6]	1	Low	O	System byte address / SDRAM address
T1	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
T2	PE[0]/BOOTSEL[0]	1	Input‡	I/O	GPIO port E / boot mode select
T3	nEINT[1]			I	External interrupt input
T18	D[21]	1	Low	I/O	Data I/O
T19	D[23]	1	Low	I/O	Data I/O
T20	A[22]/DRA[5]	1	Low	O	System byte address / SDRAM address
U1	VSSRTC			RTC ground	Real time clock ground
U2	RTCOUT			O	Real time clock oscillator output
U3	RTCIN			I/O	Real time clock oscillator input
U18	HALFWORD	1	Low	O	Halfword access select output
U19	D[24]	1	Low	I/O	Data I/O
U20	A[23]/DRA[4]	1	Low	O	System byte address / SDRAM address
V1	VDDRTC			RTC power	Real time clock power, 2.5V

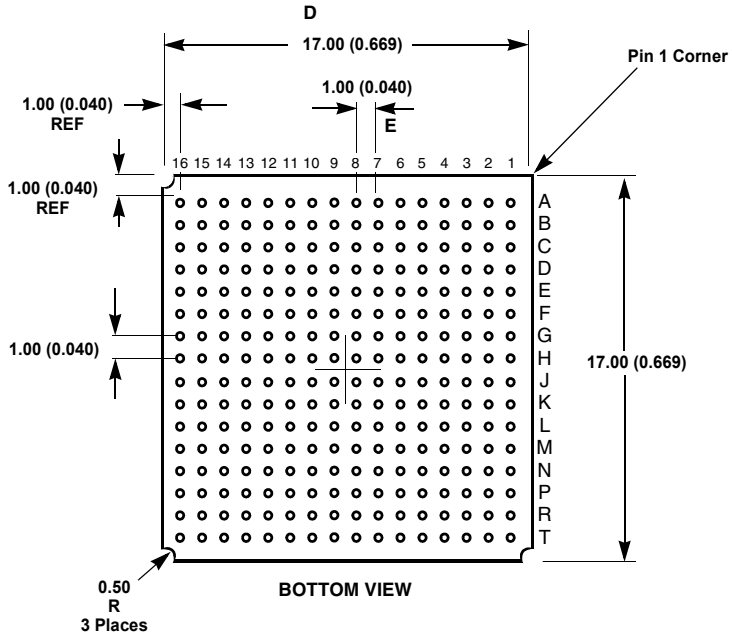
Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
W11	ADCOUT	1	Low	O	SSI1 ADC serial data output
W12	FB[0]			I	PWM feedback input
W13	COL[5]	1	High	O	Keyboard scanner column drive
W14	COL[2]	1	High	O	Keyboard scanner column drive
W15	COL[0]	1	High	O	Keyboard scanner column drive
W16	D[30]	1	Low	I/O	Data I/O
W17	A[27]/DRA[0]	2	Low	O	System byte address / SDRAM address
W18	D[26]	1	Low	I/O	Data I/O
W19	VDDIO			Pad power	Digital I/O power, 3.3V
W20	D[25]	1	Low	I/O	Data I/O
Y1	VSSIO			Pad ground	I/O ground
Y2	VSSIO			Pad ground	I/O ground
Y3	VSSIO			Pad ground	I/O ground
Y4	PD[5]	1	Low	I/O	GPIO port D
Y5	PD[3]	1	Low	I/O	GPIO port D
Y6	PD[0]/LEDFLSH	1	Low	I/O	GPIO port D / LED blinker output
Y7	SSITXDA	1	Low	O	DAI/CODEC/SSI2 serial data output
Y8	ADCIN			I	SSI1 ADC serial input
Y9	VDDCORE			Core power	Digital core power, 2.5V
Y10	DRIVE[0]	2	Input‡	I/O	PWM drive output
Y11	SMPCLK	1	Low	O	SSI1 ADC sample clock
Y12	FB[1]			I	PWM feedback input
Y13	COL[6]	1	High	O	Keyboard scanner column drive
Y14	COL[3]	1	High	O	Keyboard scanner column drive
Y15	COL[1]	1	High	O	Keyboard scanner column drive
Y16	D[31]	1	Low	I/O	Data I/O
Y17	D[28]	1	Low	I/O	Data I/O
Y18	D[27]	1	Low	I/O	Data I/O
Y19	A[25]/DRA[2]	2	Low	O	System byte address / SDRAM address



TOP VIEW

SIDE VIEW



BOTTOM VIEW

JEDEC #: MO-151
Ball Diameter: 0.50 mm ± 0.10 mm
17 ¥ 17 ¥ 1.61 mm body

Table W. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
44	T3	N1	nEXTFIQ	I	79
45	R1	L5	PE[2]/CLKSEL	I/O	80
46	R2	N2	PE[1]/BOOTSEL1	I/O	83
47	T1	M4	PE[0]/BOOTSEL0	I/O	86
53	T2	T2	PD[7]/SDQM[1]	I/O	89
54	V4	T3	PD[6/SDQM[0]]	I/O	92
55	W4	N5	PD[5]	I/O	95
56	Y4	R3	PD[4]	I/O	98
59	V5	T4	PD[3]	I/O	101
60	W5	N6	PD[2]	I/O	104
61	Y5	R4	PD[1]	I/O	107
62	V6	L7	PD[0]/LEDFLSH	O	110
68	W6	T6	SSIRXFR	I/O	122
69	Y6	K8	ADCIN	I	125
70	W8	R6	nADCCS	O	126
75	Y8	M8	DRIVE1	I/O	128
76	V9	T8	DRIVE0	I/O	131
77	W10	N8	ADCCLK	O	134
78	Y10	R8	ADCOUT	O	136
79	V11	N9	SMPCLK	O	138
80	W11	T9	FB1	I	140
82	Y11	M9	FB0	I	141
83	Y12	R9	COL7	O	142
84	W12	L9	COL6	O	144
85	V12	T10	COL5	O	146
86	Y13	K9	COL4	O	148
87	W13	R10	COL3	O	150
88	V13	N10	COL2	O	152
91	Y14	R11	COL1	O	154
92	W14	M10	COL0	O	156
93	A1	T12	BUZ	O	158
94	V14	L10	D[31]	I/O	160
95	Y15	R12	D[30]	I/O	163
96	W15	N11	D[29]	I/O	166
97	V15	T13	D[28]	I/O	169
99	Y16	R13	A[27]/DRA[0]	Out	172
100	W16	M11	D[27]	I/O	174
101	V16	T14	A[26]/DRA[1]	O	177

Table W. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
201	A7	D6	nMWE/nSDWE	O	358
202	B7	B4	nMOE/nSDCAS	O	360
204	C7	E6	nCS[0]	O	362
205	A6	A3	nCS[1]	O	364
206	B6	D5	nCS[2]	O	366
207	C6	B3	nCS[3]	O	368
208	A5	A2	nCS[4]	O	370

1) See EP7311 Users' Manual for pin naming / functionality.

2) For each pad, the JTAG connection ordering is input, output, then enable as applicable.

General Conventions

Hexadecimal numbers are presented with all letters in uppercase and a lowercase “h” appended or with a 0x at the beginning. For example, 0x14 and 03CAh are hexadecimal numbers. Binary numbers are enclosed in single quotation marks when in text (for example, ‘11’ designates a binary number). Numbers not indicated by an “h”, 0x or quotation marks are decimal.

Registers are referred to by acronym, with bits listed in brackets separated by a colon (:) (for example, CODR[7:0]), and are described in the EP7311 User’s Manual. The use of “TBD” indicates values that are “to be determined,” “n/a” designates “not available,” and “n/c” indicates a pin that is a “no connect.”

Pin Description Conventions

Abbreviations used for signal directions are listed in Table Z.

Table Z. Pin Description Conventions

Abbreviation	Direction
I	Input
O	Output
I/O	Input or Output