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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XA
Core Size	16-Bit
Speed	30MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	DMA, WDT
Number of I/O	33
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pxah30kfbe-557

DESCRIPTION

The powerful 16-bit XA CPU core and rich feature set make the XA-H3 and XA-H4 devices ideal for high-performance real-time applications such as industrial control and networking. By supporting of up to 32 MB of external memory, these devices provide a low-cost solution to embedded applications of any complexity. Features like DMA, memory controller and four advanced UARTs help solve I/O intensive tasks with a minimum of CPU load.

The XA-H3 feature set is a subset of the XA-H4 (see Table 1). The XA-H3/H4 devices are members of the Philips XA (eXtended Architecture) family of high performance 16-bit microcontrollers.

The XA-H3 and XA-H4 are designed to significantly minimize the need for external components.

FEATURES

- Large Memory Support (up to 6 MB external)
- De-multiplexed Address/Data Bus
- Six Programmable Chip Selects
  - Support for Unified Memory – allows easy user modification of all code
  - External ISP Flash support for easy code download
- Dynamic Bus Sizing – each of 6 Chip Selects can be programmed for 8-bit or 16-bit bus.
- Dynamic Bus Timing – each of 6 chip selects has individual programmable bus timing.
- 32 Programmable General Purpose I/O Pins
- Four UARTs with 230.4 kbps capability
- Eight DMA Channels

Table 1. XA-H3 and XA-H4 features comparison

Feature	XA-H3	XA-H4
Maximum External Memory (Harvard Memory Mode)	6 MB	32 MB (16 MB Code, 16 MB Data)
Maximum External Memory (Unified Memory Mode)	6 MB	16 MB
Memory Controller supports both Harvard and Unified architectures	Yes	Yes
De-multiplexed Address/Data Bus	Yes	Yes
DRAM Controller	No	Yes
DMA Channels	8	8
Dynamic Bus Sizing	Yes	Yes
Dynamic Bus Timing	Yes	Yes
Programmable Chip Selects	6	6
General Purpose IO Pins	33	33
Potential Interrupt Pins	16	16
Interrupts (programmable priority)	7 Standard SW 4 High Priority SW 13 Hardware Event	7 Standard SW 4 High Priority SW 13 Hardware Event
Counter/Timers	2 plus Watchdog	2 plus Watchdog
Baud Rate Generators[1]	4	4
Serial Ports	4 UARTS	4 USARTS
Maximum Serial Data Rates	asynch to 230.4 kbps (no sync)	asynch to 230.4 kbps sync to 1 Mbps
Match Characters	No	4 async chars per USART
Hardware Autobaud	No	up to 230.4 kbps
SCP/SPI Bus	No	

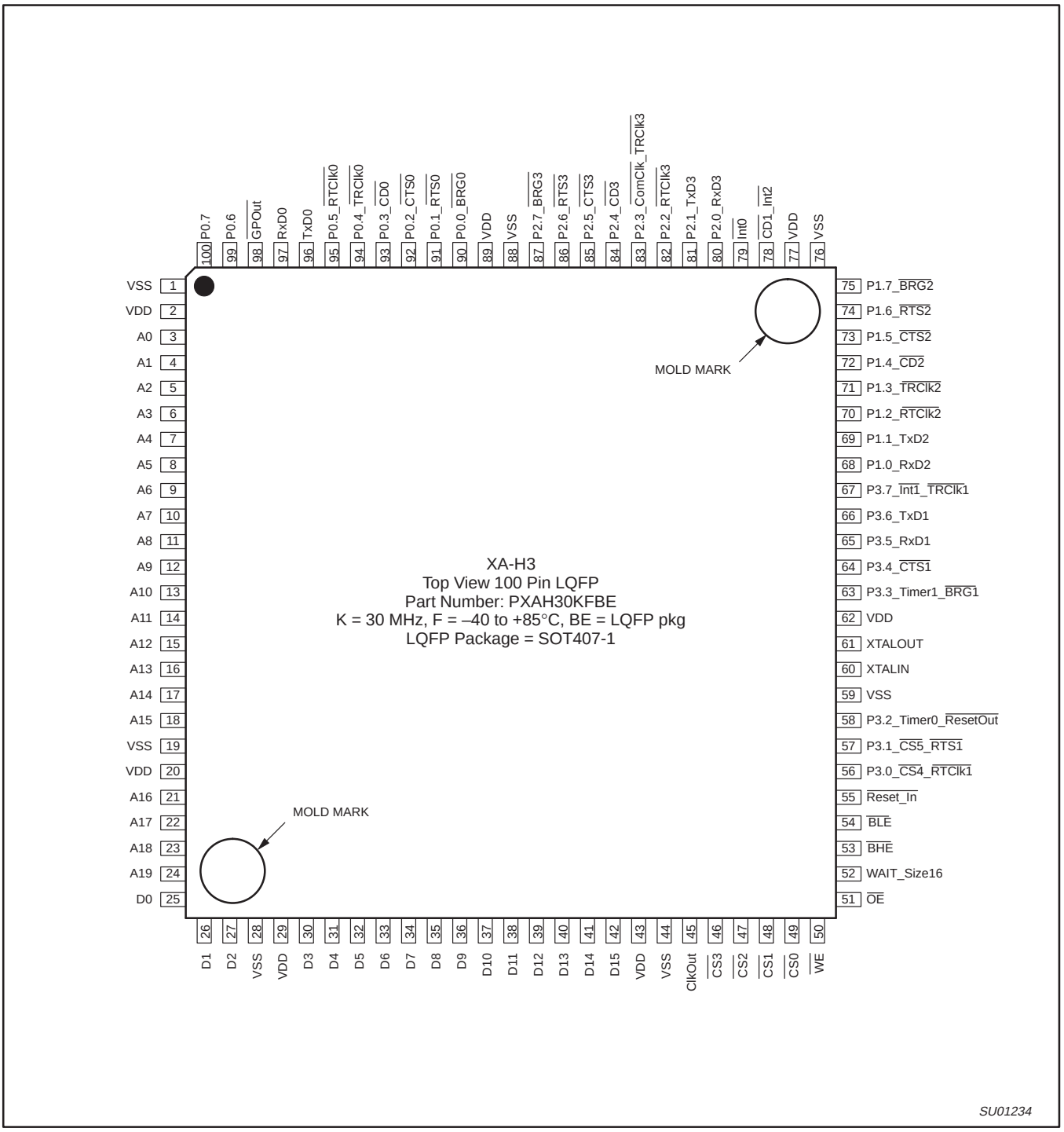
NOTE:
1. Can be used as additional counters if not needed as BRGs.

ORDERING INFORMATION

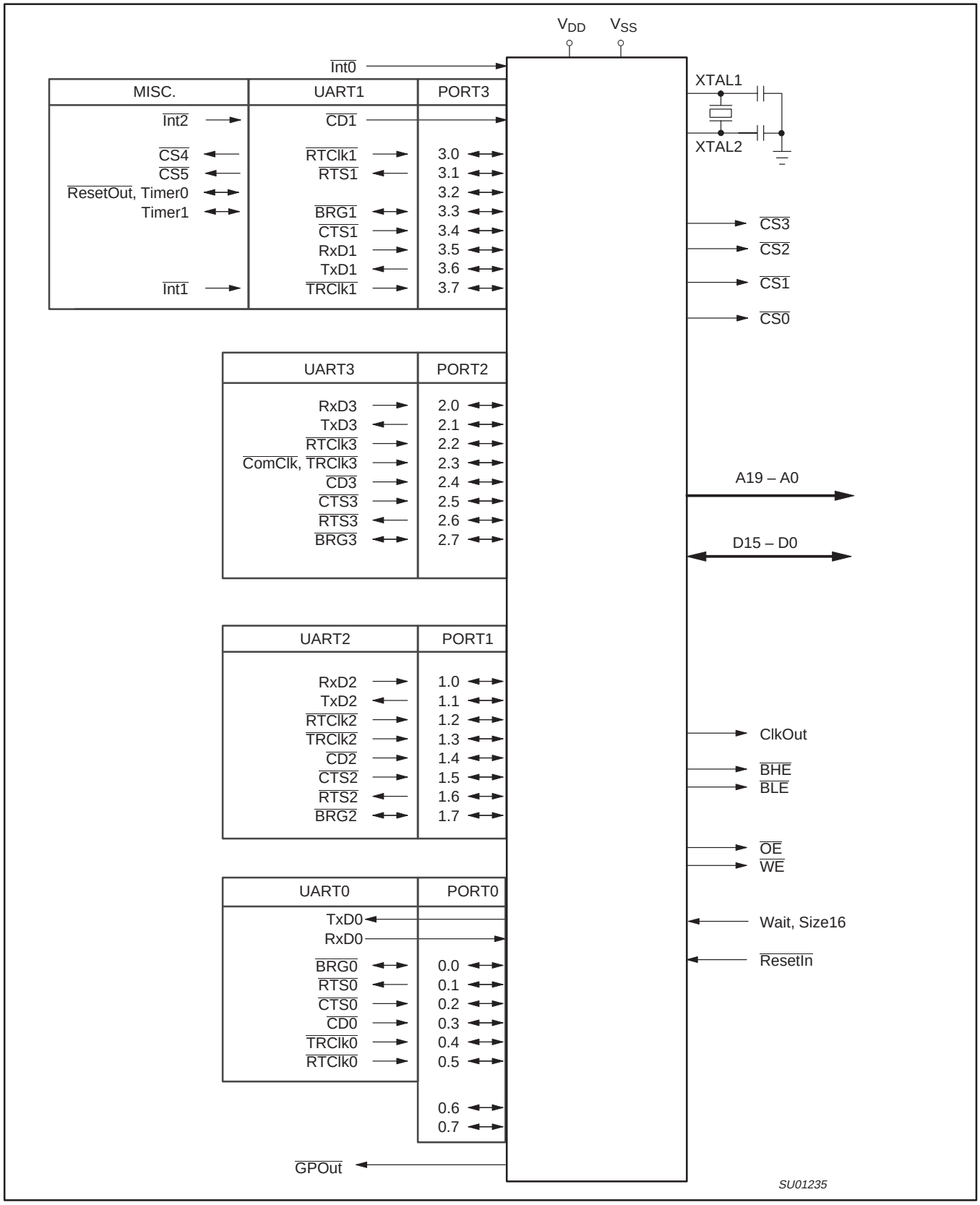
ROMless Only	Temperature range °C and Package	Freq (MHz)	Package Drawing Number
H3 = PXAH30KFBE	–40 to +85°C, 100-Pin Low Profile Quad Flat Package (LQFP)	30	SOT407-1

NOTE
K=30 MHz, F = (–40 to +85), BE = LQFP

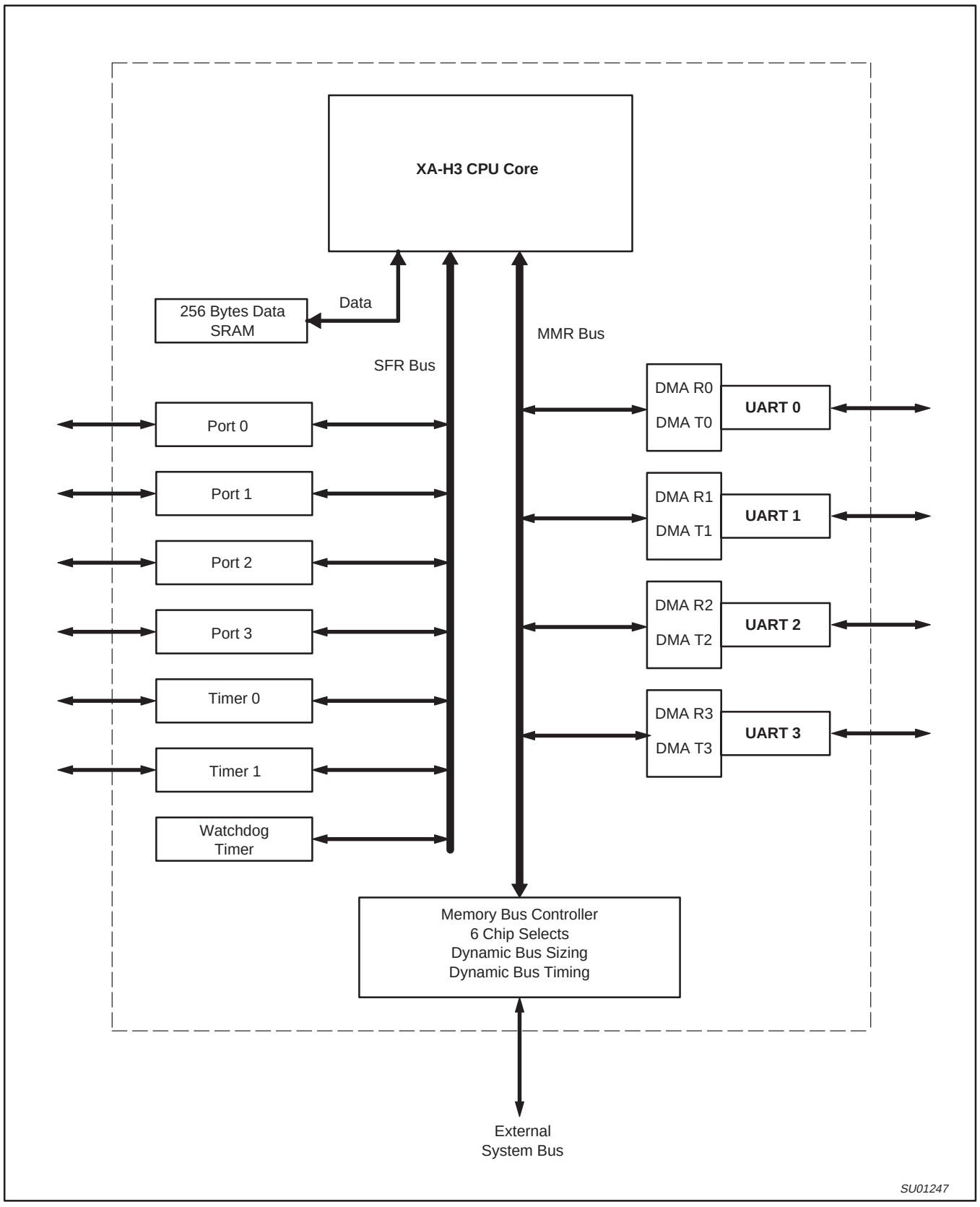
PIN CONFIGURATION



LOGIC SYMBOL XA-H3



XA-H3 BLOCK DIAGRAM



CONTROL REGISTER OVERVIEW

There are two types of control registers in the XA-H3, these are SFRs (Special Function Registers), and MMRs (Memory Mapped Registers.) The SFR registers, with the exception of MRBL, MRBH, MICFG, BCR, BRTH, BRTL, and RSTSRC are the standard XA core registers. See **WARNINGs** about BCR, BRTH, and BRTL in Table 2.

SFRs are accessed by "direct addressing" only (see *IC25 XA User Manual* for direct addressing.) The MMRs are specific to the XA-H3 on-chip peripherals, and can be accessed by any addressing mode that can be used for off-chip data accesses. The MMRs are implemented in a relocatable block. See the "Memory Controller" chapter in the *XA-H3 User Manual* for details on how to relocate the MMRs by writing a new base address into the MRBL and MRBH (MMR Base Low and High) registers.

Table 2. Special Function Registers (SFR)

Name	Description	SFR Address	Bit Functions and Addresses MSB → LSB								Reset Value
BCR	Bus Configuration Reg RESERVED – see Warning	46Ah	**WARNING** – Never write to the BCR register in the XA-H3 – it is initialized to 07h, the only legal value. This is not the same as for some other XA derivatives.								07h
BTRH	Bus Timing Reg High	469h	**WARNING** – Immediately after reset, always write BTRH = 51h, followed by writing BTRL = 40h in that order. Follow these two writes with five NOPS. This is not the same as for some other XA derivatives.								FFh
BTRL	Bus Timing Reg Low	468h									EFh
MRBL#	MMR Base Address Low	496h	MA15	MA14	MA13	MA12	–	–	–	MRBE	x0h
MRBH#	MMR Base Address High	497h	MA23	MA22	MA21	MA20	MA19	MA18	MA17	MA16	xx
MICFG#	ClkOut Tri-St Enable 1 = Enabled	499h	–	–	–	–	–	–	–	CLKOE	01h
CS	Code Segment	443h									00h
DS	Data Segment	441h									00h
ES	Extra Segment	442h									00h
			33F	33E	33D	33C	33B	33A	339	338	
IEH*	Interrupt Enable High	427h	EHSWR3	EHSWR2	EHSWR1	EHSWR0	–	EAuto	ESC23	ESC01	00h
			337	336	335	334	333	332	331	330	
IEL*	Interrupt Enable Low	426h	EA	EDMAH	EDMAL	EX2	ET1	EX1	ET0	EX0	00h
IPA0	Interrupt Priority A0	4A0h	–	PT0			–	PX0			00h
IPA1	Interrupt Priority A1	4A1h	–	PT1			–	PX1			00h
IPA2	Interrupt Priority A2	4A2h	–	PDMAL			–	PX2			00h
IPA3	Interrupt Priority A3	4A3h	Reserved				–	PDMAH			00h
IPA4	Interrupt Priority A4	4A4h	–	PSC23			–	PSC01			00h
IPA5	Interrupt Priority A5	4A5h	–	–			–	PAutoB			00h
IPA6	Interrupt Priority A6	4A6h	–	PHSWR1			–	PHSWR0			00h
IPA7	Interrupt Priority A7	4A7h	–	PHSWR3			–	PHSWR2			00h
			387	386	385	384	383	382	381	380	
P0*	Port 0	430h									FFh
			38F	38E	38D	38C	38B	38A	389	388	
P1*	Port 1	431h									FFh
			397	396	395	394	393	392	391	390	
P2*	Port 2	432h									FFh
			39F	39E	39D	39C	39B	39A	399	398	
P3*	Port 3	433h									FFh

Name	Description	SFR Address	Bit Functions and Addresses MSB							LSB	Reset Value
P0CFGA	Port 0 Configuration A	470h									5
P1CFGA	Port 1 Configuration A	471h									5
P2CFGA	Port 2 Configuration A	472h									5
P3CFGA	Port 3 Configuration A	473h									5
P0CFGB	Port 0 Configuration B	4F0h									5
P1CFGB	Port 1 Configuration B	4F1h									5
P2CFGB	Port 2 Configuration B	4F2h									5
P3CFGB	Port 3 Configuration B	4F3h									5
			227	226	225	224	223	222	221	220	
PCON*	Power Control Reg	404h	–	–	–	–	–	–	PD	IDL	00h
			20F	20E	20D	20C	20B	20A	209	208	
PSWH*	Program Status Word High	401h	SM	TM	RS1	RS0	IM3	IM2	IM1	IM0	2
			207	206	205	204	203	202	201	200	
PSWL*	Program Status Word Low	400h	C	AC	–	–	–	V	N	Z	2
			217	216	215	214	213	212	211	210	
PSW51*	80C51 Compatible PSW	402h	C	AC	F0	RS1	RS0	V	F1	P	3
RSTSRC	Reset Source Reg	463h	ROEN	–	–	–	–	R_WD	R_CMD	R_EXT	7
RTH0	Timer 0 Reload High	455h									00h
RTH1	Timer 1 Reload High	457h									00h
RTL0	Timer 0 Reload Low	454h									00h
RTL1	Timer 1 Reload Low	456h									00h
SCR	System Configuration Reg	440h	–	–	–	–	PT1	PT0	CM	PZ	00h
			21F	21E	21D	21C	21B	21A	219	218	
SSEL*	Segment Selection Reg	403h	ESWEN	R6SEG	R5SEG	R4SEG	R3SEG	R2SEG	R1SEG	R0SEG	00h
SWE	Software Interrupt Enable	47Ah	–	SWE7	SWE6	SWE5	SWE4	SWE3	SWE2	SWE1	00h
			357	356	355	354	353	352	351	350	
SWR*		42Ah	–	SWR7	SWR6	SWR5	SWR4	SWR3	SWR2	SWR1	00h
			287	286	285	284	283	282	281	280	
TCON*	Timer 0/1 Control	410h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h
TH0	Timer 0 High	451h									00h
TH1	Timer 1 High	453h									00h
TL0	Timer 0 Low	450h									00h
TL1	Timer 1 Low	452h									00h
TMOD	Timer 0/1 Mode	45Ch	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00h

MMR Name	Read/Write or Read Only	Size	Address Offset	Description	Reset Value
UART1 Write Register 14	R/W	8	85Ch	Miscellaneous Control bits	xx
UART1 Write Register 15	R/W	8	85Eh	External / Status interrupt control	f8h
Reserved – do not write		8	868h	Reserved – do not write	00h
Reserved – do not write		8	86Ah	Reserved – do not write	00h
UART1 Read Register 0	RO	8	860h	Tx/Rx buffer and external status	
UART1 Read Register 1	RO	8	862h	Receive condition status	
Reserved – do not write			864h		
UART1 Read Register 3	RO	8	866	Interrupt Pending Bits	
Reserved – do not write		8	86Ch	Reserved – do not write	
Reserved – do not write		8	86Eh	Reserved – do not write	
UART1 Read Register 8	RO	8	870h	Receive Buffer	
Reserved – do not write			872h		
UART1 Read Register 10	RO	8	874h	Clock status	
Reserved – do not write			876-87Eh		
UART2 Registers					
UART2 Write Register 0	R/W	8	880h	Command register	00h
UART2 Write Register 1	R/W	8	882h	Tx/Rx Interrupt & data transfer mode	xx
UART2 Write Register 2	R/W	8	884h	Extended Features Control	xx
UART2 Write Register 3	R/W	8	886h	Receive Parameter and Control	00h
UART2 Write Register 4	R/W	8	888h	Tx/Rx miscellaneous parameters & mode	00h
UART2 Write Register 5	R/W	8	88Ah	Tx. parameter and control	00h
Reserved – do not write		8	88Ch	Reserved – do not write	00h
Reserved – do not write		8	88Eh	Reserved – do not write	xx
UART2 Write Register 8	R/W	8	890h	Transmit Data Buffer	xx
UART2 Write Register 9	R/W	8	892h	Master Interrupt control	xx
UART2 Write Register 10	R/W	8	894h	Miscellaneous Tx/Rx control register	00h
UART2 Write Register 11	R/W	8	896h	Clock Mode Control	xx
UART2 Write Register 12	R/W	8	898h	Lower Byte of Baud rate time constant	00h
UART2 Write Register 13	R/W	8	89Ah	Upper Byte of Baud rate time constant	00h
UART2 Write Register 14	R/W	8	89Ch	Miscellaneous Control bits	xx
UART2 Write Register 15	R/W	8	89Eh	External / Status interrupt control	f8h
Reserved – do not write		8	8A8h	Reserved – do not write	00h
Reserved – do not write		8	8AAh	Reserved – do not write	00h
UART2 Read Register 0	RO	8	8A0h	Tx/Rx buffer and external status	
UART2 Read Register 1	RO	8	8A2h	Receive condition status	
Reserved – do not write			8A4h		
UART2 Read Register 3	RO	8	8A6h	Interrupt Pending Bits	
Reserved – do not write		8	8ACh	Reserved – do not write	
Reserved – do not write		8	8AEh	Reserved – do not write	
UART2 Read Register 8	RO	8	8B0h	Receive Buffer	
Reserved – do not write			8B2h		
UART2 Read Register 10	RO	8	8B4h	Clock status	
Reserved – do not write			8B6-8BEh		

MMR Name	Read/Write or Read Only	Size	Address Offset	Description	Reset Value
Data FIFO Register Ch.0 Tx	R/W	16	14Eh	14E = Byte2 = older 14F = Byte3 = younger	0000h
DMA Control Register Ch.1 Tx	R/W	8	150h	Control Register	00h
FIFO Control & Status Register Ch.1 Tx	R/W	8	151h	Control & Status Register	00h
Segment Register Ch.1 Tx	R/W	8	152h	Points to 64 k data segment	00h
Buffer Base Register Ch.1 Tx	R/W	8	154h	Wrap Reload Value for A15 – A8, A7 – A0 reloaded to zero by hardware	00h
Buffer Bound Register Ch.1 Tx	R/W	16	156h	Upper Bound (plus 1) on A15 – A0	0000h
Address Pointer Reg Ch.1 Tx	R/W	16	158h	Current Address pointer A15 – A0	0000h
Byte Count Register Ch.1 Tx	R/W	16	15Ah	Corresponds to A15 – A0 Byte Count, generates interrupt if enabled and byte count exceeded.	0000h
Data FIFO Register Ch.1 Lo Tx	R/W	16	15Ch	Byte0 & 1	0000h
Data FIFO Register Ch.1 Hi Tx	R/W	16	15Eh	Byte2 & 3	0000h
DMA Control Register Ch.2 Tx	R/W	8	160h	Control Register	00h
FIFO Control & Status Register Ch.2 Tx	R/W	8	161h	Control & Status Register	00h
Segment Register Ch.2 Tx	R/W	8	162h	Points to 64 k data segment	00h
Buffer Base Register Ch.2 Tx	R/W	8	164h	Wrap Reload Value for A15 – A8, A7 – A0 reloaded to zero by hardware	00h
Buffer Bound Register Ch.2 Tx	R/W	16	166h	Upper Bound (plus 1) on A15 – A0	0000h
Address Pointer Reg Ch.2 Tx	R/W	16	168h	Current Address pointer A15 – A0	0000h
Byte Count Register Ch.2 Tx	R/W	16	16Ah	Corresponds to A15 – A0 Byte Count, generates interrupt if enabled and byte count exceeded.	0000h
Data FIFO Register Ch.2 Lo Tx	R/W	16	16Ch	Byte0 & 1	0000h
Data FIFO Register Ch.2 Hi Tx	R/W	16	16Eh	Byte2 & 3	0000h
DMA Control Register Ch.3 Tx	R/W	8	170h	Control Register	00h
FIFO Control & Status Register Ch.3 Tx	R/W	8	171h	Control & Status Register	00h
Segment Register Ch. 3 Tx	R/W	8	172h	Points to 64 k data segment	00h
Buffer Base Register Ch. 3 Tx	R/W	8	174h	Wrap Reload Value for A15 – A8, A7 – A0 reloaded to zero by hardware	00h
Buffer Bound Register Ch.3 Tx	R/W	16	176h	Upper Bound (plus 1) on A15 – A0	0000h
Address Pointer Reg Ch.3 Tx	R/W	16	178h	Current Address pointer A15 – A0	0000h
Byte Count Register Ch.3 Tx	R/W	16	17Ah	Corresponds to A15 – A0 Byte Count, generates interrupt if enabled and byte count exceeded.	0000h
Data FIFO Register Ch.3Lo Tx	R/W	16	17Ch	Byte0 & 1	0000h
Data FIFO Register Ch.3 Hi Tx	R/W	16	17Eh	Byte2 & 3	0000h
	R/W		180-1FEh	RESERVED for future DMA	–
Miscellaneous DMA Registers					
Rx Character Time Out Register Ch.0	R/W	8	200h	0 value disables counter interrupt.	00h
Rx Character Time Out Register Ch.1	R/W	8	202h	Same as above, for Rx1	00h
Rx Character Time Out Register Ch.2	R/W	8	204h	Same as above, for Rx2	00h
Rx Character Time Out Register Ch.3	R/W	8	206h	Same as above, for Rx3	00h
Global DMA Interrupt Register	R/W	16	210h	DMA Interrupt Flags	0000h
GPOut	R/W	8	260h	GPOut[7] drives pin 98 ($\overline{\text{GPOut}}$) through an inverter. GPOut[6-0] are unused, and must be written with zeroes.	8xh

MMR Name	Read/Write or Read Only	Size	Address Offset	Description	Reset Value
Memory Interface (MIF) Registers					
B0CFG	R/W	8	280h	MIF Bank 0 Config	0Fh
B0AM	R/W	8	281h	MIF Bank 0 Base Address	00h
B0TMG	R/W	8	282h	MIF Bank 0 Timing Params	
B1CFG	R/W	8	284h	MIF Bank 1 Config	
B1AM	R/W	8	285h	MIF Bank 1 Base Address	
B1TMG	R/W	8	286h	MIF Bank 1 Timing Params	
B2CFG	R/W	8	288h	MIF Bank 2 Config	
B2AM	R/W	8	289h	MIF Bank 2 Base Address	
B2TMG	R/W	8	28Ah	MIF Bank 2 Timing Params	
B3CFG	R/W	8	28Ch	MIF Bank 3 Config	
B3AM	R/W	8	28Dh	MIF Bank 3 Base Address	
B3TMG	R/W	8	28Eh	MIF Bank 3 Timing Params	
B4CFG	R/W	8	290h	MIF Bank 4 Config	
B4AM	R/W	8	291h	MIF Bank 4 Base Address	
B4TMG	R/W	8	292h	MIF Bank 4 Timing Params	
B5CFG	R/W	8	294h	MIF Bank 5 Config	
B5AM	R/W	8	295h	MIF Bank 5 Base Address	
B5TMG	R/W	8	296h	MIF Bank 5 Timing Params	
MBCL	R/W	8	2BEh	MIF Memory Bank Configuration Lock Register	
Reserved – do not write	R/W	8	2BFh	Reserved – do not write	
Miscellaneous Registers					
Hi-Pri Soft Ints & Pin Mux Control Reg.	R/W	16	2D0h	Control bits for Hi-Priority Soft Ints, and Pin Mux	0000h
XInt2	R/W	8	2D2h	External Interrupt 2 Control	00h

FUNCTIONAL DESCRIPTION

The XA-H3 functions are described in the following sections. Because all blocks are thoroughly documented in either the *IC25 XA Data Handbook*, or the *XA-H3 User Manual*, only brief descriptions are given in this datasheet, in conjunction with references to the appropriate document.

XA CPU

The CPU is a 30 MHz implementation of the standard XA CPU core. See the *XA Data Handbook* (IC25) for details. The CPU core is identical to the G3 core. See caveat in next paragraph about the Bus Interface Unit.

Bus Interface Unit (BIU)

This is the internal Bus, not the bus at the pins. This internal bus connects the CPU to Memory Controller.

WARNING: Immediately after reset, always write BTRH = 51h, followed by BTRL = 40h, in that order. Once written, do not change the values in these registers. Follow these two writes with five NOPS. Never write to the BCR register, it comes out of reset initialized to 07h, which is the only value that will work.

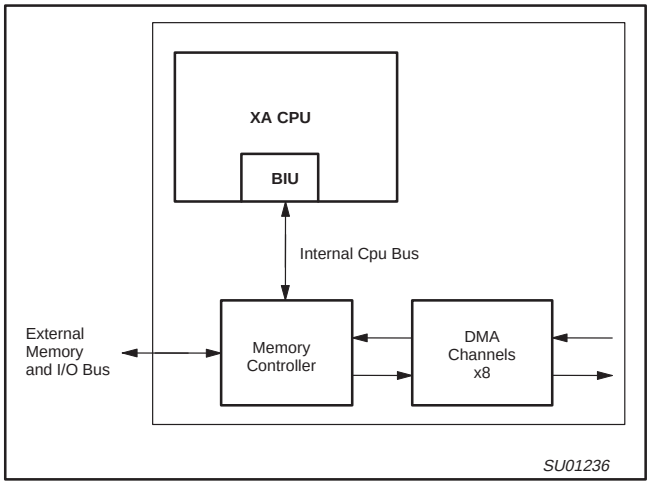


Figure 1. XA CPU Core BIU (Bus Interface Unit)

Each memory bank and associated chip select is capable of supporting a 1 MB address space (six chip selects can thus support 6 MB of SRAM and other generic devices.)

The Memory Interface can be programmed to support both Intel style and 68000 bus style SRAMs and peripherals.

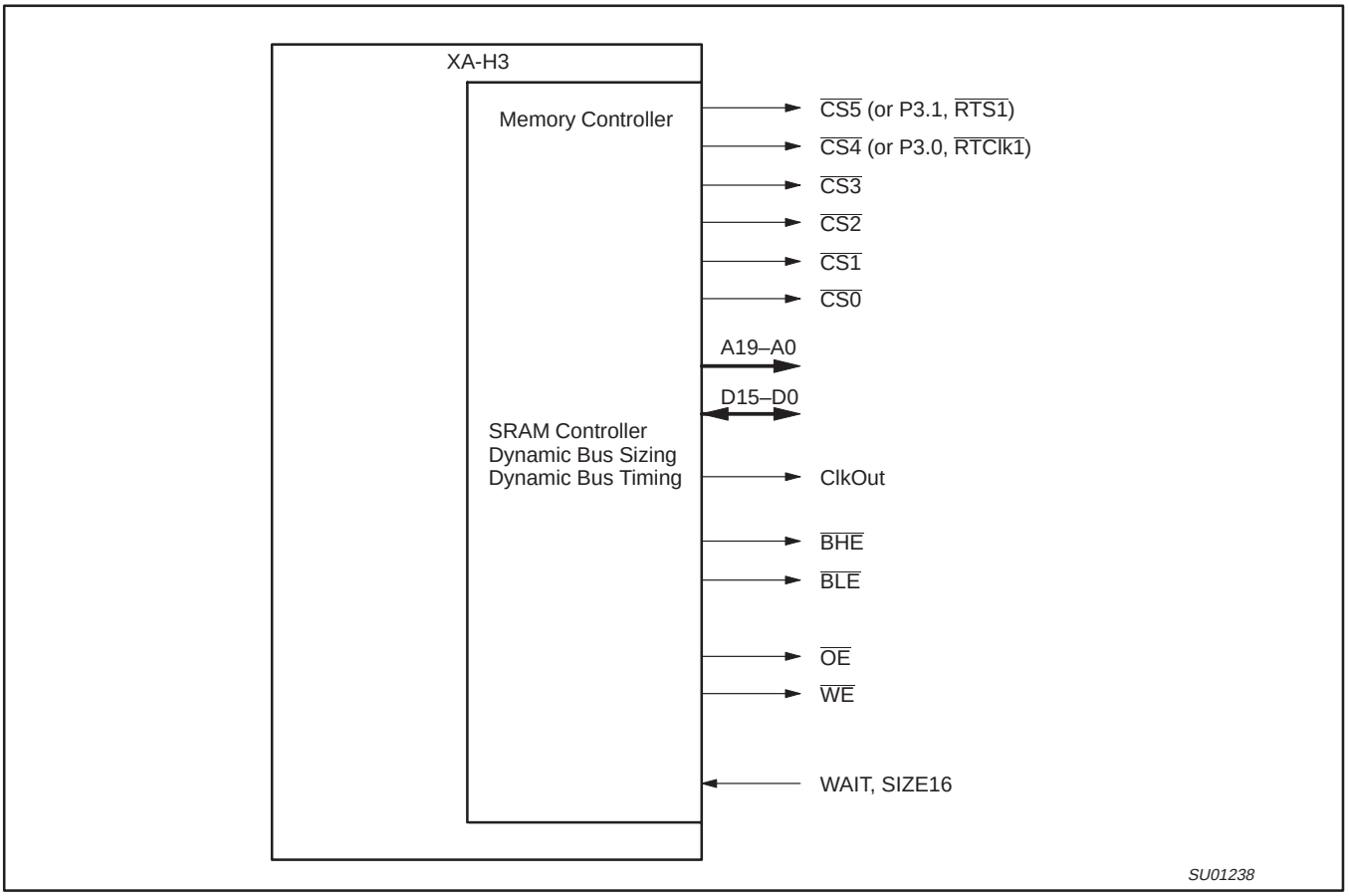


Figure 3. Memory Bus Interface Signal Pins

Bus Interface Pins

For the following discussion, see Figure 3.

Chip Select Pins

There are six chip select pins ($\overline{CS5}$ – $\overline{CS0}$)mapped to six sets of bank control registers. The following attributes are individually programmable for each bank and associated chip select : bank on/off, address range, external device access time, detailed bus strobe sequence, and bus width.

WARNING: On the external bus, **ALL** XA-H3 reads are 16-bit Reads. If the CPU instruction only specifies 8-bits, then the CPU uses the appropriate byte, and discards the extra byte. Thus “8-Bit Reads” and “16-Bit Reads” appear to be identical on the bus. **On an 8-bit bus, this will appear as two consecutive 8-bit reads** even though the CPU instruction specified a byte read.

Some 8-bit I/O devices (especially FIFOs) cannot operate correctly with 2 bytes being Read for a 1 Byte Read. The most common (and least expensive) solution is to operate these 8-bit devices on a 16-bit bus, and access them in software on all odd byte (or all even byte) boundaries. An added benefit of this technique is that byte reads are faster than on an 8-bit bus, because only 1 word is fetched (a single read) instead of 2 consecutive bytes.

Clock Output

The CLKOUT pin allows easier external bus interfacing in some situations. This output reflects the XTALIn clock input to the XA (referred to internally as CClk or System Clock), but is delayed to match the external bus outputs and strobes. The default is for CLKOUT to be output enabled at reset, but it may be turned off (tri-state disabled) by software via the MICFG MMR.
WARNING: The capacitive loading on this output must not exceed 40 pf.

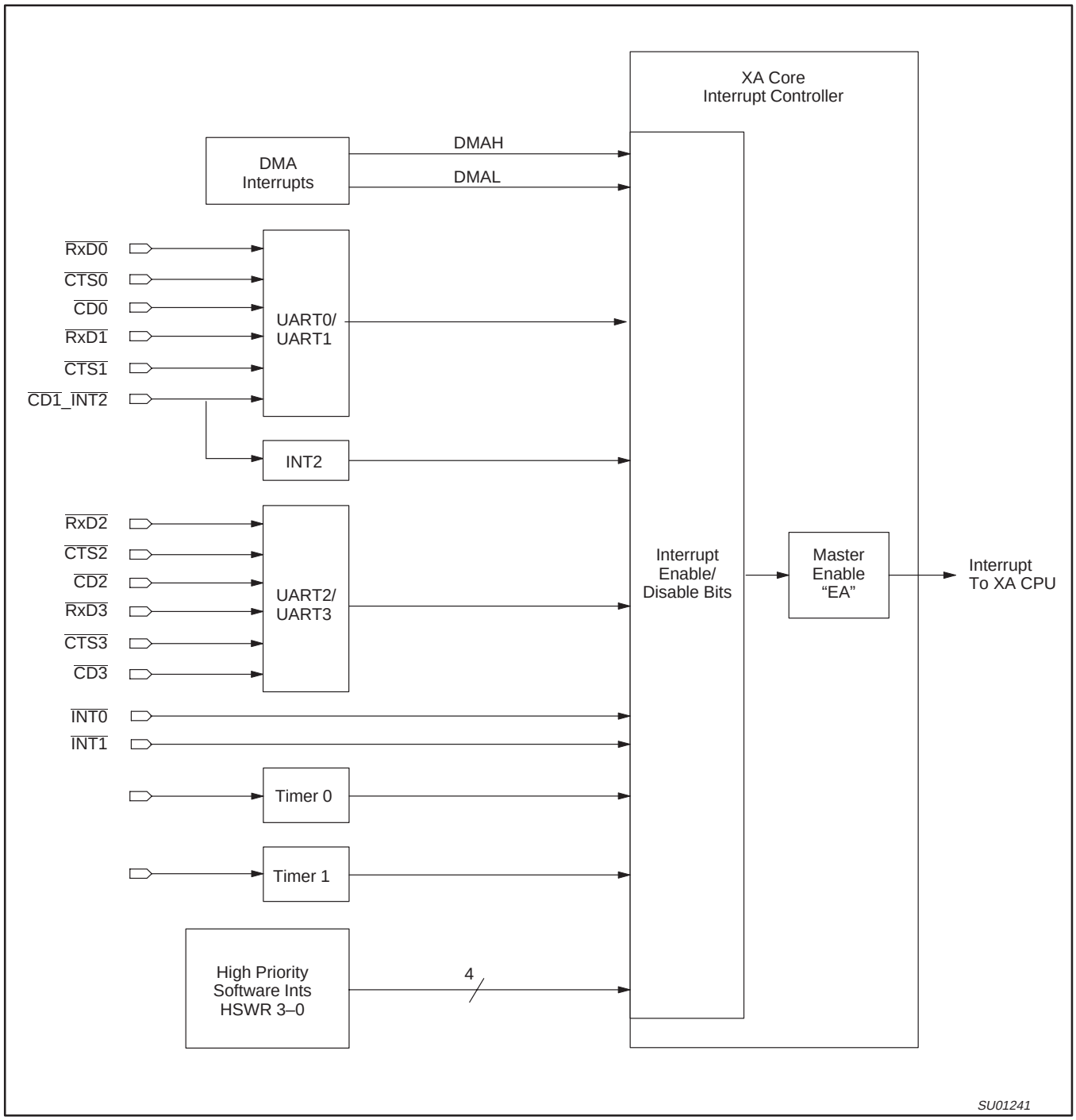


Figure 6. XA-H3 Interrupt Structure Overview

Table 7. UART0 Interrupts (Interrupt structure is the same except for bit locations for all 4 UARTs)

Potential UART0 Interrupt	Individual Enable Bit MMR Hex Offset	Source Bit MMR Hex Offset	Group Enable Bit(S) MMR Hex Offset	Group Flag Bit MMR Hex Offset	Master Enable Bit MMR Hex Offset
Rx Character Available	–	RR0[0] 820[0]	WR1[4:3] 802[4:3]	Even Channel Rx IP RR3[5] 826[5]	UART0/1 Master Interrupt Enable WR9[3] 812[3]
CRC/Framing Error	–	RR1[6] 822[6]			
Rx Overrun	–	RR1[5] 822[5]			
Parity Error	WR1[2] 802[2]	RR1[4] 822[4]			
Tx Buffer Empty	See WR1[1]	RR0[2] 820[2]	Tx Interrupt Enable WR1[1] 802[1]	Even Channel Tx IP RR3[4] 826[4]	
Break/Abort	Break/ Abort IE WR15[7] 81E[7]	RR0[7] 820[7]	Master External/Status Interrupt Enable WR1[0] 802[0]	Even Channel External/Status IP RR3[3] 826[3]	
Tx Underrun/EOM	Tx Underrun/EOM IE WR15[6] 81E[6]	RR0[6] 820[6]			
CTS	CTS IE WR15[5] 81E[5]	RR0[5] 820[5]			
DCD	DCD IE WR15[3] 81E[3]	RR0[3] 820[3]			
Zero Count	Zero Count IE WR15[1] 81E[1]	RR0[1] 820[1]			

EXCEPTION/TRAPS PRECEDENCE

Description	Vector Address	Arbitration Ranking
Reset (h/w, watchdog, s/w)	0000–0003	0 (High)
Break Point	0004–0007	1
Trace	0008–000B	1
Stack Overflow	000C–000F	1
Divide by 0	0010–0013	1
User RETI	0014–0017	1
TRAP 0–15 (software)	0040–007F	1

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Operating temperature under bias	–55 to +125	°C
Storage temperature range	–65 to +150	°C
Voltage on any other pin to V_{SS}	–0.5 to V_{DD}+0.5 V	v
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer, not device power consumption)	1.5	W

PRELIMINARY DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5.0 V +/– 10% or 3.3 V +/– 10% unless otherwise specified; T_{amb} = –40°C to +85°C for industrial, unless otherwise specified.

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
I_{DD}	Power supply current, operating	5.0 V, 30 MHz		64	80	mA
		3.3 V, 30 MHz		55	70	mA
I_{ID}	Power supply current, Idle mode	5.0 V, 30 MHz		50	70	mA
		3.3 V, 30 MHz		44	60	mA
I_{PDI}	Power supply current, Power Down mode[1]	5.0 V, 3.0 V			500	µA
V_{RAM}	RAM keep-alive voltage		1.5			V
V_{IL}	Input low voltage		–0.5		0.22 V_{DD}	V
V_{IH}	Input high voltage, except Xtal1, RST		2.2			V
V_{IH1}	Input high voltage to Xtal1, RST	For both 3.0 & 5.0 V	0.7 V_{DD}			V
V_{OL}	Output low voltage all ports[8]	I_{OL} = 3.2 mA, V_{DD} = 4.5 V			0.5	V
		I_{OL} = 1.0 mA, V_{DD} = 3.0 V			0.4	V
V_{OH1}	Output high voltage, all ports	I_{OH} = –100 µA, V_{DD} = 4.5 V	2.4			V
		I_{OH} = –30 µA, V_{DD} = 3.0 V	2.0			V
V_{OH2}	Output high voltage, all ports	I_{OH} = 3.2 mA, V_{DD} = 4.5 V	2.4			V
		I_{OH} = 1.0 mA, V_{DD} = 3.0 V	2.2			V
C_{IO}	Input/Output pin capacitance				15	pF
I_{IL}	Logical 0 input current, all ports[7]	V_{IN} = 0.45 V			–50	µA
I_{LI}	Input leakage current, all ports[6]	V_{IN} = V_{IL} or V_{IH}			±10	µA
I_{TL}	Logical 1 to 0 transition current, all ports[5]	At V_{DD} = 5.5 V			–650	µA
		At V_{DD} = 3.6 V			–250	µA

NOTE:
1. V_{DD} must be raised to within the operating range before power down mode is exited.
2. Ports in quasi-bidirectional mode with weak pullup.
3. Ports in PUSH-PULL mode, both pullup and pulldown assumed to be the same strength.
4. In all output modes.
5. Port pins source a transition current when used in quasi-bidirectional mode and externally driven from 1 to 0. This current is highest when V_{IN} is approximately 2 V.
6. Measured with port in high impedance mode.
7. Measured with port in quasi-bidirectional mode.
8. Under steady state (non-transient) conditions, IOL must be externally limited as follows:
   Maximum I_{OL} per port pin: 15 mA (NOTE: This is +85°C specification for V_{DD} = 5 V)
   Maximum I_{OL} per 8-bit port: 26 mA
   Maximum total I_{OL} for all outputs: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

PRELIMINARY AC ELECTRICAL CHARACTERISTICS (5.0 V +/–10%)

Symbol	Figure	Parameter	Limits		Unit
			Min	Max	
All Cycles					
F_C		System Clock Frequency	0	30	MHz
t_C	13	System Clock Period = 1/FC	33.33	–	ns
t_{CHCX}	13	XTALIN High Time	t_C* 0.5	–	ns
t_{CLCX}	13	XTALIN Low Time	t_C* 0.4	–	ns
t_{CLCH}	13	XTALIN Rise Time	–	5	ns
t_{CHCL}	13	XTALIN Fall Time	–	5	ns
t_{AVSL}	All	Address Valid to Strobe low	t_C – 21	–	ns
t_{CHAH}	All	Address hold after CLKOUT rising edge [7]	1	–	ns
t_{CHAV}	All	Delay from CLKOUT rising edge to address valid	–	25	ns
t_{CHSH}	All	Delay from CLKOUT rising edge to Strobe High[7]	1	21	ns
t_{CHSL}	All	Delay from CLKOUT rising edge to Strobe Low[7]	1	19	ns
t_{CODH}	14	ClkOut Duty Cycle High (into 40 pF max.)	t_{CHCX}–7	t_{CHCX}+3	ns
Data Read Only					
t_{AHDR}	10	Address hold (A19 – A1 only, not A0) after $\overline{CS}$, $\overline{BLE}$, $\overline{BHE}$ rise at end of Data Read Cycle (not code fetch)	t_C – 12	–	ns
Data Read and Instruction Fetch Cycles					
t_{DIS}	7, 8, 10, 11	Data In Valid setup to ClkOut rising edge	25	–	ns
t_{DIH}	7, 8, 10, 11	Data In Valid hold after ClkOut rising edge [2]	0	–	ns
t_{OHDE}	10	$\overline{OE}$ high to XA Data Bus Driver Enable	t_C – 14	–	ns
Write Cycles					
t_{CHDV}	9	Clock High to Data Valid	–	25	ns
t_{DVSL}	12	Data Valid prior to Strobe Low	t_C – 23	–	ns
t_{SHAH}	9, 12	Minimum Address Hold Time after strobe goes inactive	t_C – 25	–	ns
t_{SHDH}	9, 12	Data hold after strobes ($\overline{CS}$ and $\overline{BHE}$/$\overline{BLE}$) high	t_C – 25	–	ns
Wait Input					
t_{WS}	15	WAIT setup (stable high or low) to CLKOUT rising edge	20	–	ns
t_{WH}	15	WAIT hold (stable high or low) after CLKOUT rising edge	0	–	ns

NOTE:

1. On a 16-bit bus, if only one byte is being written, then only one of $\overline{BLE}$ or $\overline{BHE}$ will go active. On an 8-bit bus, $\overline{BLE}$ goes active for all (odd or even address) accesses. $\overline{BHE}$ will not go active during any accesses on an 8 bit bus.
2. The bus timing is designed to make meeting hold time very straightforward without glue logic. On all reads and fetches, in order to meet hold time, the slave should hold data valid on the bus until the earliest of $\overline{CS}$, $\overline{BHE}$/$\overline{BLE}$, $\overline{OE}$, goes high (inactive), or until the address changes.
3. To avoid 3-State fights during read cycles and fetch cycles, do not drive data bus until $\overline{OE}$ goes active
4. **WARNING:** ClkOut is specified at 40 pF max. More than 40 pf on ClkOut may significantly degrade the ClkOut waveform. Load capacitance for all outputs (except ClkOut) = 80 pF.
5. Not all combinations of bus timing configuration values result in valid bus cycles. Please refer to the *XA-H3 User Manual* for details.
6. When code is being fetched on the external bus, a burst mode fetch is used. This burst can be from 2 to 16 bytes long. On a 16-bit bus, A3 – A1 are incremented for each new word of the burst. On an 8-bit bus, A3 – A0 are incremented for each new byte of the burst code fetch.
7. The MIN value for this parameter is guaranteed by design and is not tested in production to the specified limit. In those cases where a maximum value is specified in the table for this parameter, it is tested.

AC ELECTRICAL CHARACTERISTICS (3.3 V +/–10%)

Vdd = 3.3 V +/– 10%; T_{amb} = –40°C to +85°C (industrial)

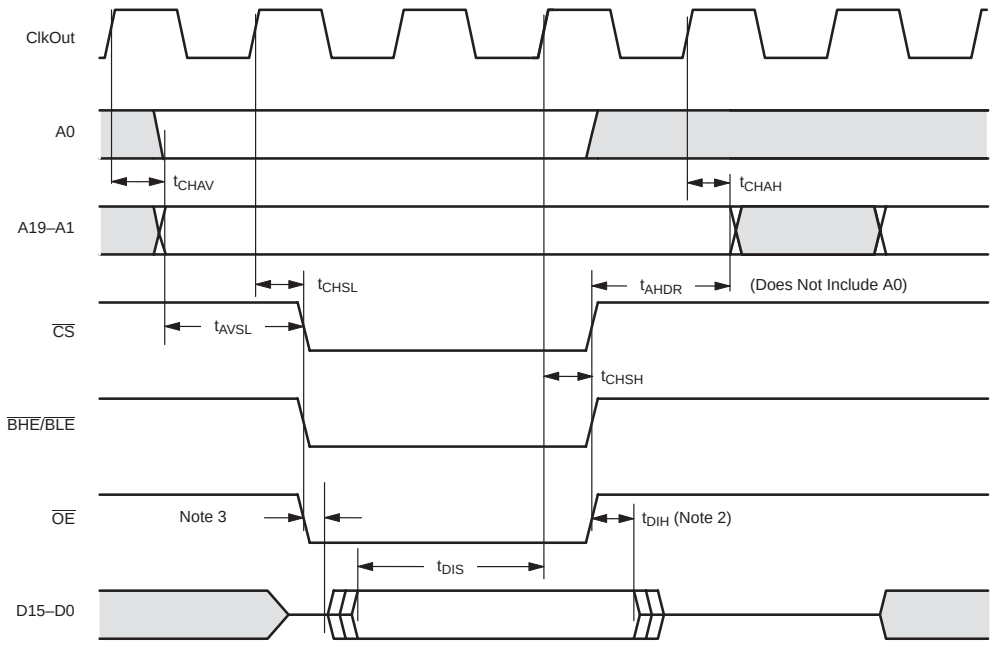
Symbol	Figure	Parameter	Limits		Unit
			Min	Max	
All Cycles					
F_C		System Clock (internally called CClk) Frequency	0	30	MHz
t_C	13	System Clock Period = 1/FC	33.33	–	ns
t_{CHCX}	13	XTALIN High Time	t_C* 0.5	–	ns
t_{CLCX}	13	XTALIN Low Time	t_C* 0.4	–	ns
t_{CLCH}	13	XTALIN Rise Time	–	5	ns
t_{CHCL}	13	XTALIN Fall Time	–	5	ns
t_{AVSL}	All	Address Valid to Strobe low	t_C – 21	–	ns
t_{CHAH}	All	Address hold after CLKOUT rising edge [7]	1	–	ns
t_{CHAV}	All	Delay from CLKOUT rising edge to address valid	–	30	ns
t_{CHSH}	All	Delay from CLKOUT rising edge to Strobe High [7]	1	28	ns
t_{CHSL}	All	Delay from CLKOUT rising edge to Strobe Low [7]	1	25	ns
t_{CODH}	14	ClkOut Duty Cycle High (into 40 pF max.)	t_{CHCX}–7	t_{CHCX}+3	ns
Data Read Only					
t_{AHDR}	10	Address hold (A19 – A1 only, not A0) after $\overline{CS}$, $\overline{BLE}$, $\overline{BHE}$ rise at end of Data Read Cycle (not code fetch)	t_C – 12	–	ns
Data Read and Instruction Fetch Cycles					
t_{DIS}	7, 8, 10, 11	Data In Valid setup to ClkOut rising edge	32	–	ns
t_{DIH}	7, 8, 10, 11	Data In Valid hold after ClkOut rising edge [2]	0	–	ns
t_{OHDE}	10	$\overline{OE}$ high to XA Data Bus Driver Enable	t_C – 19	–	ns
Write Cycles					
t_{CHDV}	9	Clock High to Data Valid	–	30	ns
t_{DVSL}	12	Data Valid prior to Strobe Low	t_C – 23	–	ns
t_{SHAH}	9, 12	Minimum Address Hold Time after strobe goes inactive	t_C – 25	–	ns
t_{SHDH}	9, 12	Data hold after strobes ($\overline{CS}$ and $\overline{BHE}$/$\overline{BLE}$) high	t_C – 25	–	ns
Wait Input					
t_{WS}	15	WAIT setup (stable high or low)prior to CLKOUT rising edge	25	–	ns
t_{WH}	15	WAIT hold (stable high or low) after CLKOUT rising edge	0	–	ns

NOTE:

1. On a 16-bit bus, if only one byte is being written, then only one of $\overline{BLE}$ or $\overline{BHE}$ will go active. On an 8-bit bus, $\overline{BLE}$ goes active for all (odd or even address) accesses. $\overline{BHE}$ will not go active during any accesses on an 8-bit bus.
2. The bus timing is designed to make meeting hold time very straightforward without glue logic. On all reads and fetches, in order to meet hold time, the slave should hold data valid on the bus until the earliest of $\overline{CS}$, $\overline{BHE}$/$\overline{BLE}$, $\overline{OE}$, goes high (inactive), or until the address changes.
3. To avoid 3-State fights during read cycles and fetch cycles, do not drive data bus until $\overline{OE}$ goes active
4. **WARNING:** ClkOut is specified at 40 pF max. More than 40 pf on ClkOut may significantly degrade the ClkOut waveform. Load capacitance for all outputs (except ClkOut) = 80 pF.
5. Not all combinations of bus timing configuration values result in valid bus cycles. Please refer to the *XA-H3 User Manual* for details.
6. When code is being fetched on the external bus, a burst mode fetch is used. This burst can be from 2 to 16 bytes long. On a 16-bit bus, A3 – A1 are incremented for each new word of the burst. On an 8-bit bus, A3 – A0 are incremented for each new byte of the burst code fetch.
7. The MIN value for this parameter is guaranteed by design and is not tested in production to the specified limit. In those cases where a maximum value is specified in the table for this parameter, it is tested.

TIMING DIAGRAMS

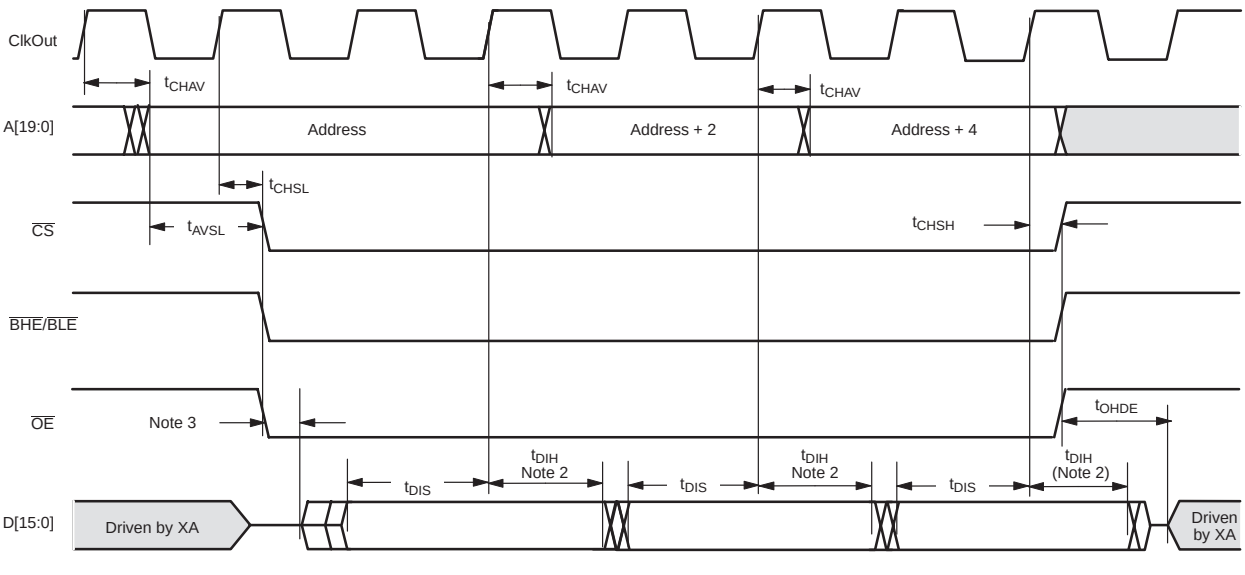
All references to numbered Notes are to the notes following the AC Electrical Characteristics tables



Note: On Generic Data Reads, A0 can terminate a full clock period before A19–A1, and therefore should not be used on some peripheral devices.

SU01277

Figure 7. Read on 16-Bit Bus



Note: The processor can prefetch from one to eight words.

SU01131

Figure 8. Burst Code Fetch on 16-Bit Bus

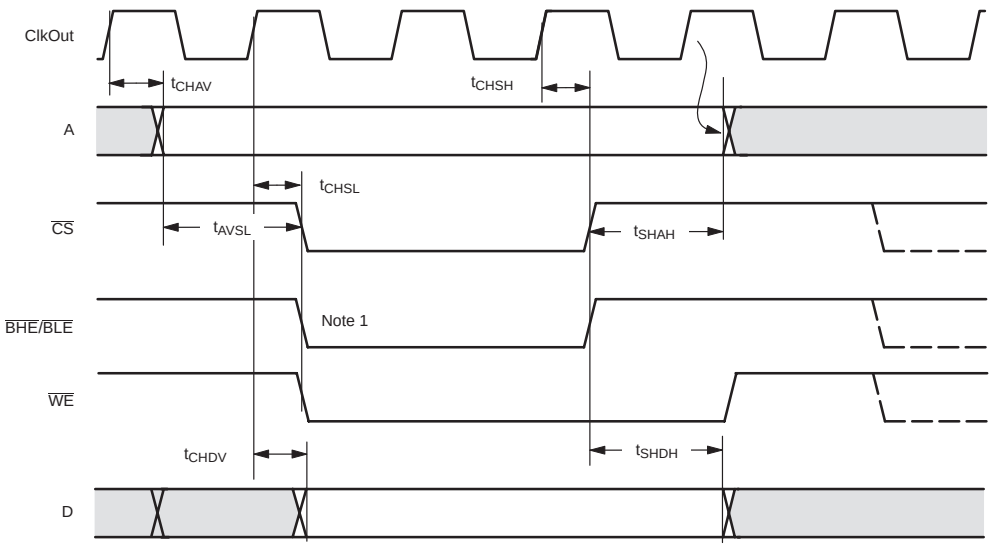
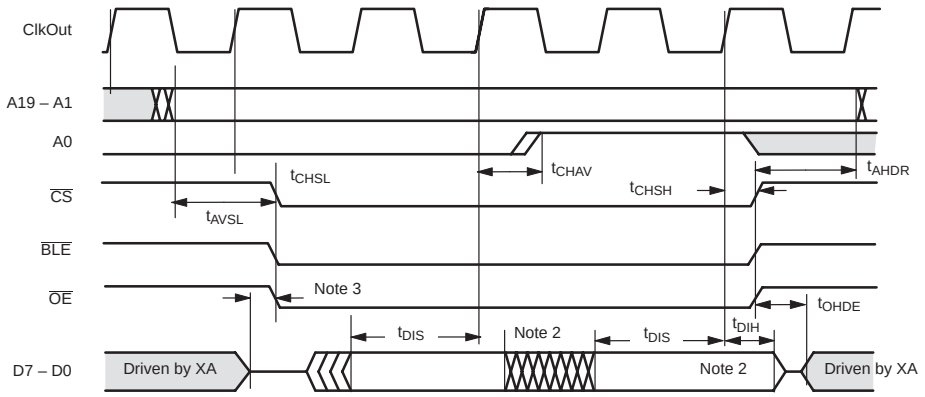


Figure 9. Write (byte write on 8-bit bus, or all writes on 16-bit bus)

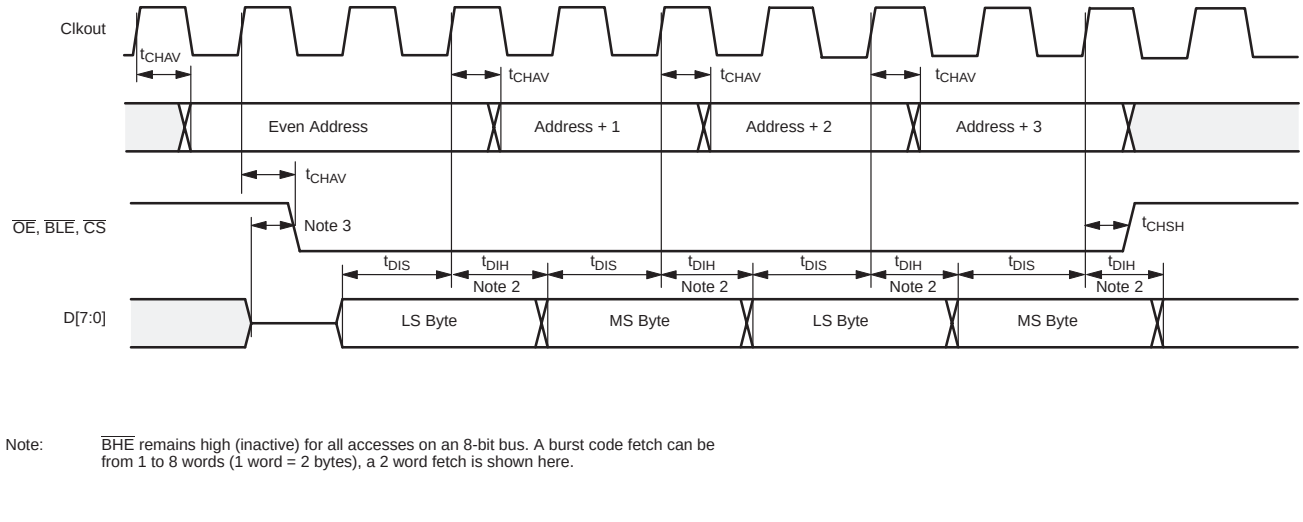


On all cycles on 8-bit bus, $\overline{BHE}$ remains high (inactive)

Note: On the external bus, ALL XA-H4 reads are 16-bit reads. If the CPU instruction only specifies 8-bits, then the CPU uses the appropriate byte, and discards the extra byte. Thus, “8-Bit Reads” and “16-Bit Reads” appear to be identical on the bus. On an 8-bit bus, this will appear as two consecutive 8-bit reads even though the CPU will only use one of the two bytes.

WARNING: Some 8-bit I/O devices (especially FIFOS) cannot operate correctly with 2 bytes being read for a one byte read. The most common (and least expensive) solution is to operate these 8-bit devices on a 16-bit bus, and access them in software on all odd byte (or all even byte) boundaries. An added benefit of this technique is that byte reads are faster than on an 8-bit bus, because only 1 word is fetched (a single read) instead of 2 consecutive bytes.

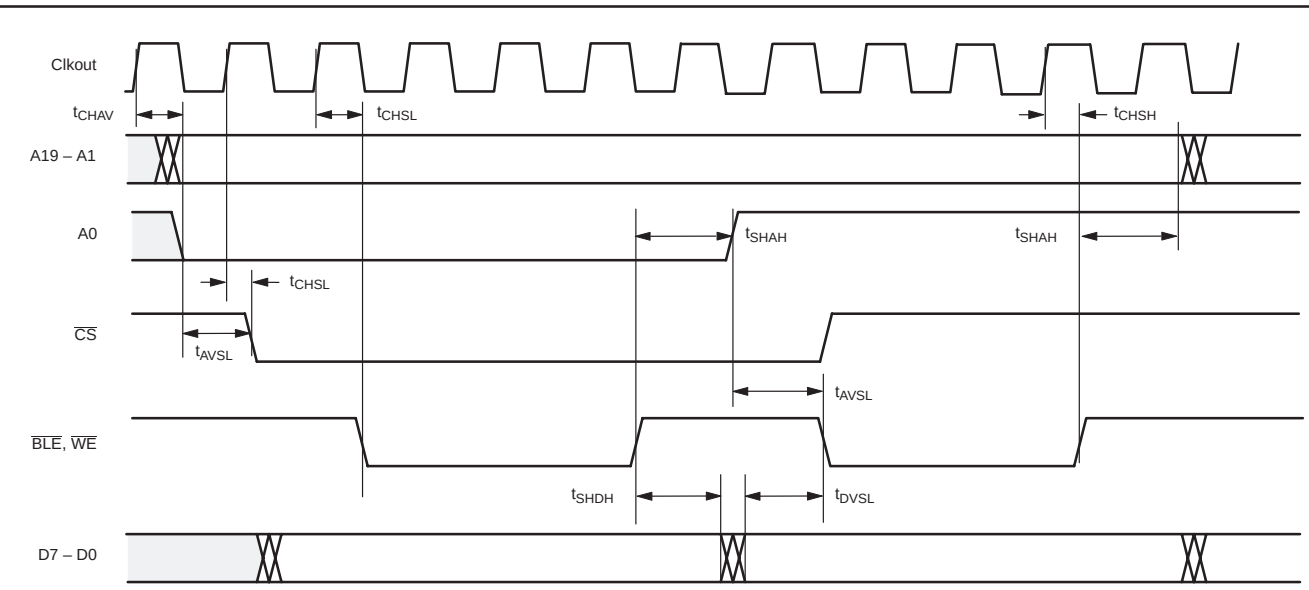
Figure 10. Read (16-Bit or 8-Bit) on 8 Bit Bus



Note: $\overline{BHE}$ remains high (inactive) for all accesses on an 8-bit bus. A burst code fetch can be from 1 to 8 words (1 word = 2 bytes), a 2 word fetch is shown here.

SU01245

Figure 11. Burst Code Fetch on 8-bit bus

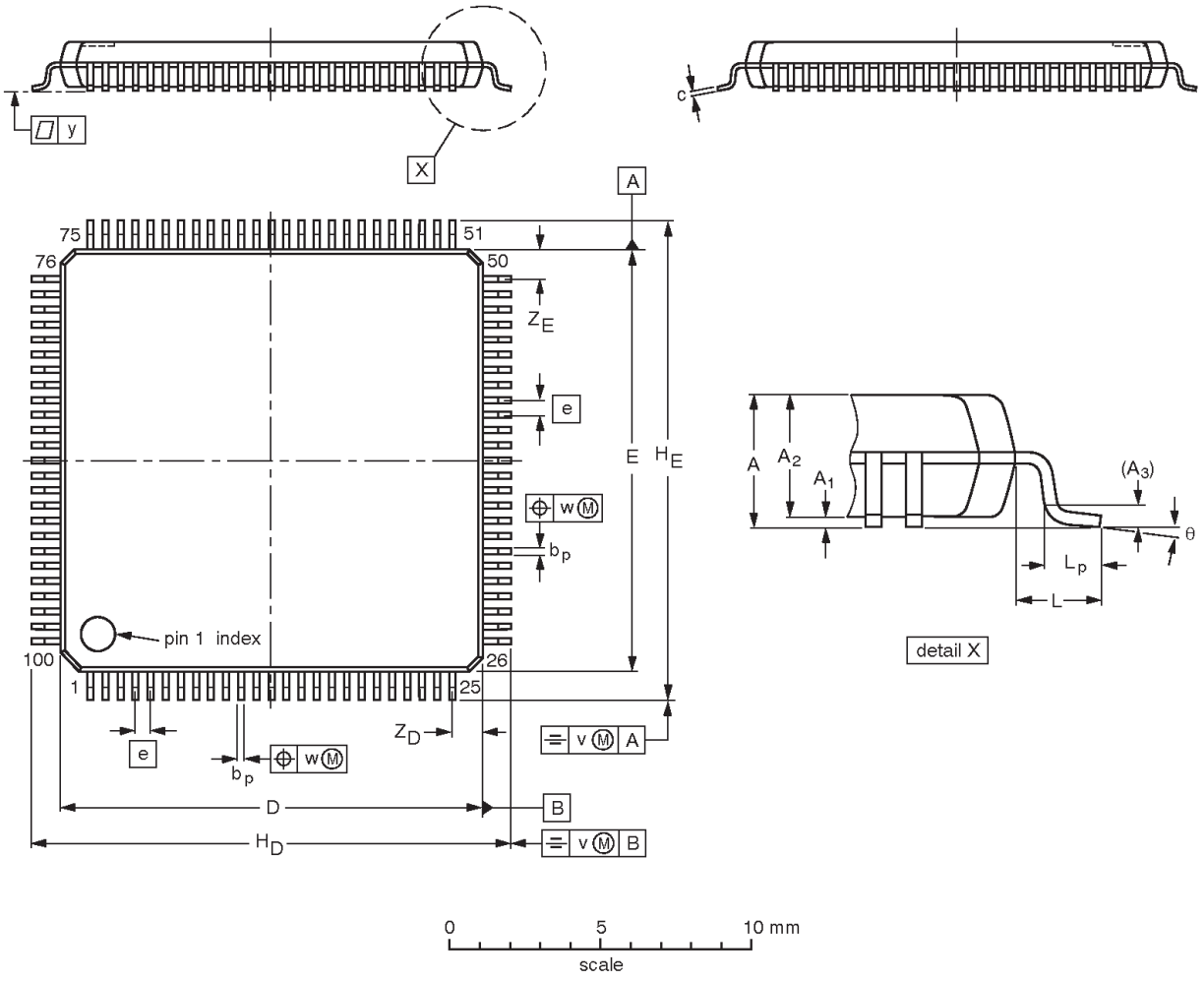


Note. $\overline{OE}$ is inactive during all writes.

SU01246

Figure 12. 16-Bit Write on 8-Bit Bus

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.5 1.3	0.25	0.28 0.16	0.18 0.12	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.2	0.12	0.1	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1						~~95-12-19~~ 97-08-04

NOTES