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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC140 Core
Interface	DSI, Ethernet, RS-232
Clock Rate	300MHz
Non-Volatile Memory	External
On-Chip RAM	1.436MB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	431-BFBGA, FCBGA
Supplier Device Package	431-FCPBGA (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmsc8122tmp4800v

1 Pin Assignments

This section includes diagrams of the MSC8122 package ball grid array layouts and pinout allocation tables.

1.1 FC-PBGA Ball Layout Diagrams

Top and bottom views of the FC-PBGA package are shown in **Figure 3** and **Figure 4** with their ball location index numbers.

Bottom View

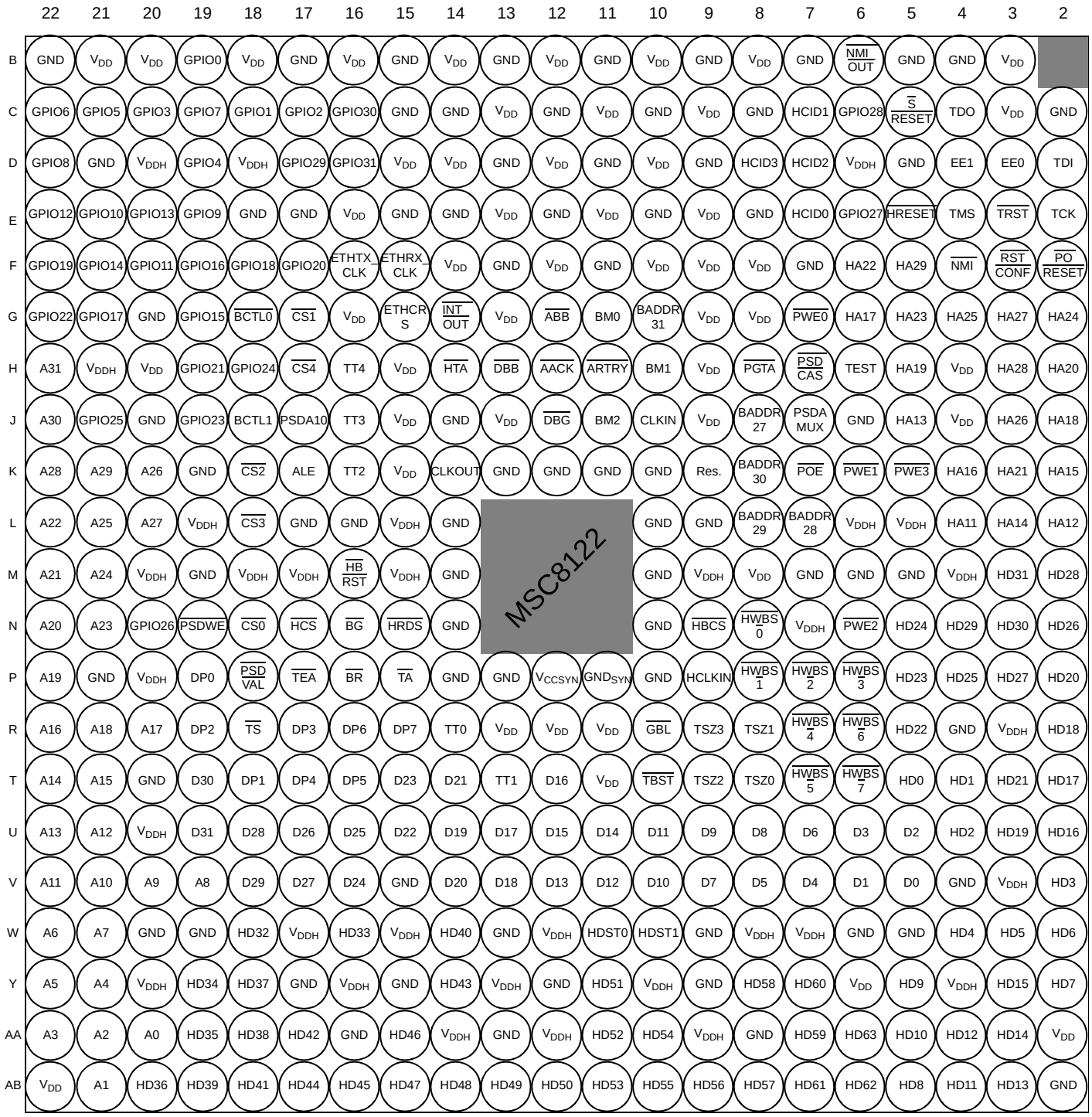


Figure 4. MSC8122 Package, Bottom View

Table 1. MSC8122 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
H21	V_{DDH}	K15	V_{DD}
H22	A31	K16	TT2/$\overline{CS5}$
J2	HA18	K17	ALE
J3	HA26	K18	$\overline{CS2}$
J4	V_{DD}	K19	GND
J5	HA13	K20	A26
J6	GND	K21	A29
J7	PSDAMUX/PGPL5	K22	A28
J8	BADDR27	L2	HA12
J9	V_{DD}	L3	HA14
J10	CLKIN	L4	HA11
J11	BM2/TC2/BNKSEL2	L5	V_{DDH}
J12	$\overline{DBG}$	L6	V_{DDH}
J13	V_{DD}	L7	BADDR28
J14	GND	L8	$\overline{IRQ5}$/BADDR29
J15	V_{DD}	L9	GND
J16	TT3/$\overline{CS6}$	L10	GND
J17	PSDA10/PGPL0	L14	GND
J18	$\overline{BCTL1}$/$\overline{CS5}$	L15	V_{DDH}
J19	GPIO23/TDM0TDAT/$\overline{IRQ13}$	L16	GND
J20	GND	L17	GND
J21	GPIO25/TDM0RCLK/$\overline{IRQ15}$	L18	$\overline{CS3}$
J22	A30	L19	V_{DDH}
K2	HA15	L20	A27
K3	HA21	L21	A25
K4	HA16	L22	A22
K5	$\overline{PWE3}$/$\overline{PSDDQM3}$/$\overline{PBS3}$	M2	HD28
K6	$\overline{PWE1}$/$\overline{PSDDQM1}$/$\overline{PBS1}$	M3	HD31
K7	$\overline{POE}$/$\overline{PSDRAS}$/PGPL2	M4	V_{DDH}
K8	$\overline{IRQ2}$/BADDR30	M5	GND
K9	Reserved	M6	GND
K10	GND	M7	GND
K11	GND	M8	V_{DD}
K12	GND	M9	V_{DDH}
K13	GND	M10	GND
K14	CLKOUT	M14	GND

Table 1. MSC8122 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
M15	V_{DDH}	P12	V_{CCSYN}
M16	$\overline{\text{HBRST}}$	P13	GND
M17	V_{DDH}	P14	GND
M18	V_{DDH}	P15	$\overline{\text{TA}}$
M19	GND	P16	$\overline{\text{BR}}$
M20	V_{DDH}	P17	$\overline{\text{TEA}}$
M21	A24	P18	$\overline{\text{PSDVAL}}$
M22	A21	P19	DP0/DREQ1/$\overline{\text{EXT\_BR2}}$
N2	HD26	P20	V_{DDH}
N3	HD30	P21	GND
N4	HD29	P22	A19
N5	HD24	R2	HD18
N6	$\overline{\text{PWE2}}$/$\overline{\text{PSDDQM2}}$/$\overline{\text{PBS2}}$	R3	V_{DDH}
N7	V_{DDH}	R4	GND
N8	$\overline{\text{HWBS0}}$/$\overline{\text{HDBS0}}$/$\overline{\text{HWBE0}}$/$\overline{\text{HDBE0}}$	R5	HD22
N9	$\overline{\text{HBCS}}$	R6	$\overline{\text{HWBS6}}$/$\overline{\text{HDBS6}}$/$\overline{\text{HWBE6}}$/$\overline{\text{HDBE6}}$/$\overline{\text{PWE6}}$/$\overline{\text{PSDDQM6}}$/$\overline{\text{PBS6}}$
N10	GND	R7	$\overline{\text{HWBS4}}$/$\overline{\text{HDBS4}}$/$\overline{\text{HWBE4}}$/$\overline{\text{HDBE4}}$/$\overline{\text{PWE4}}$/$\overline{\text{PSDDQM4}}$/$\overline{\text{PBS4}}$
N14	GND	R8	TSZ1
N15	$\overline{\text{HRDS}}$/HRW/$\overline{\text{HRDE}}$	R9	TSZ3
N16	$\overline{\text{BG}}$	R10	$\overline{\text{IRQ1}}$/$\overline{\text{GBL}}$
N17	$\overline{\text{HCS}}$	R11	V_{DD}
N18	$\overline{\text{CS0}}$	R12	V_{DD}
N19	$\overline{\text{PSDWE}}$/PGPL1	R13	V_{DD}
N20	GPIO26/TDM0RDAT	R14	TT0/HA7
N21	A23	R15	$\overline{\text{IRQ7}}$/DP7/DREQ4
N22	A20	R16	$\overline{\text{IRQ6}}$/DP6/DREQ3
P2	HD20	R17	$\overline{\text{IRQ3}}$/DP3/DREQ2/$\overline{\text{EXT\_BR3}}$
P3	HD27	R18	$\overline{\text{TS}}$
P4	HD25	R19	$\overline{\text{IRQ2}}$/DP2/$\overline{\text{DACK2}}$/$\overline{\text{EXT\_DBG2}}$
P5	HD23	R20	A17
P6	$\overline{\text{HWBS3}}$/$\overline{\text{HDBS3}}$/$\overline{\text{HWBE3}}$/$\overline{\text{HDBE3}}$	R21	A18
P7	$\overline{\text{HWBS2}}$/$\overline{\text{HDBS2}}$/$\overline{\text{HWBE2}}$/$\overline{\text{HDBE2}}$	R22	A16
P8	$\overline{\text{HWBS1}}$/$\overline{\text{HDBS1}}$/$\overline{\text{HWBE1}}$/$\overline{\text{HDBE1}}$	T2	HD17
P9	HCLKIN	T3	HD21
P10	GND	T4	HD1/DSISYNC
P11	GND_{SYN}	T5	HD0/SWTE

Table 1. MSC8122 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
T6	HWBS7/HDBS7/HWBE7/HDBE7/PWE7/PSDDQM7/PBS7	U21	A12
T7	HWBS5/HDBS5/HWBE5/HDBE5/PWE5/PSDDQM5/PBS5	U22	A13
T8	TSZ0	V2	HD3/MODCK1
T9	TSZ2	V3	V_{DDH}
T10	TBST	V4	GND
T11	V_{DD}	V5	D0
T12	D16	V6	D1
T13	TT1	V7	D4
T14	D21	V8	D5
T15	D23	V9	D7
T16	IRQ5/DP5/DACK4/EXT_BG3	V10	D10
T17	IRQ4/DP4/DACK3/EXT_DBG3	V11	D12
T18	IRQ1/DP1/DACK1/EXT_BG2	V12	D13
T19	D30	V13	D18
T20	GND	V14	D20
T21	A15	V15	GND
T22	A14	V16	D24
U2	HD16	V17	D27
U3	HD19	V18	D29
U4	HD2/DSI64	V19	A8
U5	D2	V20	A9
U6	D3	V21	A10
U7	D6	V22	A11
U8	D8	W2	HD6
U9	D9	W3	HD5/CNFGS
U10	D11	W4	HD4/MODCK2
U11	D14	W5	GND
U12	D15	W6	GND
U13	D17	W7	V_{DDH}
U14	D19	W8	V_{DDH}
U15	D22	W9	GND
U16	D25	W10	HDST1/HA10
U17	D26	W11	HDST0/HA9
U18	D28	W12	V_{DDH}
U19	D31	W13	GND
U20	V_{DDH}	W14	HD40/D40/ETHRXD0

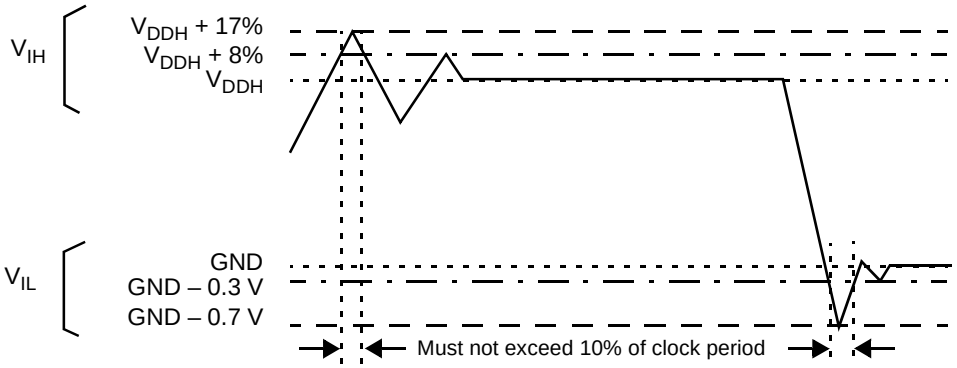


Figure 5. Overshoot/Undershoot Voltage for V_{IH} and V_{IL}

2.5 AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs. When systems such as DSP farms are developed using the DSI, use a device loading of 4 pF per pin. AC timings are based on a 20 pF load, except where noted otherwise, and a 50 Ω transmission line. For loads smaller than 20 pF, subtract 0.06 ns per pF down to 10 pF load. For loads larger than 20 pF, add 0.06 ns for SIU/Ethernet/DSI delay and 0.07 ns for GPIO/TDM/timer delay. When calculating overall loading, also consider additional RC delay.

2.5.1 Output Buffer Impedances

Table 6. Output Buffer Impedances

Output Buffers	Typical Impedance (Ω)
System bus	50
Memory controller	50
Parallel I/O	50
Note: These are typical values at 65°C. The impedance may vary by ±25% depending on device process and operating temperature.	

2.5.2 Start-Up Timing

Starting the device requires coordination among several input sequences including clocking, reset, and power. **Section 2.5.3** describes the clocking characteristics. **Section 2.5.4** describes the reset and power-up characteristics. You must use the following guidelines when starting up an MSC8122 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the power-up sequence. See **Table 11** for timing.
- If possible, bring up the V_{DD} and V_{DDH} levels together. For designs with separate power supplies, bring up the V_{DD} levels and then the V_{DDH} levels (see **Figure 7**).
- CLKIN should start toggling at least 16 cycles (starting after V_{DDH} reaches its nominal level) before $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation (see **Figure 6** and **Figure 7**).
- CLKIN must not be pulled high during V_{DDH} power-up. CLKIN can toggle during this period.

Note: See **Section 3.1** for start-up sequencing recommendations and **Section 3.2** for power supply design recommendations.

The following figures show acceptable start-up sequence examples. **Figure 6** shows a sequence in which V_{DD} and V_{DDH} are raised together. **Figure 7** shows a sequence in which V_{DDH} is raised after V_{DD} and CLKIN begins to toggle as V_{DDH} rises.

In all cases, the power-up sequence must follow the guidelines shown in **Figure 8**.

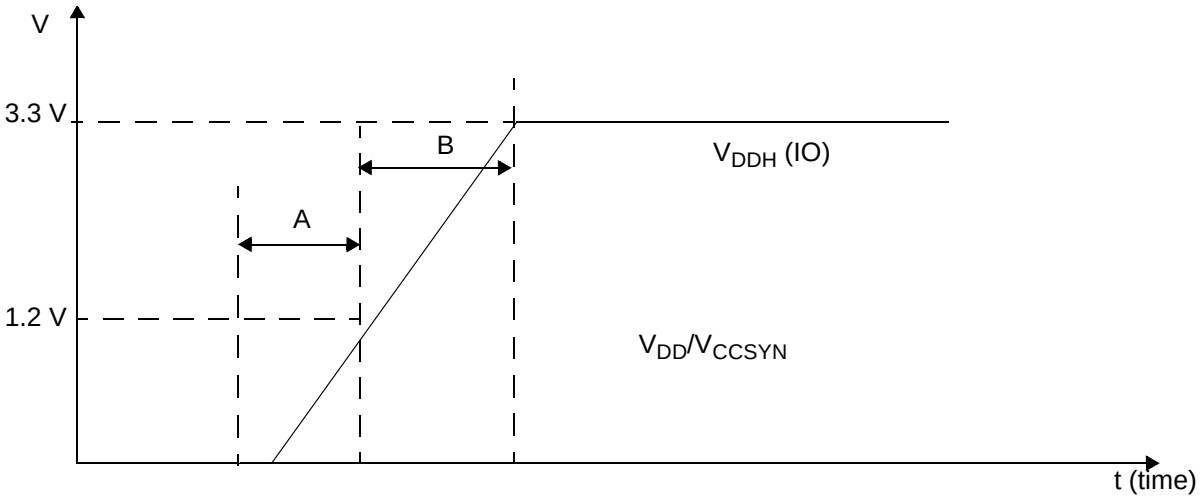


Figure 8. Power-Up Sequence for V_{DDH} and V_{DD}/V_{CCSYN}

The following rules apply:

1. During time interval A, V_{DDH} should always be equal to or less than the V_{DD}/V_{CCSYN} voltage level. The duration of interval A should be kept below 10 ms.
2. The duration of timing interval B should be kept as small as possible and less than 10 ms.

2.5.3 Clock and Timing Signals

The following sections include a description of clock signal characteristics. **Table 7** shows the maximum frequency values for internal (Core, Reference, Bus, and DSI) and external (CLKIN and CLKOUT) clocks. The user must ensure that maximum frequency values are not exceeded.

Table 7. Maximum Frequencies

Characteristic	Maximum in MHz
Core frequency	300/400/500
Reference frequency (REFCLK)	100/133/166
Internal bus frequency (BLCK)	100/133/166
DSI clock frequency (HCLKIN) • Core frequency = 300 MHz • Core frequency = 400/500 MHz	 HCLKIN ≤ (min{70 MHz, CLKOUT}) HCLKIN ≤ (min{100 MHz, CLKOUT})
External clock frequency (CLKIN or CLKOUT)	100/133/166

Table 8. Clock Frequencies

Characteristics	Symbol	300 MHz Device		400 MHz Device		500 MHz Device	
		Min	Max	Min	Max	Min	Max
CLKIN frequency	F_{CLKIN}	20	100	20	133.3	20	166.7
BCLK frequency	F_{BCLK}	40	100	40	133.3	40	166.7
Reference clock (REFCLK) frequency	F_{REFCLK}	40	100	40	133.3	40	166.7
Output clock (CLKOUT) frequency	F_{CLKOUT}	40	100	40	133.3	40	166.7
SC140 core clock frequency	F_{CORE}	200	300	200	400	200	500
Note: The rise and fall time of external clocks should be 3 ns maximum							

Table 9. System Clock Parameters

Characteristic	Min	Max	Unit
Phase jitter between BCLK and CLKIN	—	0.3	ns
CLKIN frequency	20	see **Table 8**	MHz
CLKIN slope	—	3	ns
CLKIN period jitter[1]	—	150	ps
CLKIN jitter spectrum	150	—	KHz
PLL input clock (after predivider)	20	100	MHz
PLL output frequency (VCO output) • 300 MHz core • 400 MHz core • 500 MHz core	800	 1200 1600 2000	MHz MHz MHz MHz
CLKOUT frequency jitter[1]	—	200	ps
CLKOUT phase jitter[1] with CLKIN phase jitter of ±100 ps.	—	500	ps

Notes: **1.** Peak-to-peak.
2. Not tested. Guaranteed by design.

2.5.4 Reset Timing

The MSC8122 has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)
- External hard reset ($\overline{\text{HRESET}}$)
- External soft reset ($\overline{\text{SRESET}}$)
- Software watchdog reset
- Bus monitor reset
- Host reset command through JTAG

All MSC8122 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 10** describes the reset sources.

Table 10. Reset Sources

Name	Direction	Description
Power-on reset ($\overline{\text{PORESET}}$)	Input	Initiates the power-on reset flow that resets the MSC8122 and configures various attributes of the MSC8122. On $\overline{\text{PORESET}}$, the entire MSC8122 device is reset. SPLL states is reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the SC140 extended cores are reset, and system configuration is sampled. The clock mode (MODCK bits), reset configuration mode, boot mode, Chip ID, and use of either a DSI 64 bits port or a System Bus 64 bits port are configured only when $\overline{\text{PORESET}}$ is asserted.
External hard reset ($\overline{\text{HRESET}}$)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC8122. While $\overline{\text{HRESET}}$ is asserted, $\overline{\text{SRESET}}$ is also asserted. $\overline{\text{HRESET}}$ is an open-drain pin. Upon hard reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the SC140 extended cores are reset, and system configuration is sampled. The most configurable features are reconfigured. These features are defined in the 32-bit hard reset configuration word described in *Hard Reset Configuration Word* section of the *Reset* chapter in the *MSC8122 Reference Manual*.
External soft reset ($\overline{\text{SRESET}}$)	Input/ Output	Initiates the soft reset flow. The MSC8122 detects an external assertion of $\overline{\text{SRESET}}$ only if it occurs while the MSC8122 is not asserting reset. $\overline{\text{SRESET}}$ is an open-drain pin. Upon soft reset, $\overline{\text{SRESET}}$ is driven, the SC140 extended cores are reset, and system configuration is maintained.
Software watchdog reset	Internal	When the MSC8122 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
Bus monitor reset	Internal	When the MSC8122 bus monitor count reaches zero, a bus monitor hard reset is asserted. The enabled bus monitor event then generates an internal hard reset sequence.
Host reset command through the TAP	Internal	When a host reset command is written through the Test Access Port (TAP), the TAP logic asserts the soft reset signal and an internal soft reset sequence is generated.

2.5.4.3 Reset Timing Tables

Table 12 and **Figure 9** describe the reset timing for a reset configuration write through the direct slave interface (DSI) or through the system bus.

Table 12. Timing for a Reset Configuration Write through the DSI or System Bus

No.	Characteristics	Expression	Min	Max	Unit
1	Required external PORESET duration minimum • CLKIN = 20 MHz • CLKIN = 100 MHz (300 MHz core) • CLKIN = 133 MHz (400 MHz core) • CLKIN = 166 MHz (500 MHz core)	16/CLKIN	 800 160 120 96	 — — — —	 ns ns ns ns
2	Delay from deassertion of external PORESET to deassertion of internal PORESET • CLKIN = 20 MHz to 166 MHz	1024/CLKIN	 6.17	 51.2	 µs
3	Delay from de-assertion of internal PORESET to SPLL lock • CLKIN = 20 MHz (RDF = 1) • CLKIN = 100 MHz (RDF = 1) (300 MHz core) • CLKIN = 133 MHz (RDF = 2) (400 MHz core) • CLKIN = 166 MHz (RDF = 2) (500 MHz core)	6400/(CLKIN/RDF) (PLL reference clock-division factor)	 320 64 96 77	 320 64 96 77	 µs µs µs µs
5	Delay from SPLL to HRESET deassertion • REFCLK = 40 MHz to 166 MHz	512/REFCLK	3.08	12.8	µs
6	Delay from SPLL lock to SRESET deassertion • REFCLK = 40 MHz to 166 MHz	515/REFCLK	3.10	12.88	µs
7	Setup time from assertion of RSTCONF, CNFGS, DSISYNC, DSI64, CHIP_ID[0–3], BM[0–2], SWTE, and MODCK[1–2] before deassertion of PORESET		3	—	ns
8	Hold time from deassertion of PORESET to deassertion of RSTCONF, CNFGS, DSISYNC, DSI64, CHIP_ID[0–3], BM[0–2], SWTE, and MODCK[1–2]		5	—	ns
Note:	Timings are not tested, but are guaranteed by design.				

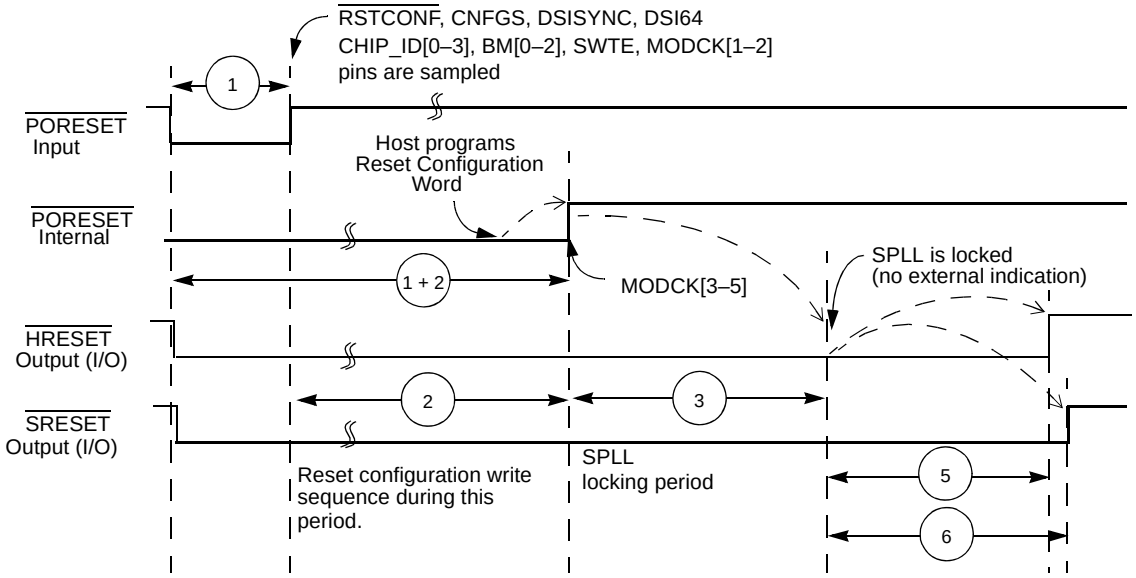


Figure 9. Timing Diagram for a Reset Configuration Write

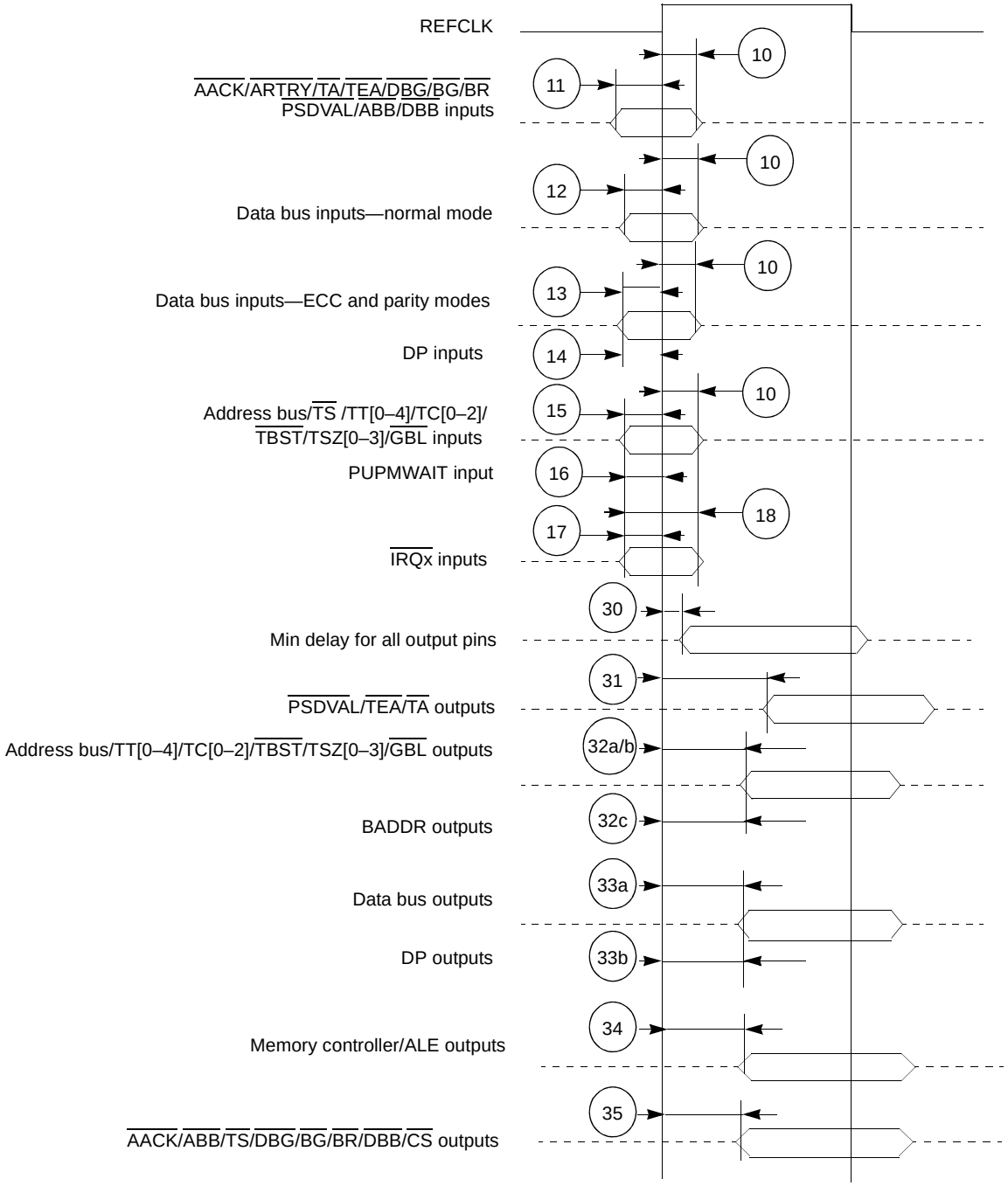


Figure 11. SIU Timing Diagram

2.5.5.3 DMA Data Transfers

Table 17 describes the DMA signal timing.

Table 17. DMA Signals

No.	Characteristic	Ref = CLKIN		Ref = CLKOUT (1.2 V only)		Units
		Min	Max	Min	Max	
37	DREQ set-up time before the 50% level of the falling edge of REFCLK	5.0	—	5.0	—	ns
38	DREQ hold time after the 50% level of the falling edge of REFCLK	0.5	—	0.5	—	ns
39	$\overline{\text{DONE}}$ set-up time before the 50% level of the rising edge of REFCLK	5.0	—	5.0	—	ns
40	$\overline{\text{DONE}}$ hold time after the 50% level of the rising edge of REFCLK	0.5	—	0.5	—	ns
41	$\overline{\text{DACK}}$/$\overline{\text{DRACK}}$/$\overline{\text{DONE}}$ delay after the 50% level of the REFCLK rising edge	0.5	7.5	0.5	8.4	ns

The DREQ signal is synchronized with REFCLK. To achieve fast response, a synchronized peripheral should assert DREQ according to the timings in **Table 17**. **Figure 13** shows synchronous peripheral interaction.

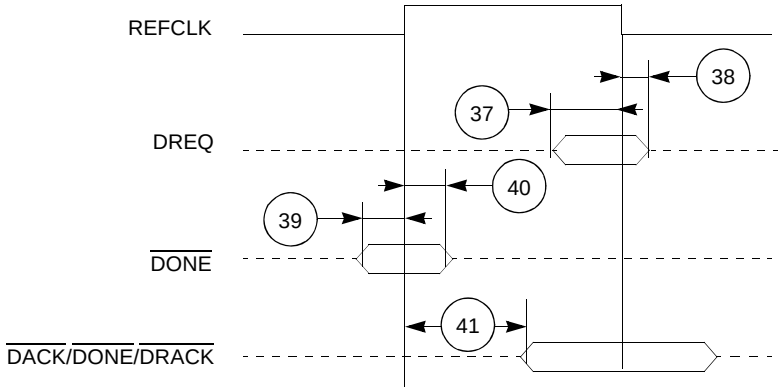
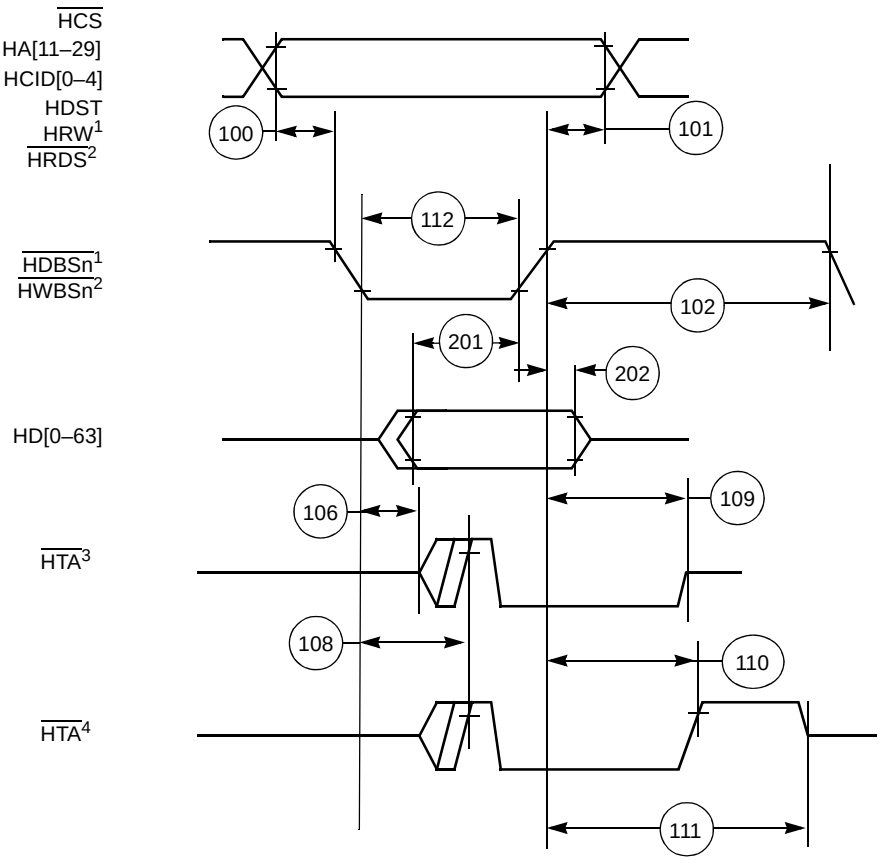


Figure 13. DMA Signals

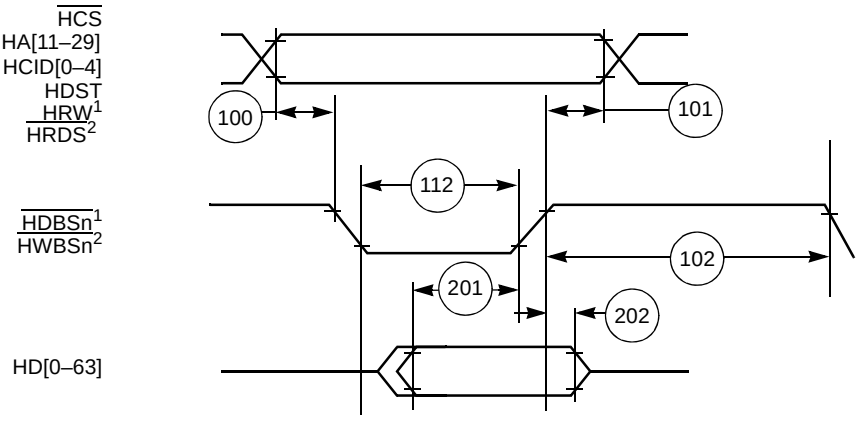
Figure 15 shows DSI asynchronous write signals timing.



Notes:
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.
3. HTA released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
4. HTA released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

Figure 15. Asynchronous Single- and Dual-Strobe Modes Write Timing Diagram

Figure 16 shows DSI asynchronous broadcast write signals timing.



Notes:
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.

Figure 16. Asynchronous Broadcast Write Timing Diagram

2.5.6.2 DSI Synchronous Mode

Table 19. DSI Inputs in Synchronous Mode

No.	Characteristic	Expression	1.1 V Core		1.2 V Core		Units
			Min	Max	Min	Max	
120	HCLKIN cycle time[1,2]	HTC	10.0	55.6	10.0	55.6	ns
121	HCLKIN high pulse width	(0.5 ± 0.1) × HTC	4.0	33.3	4.0	33.3	ns
122	HCLKIN low pulse width	(0.5 ± 0.1) × HTC	4.0	33.3	4.0	33.3	ns
123	HA[11–29] inputs set-up time	—	1.2	—	1.2	—	ns
124	HD[0–63] inputs set-up time	—	0.6	—	0.4	—	ns
125	HCID[0–4] inputs set-up time	—	1.3	—	1.3	—	ns
126	All other inputs set-up time	—	1.2	—	1.2	—	ns
127	All inputs hold time	—	1.5	—	1.5	—	ns

Notes: **1.** Values are based on a frequency range of 18–100 MHz.
2. Refer to **Table 7** for HCLKIN frequency limits.

Table 20. DSI Outputs in Synchronous Mode

No.	Characteristic	1.1 V Core		1.2 V Core		Units
		Min	Max	Min	Max	
128	HCLKIN high to HD[0–63] output active	2.0	—	2.0	—	ns
129	HCLKIN high to HD[0–63] output valid	—	7.6	—	6.3	ns
130	HD[0–63] output hold time	1.7	—	1.7	—	ns
131	HCLKIN high to HD[0–63] output high impedance	—	8.3	—	7.6	ns
132	HCLKIN high to $\overline{\text{HTA}}$ output active	2.2	—	2.0	—	ns
133	HCLKIN high to $\overline{\text{HTA}}$ output valid	—	7.4	—	5.9	ns
134	$\overline{\text{HTA}}$ output hold time	1.7	—	1.7	—	ns
135	HCLKIN high to $\overline{\text{HTA}}$ high impedance	—	7.5	—	6.3	ns

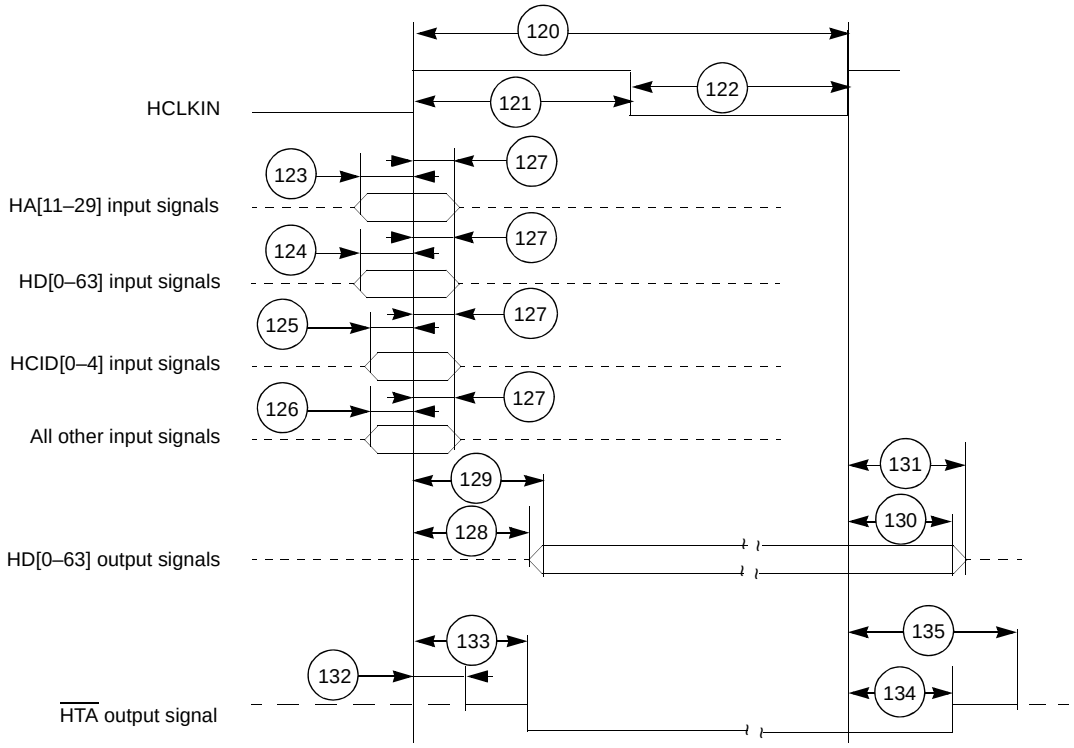


Figure 17. DSI Synchronous Mode Signals Timing Diagram

2.5.8 UART Timing

Table 22. UART Timing

No.	Characteristics	Expression	Min	Max	Unit
400	URXD and UTXD inputs high/low duration	$16 \times T_{REFCLK}$	160.0	—	ns
401	URXD and UTXD inputs rise/fall time			10	ns
402	UTXD output rise/fall time			10	ns

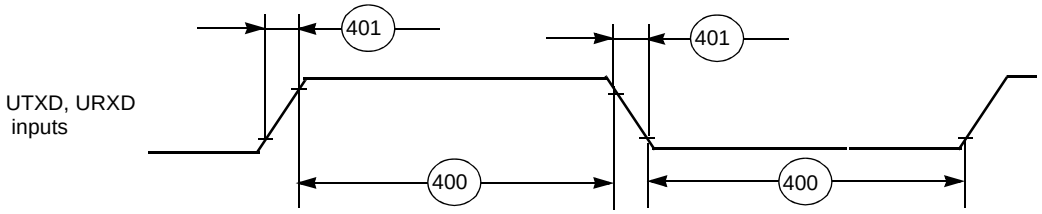


Figure 20. UART Input Timing

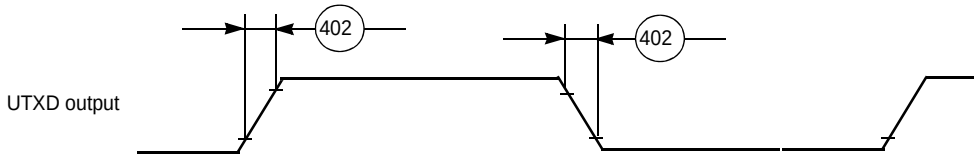


Figure 21. UART Output Timing

2.5.9 Timer Timing

Table 23. Timer Timing

No.	Characteristics	Ref = CLKIN		Unit
		Min	Max	
500	TIMERx frequency	10.0	—	ns
501	TIMERx Input high period	4.0	—	ns
502	TIMERx Output low period	4.0	—	ns
503	TIMERx Propagations delay from its clock input • 1.1 V core • 1.2 V core	 3.1 2.8	 9.5 8.1	 ns ns

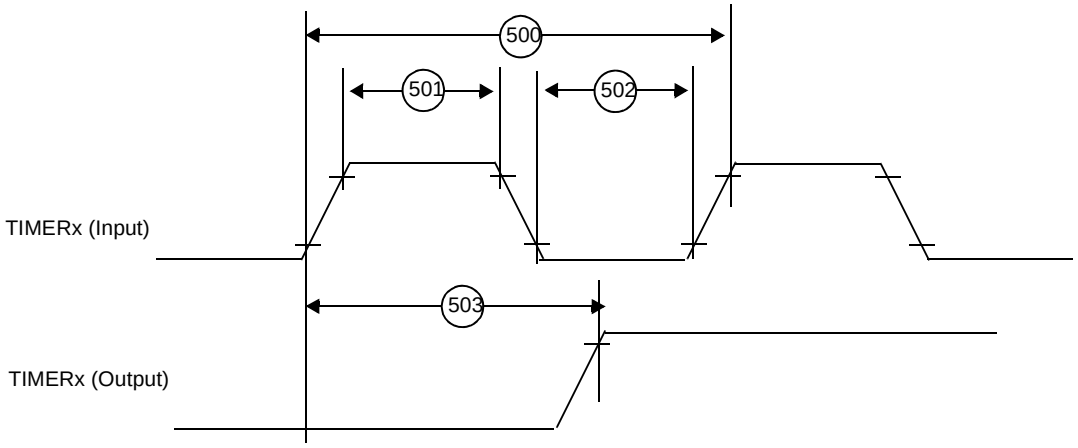


Figure 22. Timer Timing

2.5.10 Ethernet Timing

2.5.10.1 Management Interface Timing

Table 24. Ethernet Controller Management Interface Timing

No.	Characteristics	Min	Max	Unit
801	ETHMDIO to ETHMDC rising edge set-up time	10	—	ns
802	ETHMDC rising edge to ETHMDIO hold time	10	—	ns

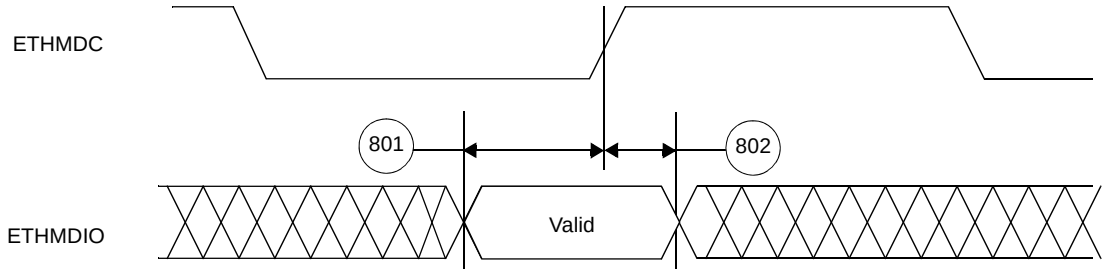


Figure 23. MDIO Timing Relationship to MDC

Table 30. JTAG Timing (continued)

No.	Characteristics	All frequencies		Unit
		Min	Max	
704	Boundary scan input data set-up time	5.0	—	ns
705	Boundary scan input data hold time	20.0	—	ns
706	TCK low to output data valid	0.0	30.0	ns
707	TCK low to output high impedance	0.0	30.0	ns
708	TMS, TDI data set-up time	5.0	—	ns
709	TMS, TDI data hold time	20.0	—	ns
710	TCK low to TDO data valid	0.0	20.0	ns
711	TCK low to TDO high impedance	0.0	20.0	ns
712	$\overline{\text{TRST}}$ assert time	100.0	—	ns
713	$\overline{\text{TRST}}$ set-up time to TCK low	30.0	—	ns
Note:	All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.			

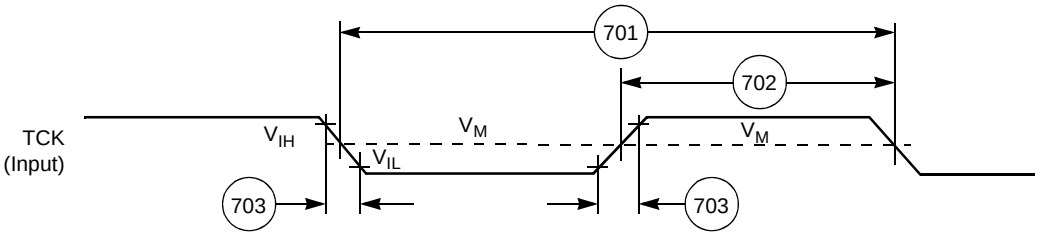


Figure 29. Test Clock Input Timing Diagram

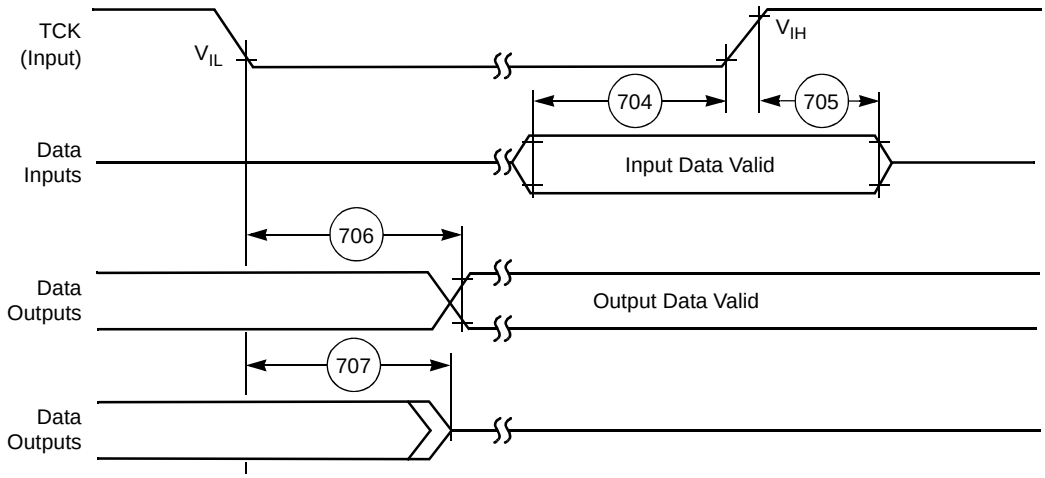


Figure 30. Boundary Scan (JTAG) Timing Diagram

3.5 Thermal Considerations

An estimation of the chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 1}$$

where

T_A = ambient temperature near the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$P_D = P_{INT} + P_{I/O}$ = power dissipation in the package (W)
$P_{INT} = I_{DD} \times V_{DD}$ = internal power dissipation (W)
$P_{I/O}$ = power dissipated from device on output pins (W)

The power dissipation values for the MSC8122 are listed in **Table 2-3**. The ambient temperature for the device is the air temperature in the immediate vicinity that would cool the device. The junction-to-ambient thermal resistances are JEDEC standard values that provide a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. The value that more closely approximates a specific application depends on the power dissipated by other components on the printed circuit board (PCB). The value obtained using a single layer board is appropriate for tightly packed PCB configurations. The value obtained using a board with internal planes is more appropriate for boards with low power dissipation (less than 0.02 W/cm^2 with natural convection) and well separated components. Based on an estimation of junction temperature using this technique, determine whether a more detailed thermal analysis is required. Standard thermal management techniques can be used to maintain the device thermal junction temperature below its maximum. If T_J appears to be too high, either lower the ambient temperature or the power dissipation of the chip. You can verify the junction temperature by measuring the case temperature using a small diameter thermocouple (40 gauge is recommended) or an infrared temperature sensor on a spot on the device case that is painted black. The MSC8122 device case surface is too shiny (low emissivity) to yield an accurate infrared temperature measurement. Use the following equation to determine T_J:

$$T_J = T_T + (\theta_{JA} \times P_D) \quad \textit{Eqn. 2}$$

where

T_T = thermocouple (or infrared) temperature on top of the package (°C)
θ_{JA} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

Note: See *MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines* (AN2601/D).

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Package Type	Core Voltage	Operating Temperature	Core Frequency (MHz)	Order Number	
					Lead-Free	Lead-Bearing
MSC8122	Flip Chip Plastic Ball Grid Array (FC-PBGA)	1.1 V	–40° to 105°C	300	MSC8122TVT4800V	MSC8122TMP4800V
				400	MSC8122TVT6400V	MSC8122TMP6400V
		1.2 V	–40° to 105°C	400	MSC8122TVT6400	MSC8122TMP6400
			0° to 90°C	500	MSC8122VT8000	MSC8122MP8000

5 Package Information

Notes:
1. All dimensions in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M–1994.
3. Features are symmetrical about the package center lines unless dimensioned otherwise.
4. Maximum solder ball diameter measured parallel to Datum A.
5. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
6. Parallelism measurement shall exclude any effect of mark on top surface of package.
7. Capacitors may not be present on all devices.
8. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
9. FC CBGA (Ceramic) package code: 5238.
   FC PBGA (Plastic) package code: 5263.
10. Pin 1 indicator can be in the form of number 1 marking or an “L” shape marking.

Figure 35. MSC8122 Mechanical Information, 431-pin FC-PBGA Package

6 Product Documentation

- *MSC8122 Technical Data Sheet* (MSC8122). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8122 device.
- *MSC8122 Reference Manual* (MSC8122RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC8122 device.
- *SC140 DSP Core Reference Manual*. Covers the SC140 core architecture, control registers, clock registers, program control, and instruction set.

7 Revision History

Table 31 provides a revision history for this data sheet.

Table 31. Document Revision History

Revision	Date	Description
0	May 2004	• Initial release.
1	Jun. 2004	• Updated timing number 32b. • Updated DSI timing specifications.
2	Sep 2004	• New orderable parts added with other core voltage and temperature options. • Updated thermal characteristics. • In Table 2-14, removed references to 30 pF. • Design guidelines and layout recommendations updated.
3	Nov. 2004	• Added 500 MHz core and 166 MHz bus speed options. • Definitions of GPIO[27–28] updated. • Bus, TDM, and GPIO timing updated. I^2C timing changed to GPIO timing. • GPIO[27–28] connections updated. MWBEn replaced with correct name HWBEn. • Design guidelines update.
4	Jan. 2005	• Package type changed to FC-PBGA for all frequencies. • Low-voltage 300 MHz power changed to 1.1 V. • $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ definitions updated. • Undershoot and overshoot values added for V_{DDH}. • RMII timing updated. • Design guidelines updated and reorganized.
5	Apr. 2005	• Added 400 MHz, 1.1 V core part. • Temperature range descriptions changed to standard and extended. • CLKOUT timing specifications added. • Device start-up guidelines added to design considerations and updated power supply guidelines. • Ordering information updated.
6	May 2005	• Multiple AC timing specifications updated.
7	May 2005	• Multiple AC timing specifications updated.
8	Jul. 2005	• Multiple AC timing specifications updated.
9	Jul. 2005	• AC specification table layout modified.
10	Sep. 2005	• ETHTX_EN type and $\overline{\text{TRST}}$ description updated. • Package drawing updated. • Clock specifications updated. • Start-up sequence updated.
11	Oct 2005	• V_{DDH} + 10% changed to V_{DDH} + 8% in **Figure 2-1**. • V_{DDH} +20% changed to V_{DDH} + 17% in **Figure 2-1**.
12	Apr 2006	• Reset timing updated to reflect actual values in **Table 2-11**.
13	Oct. 2006	• Added new timings 17 and 18 for IRQ set time and pulse width in **Table 2-13**
14	Dec. 2007	• Converted to new data sheet format. • Added PLL supply current to **Table 5** in **Section 2.4**. • Modified **Figure 5** in **Section 2.4** to make it clear that the time limits for undershoot referred to values below –0.3 V and not GND. • Added cross-references between **Sections 2.5.2** and **Section 3.1** and **3.2**. • Added power-sequence guidelines to **Sections 2.5.2**. • Added CLKIN jitter characteristic specifications to Table 9. • Added additional guidelines to prevent reverse current to **Section 3.1**. • Added connectivity guidelines for DSI in sliding windows mode to **Section 3.3**.
15	May 2008	• Changed V_{IL} maximum and reference value to 0.8 V in **Table 5**.
16	Dec. 2008	• Clarified the wording of note 2 in **Table 15** on p. 24.