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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC140 Core
Interface	DSI, Ethernet, RS-232
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	1.436MB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	431-BFBGA, FCBGA
Supplier Device Package	431-FCPBGA (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmsc8122tvt6400v

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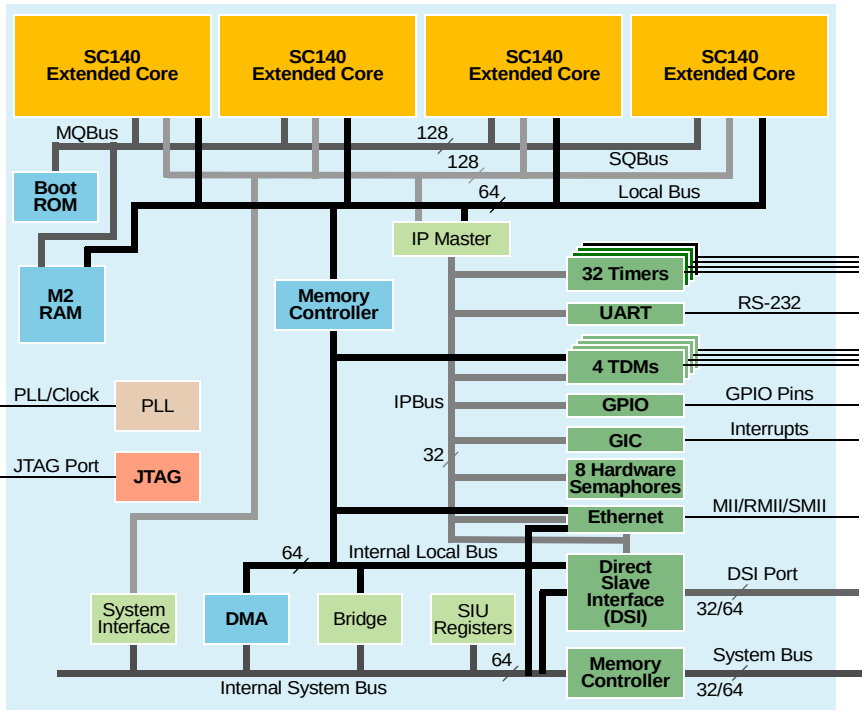
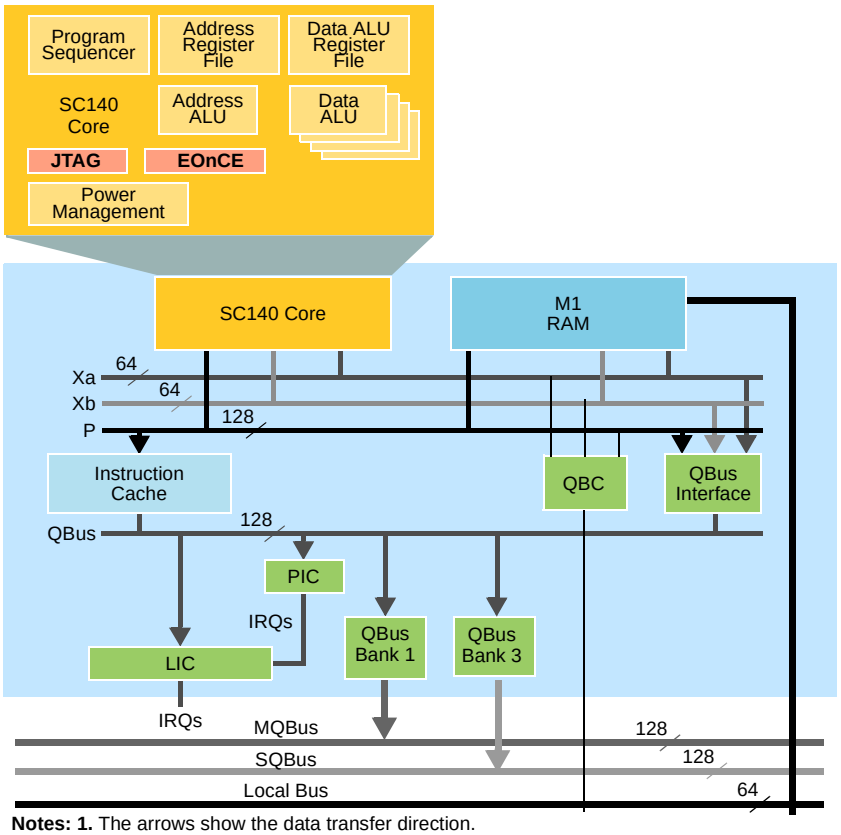


Figure 1. MSC8122 Block Diagram



Notes: **1.** The arrows show the data transfer direction.
2. The QBus interface includes a bus switch, write buffer, fetch unit, and a control unit that defines four QBus banks. In addition, the QBC handles internal memory contentions.

Figure 2. StarCore SC140 DSP Extended Core Block Diagram

1 Pin Assignments

This section includes diagrams of the MSC8122 package ball grid array layouts and pinout allocation tables.

1.1 FC-PBGA Ball Layout Diagrams

Top and bottom views of the FC-PBGA package are shown in **Figure 3** and **Figure 4** with their ball location index numbers.

Top View

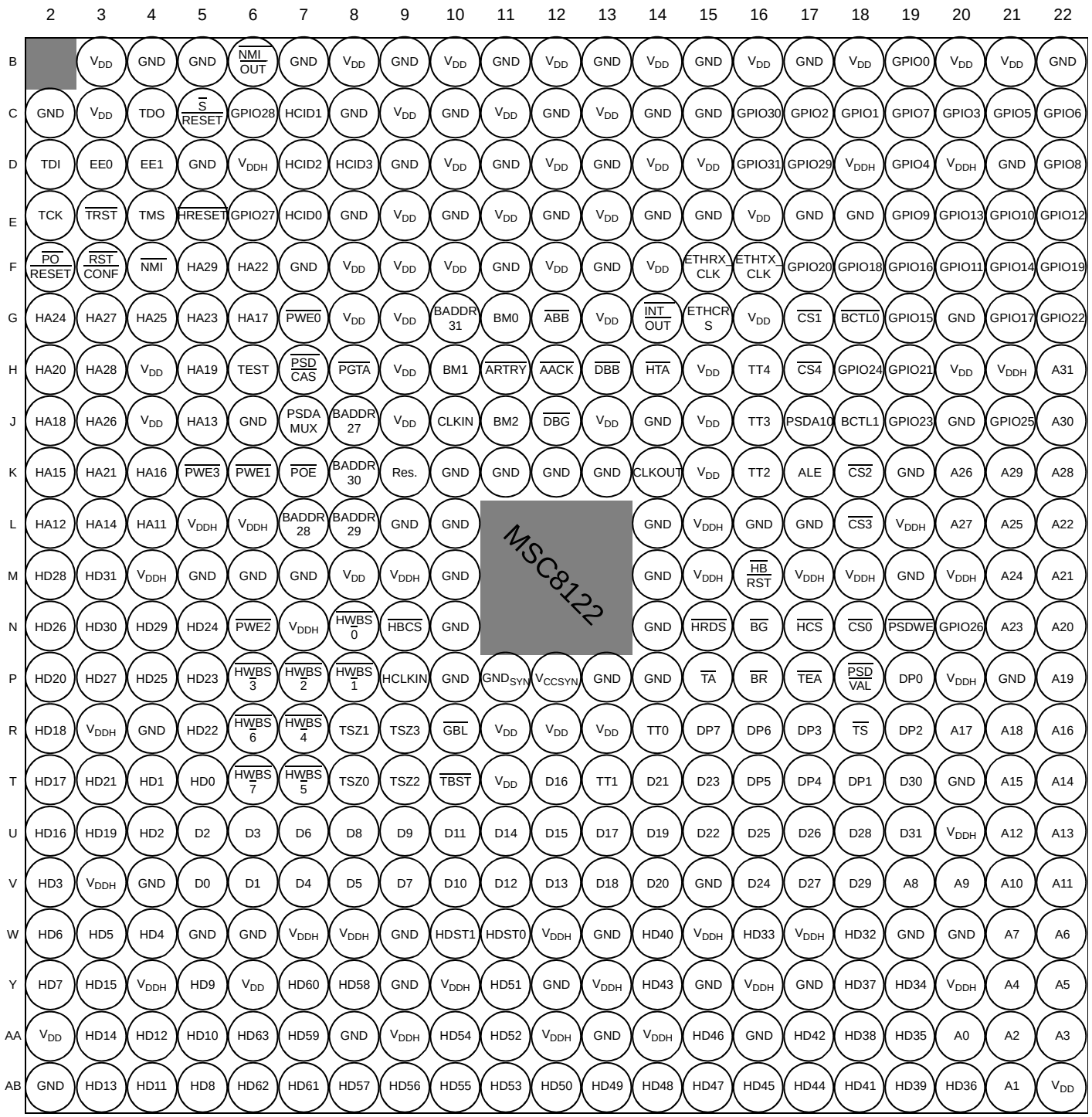


Figure 3. MSC8122 Package, Top View

Table 1. MSC8122 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
H21	V_{DDH}	K15	V_{DD}
H22	A31	K16	TT2/$\overline{CS5}$
J2	HA18	K17	ALE
J3	HA26	K18	$\overline{CS2}$
J4	V_{DD}	K19	GND
J5	HA13	K20	A26
J6	GND	K21	A29
J7	PSDAMUX/PGPL5	K22	A28
J8	BADDR27	L2	HA12
J9	V_{DD}	L3	HA14
J10	CLKIN	L4	HA11
J11	BM2/TC2/BNKSEL2	L5	V_{DDH}
J12	$\overline{DBG}$	L6	V_{DDH}
J13	V_{DD}	L7	BADDR28
J14	GND	L8	$\overline{IRQ5}$/BADDR29
J15	V_{DD}	L9	GND
J16	TT3/$\overline{CS6}$	L10	GND
J17	PSDA10/PGPL0	L14	GND
J18	$\overline{BCTL1}$/$\overline{CS5}$	L15	V_{DDH}
J19	GPIO23/TDM0TDAT/$\overline{IRQ13}$	L16	GND
J20	GND	L17	GND
J21	GPIO25/TDM0RCLK/$\overline{IRQ15}$	L18	$\overline{CS3}$
J22	A30	L19	V_{DDH}
K2	HA15	L20	A27
K3	HA21	L21	A25
K4	HA16	L22	A22
K5	$\overline{PWE3}$/$\overline{PSDDQM3}$/$\overline{PBS3}$	M2	HD28
K6	$\overline{PWE1}$/$\overline{PSDDQM1}$/$\overline{PBS1}$	M3	HD31
K7	$\overline{POE}$/$\overline{PSDRAS}$/PGPL2	M4	V_{DDH}
K8	$\overline{IRQ2}$/BADDR30	M5	GND
K9	Reserved	M6	GND
K10	GND	M7	GND
K11	GND	M8	V_{DD}
K12	GND	M9	V_{DDH}
K13	GND	M10	GND
K14	CLKOUT	M14	GND

Table 1. MSC8122 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
M15	V_{DDH}	P12	V_{CCSYN}
M16	$\overline{\text{HBRST}}$	P13	GND
M17	V_{DDH}	P14	GND
M18	V_{DDH}	P15	$\overline{\text{TA}}$
M19	GND	P16	$\overline{\text{BR}}$
M20	V_{DDH}	P17	$\overline{\text{TEA}}$
M21	A24	P18	$\overline{\text{PSDVAL}}$
M22	A21	P19	DP0/DREQ1/$\overline{\text{EXT\_BR2}}$
N2	HD26	P20	V_{DDH}
N3	HD30	P21	GND
N4	HD29	P22	A19
N5	HD24	R2	HD18
N6	$\overline{\text{PWE2}}$/$\overline{\text{PSDDQM2}}$/$\overline{\text{PBS2}}$	R3	V_{DDH}
N7	V_{DDH}	R4	GND
N8	$\overline{\text{HWBS0}}$/$\overline{\text{HDBS0}}$/$\overline{\text{HWBE0}}$/$\overline{\text{HDBE0}}$	R5	HD22
N9	$\overline{\text{HBCS}}$	R6	$\overline{\text{HWBS6}}$/$\overline{\text{HDBS6}}$/$\overline{\text{HWBE6}}$/$\overline{\text{HDBE6}}$/$\overline{\text{PWE6}}$/$\overline{\text{PSDDQM6}}$/$\overline{\text{PBS6}}$
N10	GND	R7	$\overline{\text{HWBS4}}$/$\overline{\text{HDBS4}}$/$\overline{\text{HWBE4}}$/$\overline{\text{HDBE4}}$/$\overline{\text{PWE4}}$/$\overline{\text{PSDDQM4}}$/$\overline{\text{PBS4}}$
N14	GND	R8	TSZ1
N15	$\overline{\text{HRDS}}$/HRW/$\overline{\text{HRDE}}$	R9	TSZ3
N16	$\overline{\text{BG}}$	R10	$\overline{\text{IRQ1}}$/$\overline{\text{GBL}}$
N17	$\overline{\text{HCS}}$	R11	V_{DD}
N18	$\overline{\text{CS0}}$	R12	V_{DD}
N19	$\overline{\text{PSDWE}}$/PGPL1	R13	V_{DD}
N20	GPIO26/TDM0RDAT	R14	TT0/HA7
N21	A23	R15	$\overline{\text{IRQ7}}$/DP7/DREQ4
N22	A20	R16	$\overline{\text{IRQ6}}$/DP6/DREQ3
P2	HD20	R17	$\overline{\text{IRQ3}}$/DP3/DREQ2/$\overline{\text{EXT\_BR3}}$
P3	HD27	R18	$\overline{\text{TS}}$
P4	HD25	R19	$\overline{\text{IRQ2}}$/DP2/$\overline{\text{DACK2}}$/$\overline{\text{EXT\_DBG2}}$
P5	HD23	R20	A17
P6	$\overline{\text{HWBS3}}$/$\overline{\text{HDBS3}}$/$\overline{\text{HWBE3}}$/$\overline{\text{HDBE3}}$	R21	A18
P7	$\overline{\text{HWBS2}}$/$\overline{\text{HDBS2}}$/$\overline{\text{HWBE2}}$/$\overline{\text{HDBE2}}$	R22	A16
P8	$\overline{\text{HWBS1}}$/$\overline{\text{HDBS1}}$/$\overline{\text{HWBE1}}$/$\overline{\text{HDBE1}}$	T2	HD17
P9	HCLKIN	T3	HD21
P10	GND	T4	HD1/DSISYNC
P11	GND_{SYN}	T5	HD0/SWTE

Table 1. MSC8122 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
T6	HWBS7/HDBS7/HWBE7/HDBE7/PWE7/PSDDQM7/PBS7	U21	A12
T7	HWBS5/HDBS5/HWBE5/HDBE5/PWE5/PSDDQM5/PBS5	U22	A13
T8	TSZ0	V2	HD3/MODCK1
T9	TSZ2	V3	V_{DDH}
T10	TBST	V4	GND
T11	V_{DD}	V5	D0
T12	D16	V6	D1
T13	TT1	V7	D4
T14	D21	V8	D5
T15	D23	V9	D7
T16	IRQ5/DP5/DACK4/EXT_BG3	V10	D10
T17	IRQ4/DP4/DACK3/EXT_DBG3	V11	D12
T18	IRQ1/DP1/DACK1/EXT_BG2	V12	D13
T19	D30	V13	D18
T20	GND	V14	D20
T21	A15	V15	GND
T22	A14	V16	D24
U2	HD16	V17	D27
U3	HD19	V18	D29
U4	HD2/DSI64	V19	A8
U5	D2	V20	A9
U6	D3	V21	A10
U7	D6	V22	A11
U8	D8	W2	HD6
U9	D9	W3	HD5/CNFGS
U10	D11	W4	HD4/MODCK2
U11	D14	W5	GND
U12	D15	W6	GND
U13	D17	W7	V_{DDH}
U14	D19	W8	V_{DDH}
U15	D22	W9	GND
U16	D25	W10	HDST1/HA10
U17	D26	W11	HDST0/HA9
U18	D28	W12	V_{DDH}
U19	D31	W13	GND
U20	V_{DDH}	W14	HD40/D40/ETHRXD0

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core and PLL supply voltage: • Standard — 400 MHz — 500 MHz • Reduced (300 and 400 MHz)	V_{DD} V_{CCSYN}	 1.14 to 1.26 1.16 to 1.24 1.07 to 1.13	 V V V
I/O supply voltage	V_{DDH}	3.135 to 3.465	V
Input voltage	V_{IN}	–0.2 to V_{DDH}+0.2	V
Operating temperature range: • Standard • Extended	 T_J T_J	 0 to 90 –40 to 105	 °C °C

2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC8122 for the FC-PBGA packages.

Table 4. Thermal Characteristics for the MSC8122

Characteristic	Symbol	FC-PBGA 20 × 20 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	26	21	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	19	15	°C/W
Junction-to-board (bottom)[4]	$R_{\theta JB}$	9		°C/W
Junction-to-case[5]	$R_{\theta JC}$	0.9		°C/W
Junction-to-package-top[6]	Ψ_{JT}	1		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Section 3.5, *Thermal Considerations* provides a detailed explanation of these characteristics.

Table 15. AC Timing for SIU Outputs

No.	Characteristic	Value for Bus Speed in MHz[3]				Units
		Ref = CLKIN			Ref = CLKOUT	
		1.1 V	1.2 V	1.2 V	1.2 V	
		100/133	133	166	100/133	
30[2]	Minimum delay from the 50% level of the REFCLK for all signals	0.9	0.8	0.8	1.0	ns
31	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$ max delay from the 50% level of the REFCLK rising edge	6.0	4.9	4.9	5.8	ns
32a	Address bus max delay from the 50% level of the REFCLK rising edge • Multi-master mode (SIUBCR[EBM] = 1) • Single-master mode (SIUBCR[EBM] = 0)	 6.4 5.3	 5.5 4.2	 5.5 3.9	 6.4 5.1	 ns ns
32b	Address attributes: TT[0–1]/$\overline{\text{TBST}}$/TSZ/$\overline{\text{GBL}}$ max delay from the 50% level of the REFCLK rising edge	6.4	5.1	5.1	6.0	ns
32c	Address attributes: TT[2–4]/TC max delay from the 50% level of the REFCLK rising edge	6.9	5.7	5.7	6.6	ns
32d	BADDR max delay from the 50% level of the REFCLK rising edge	5.2	4.2	4.2	5.1	ns
33a	Data bus max delay from the 50% level of the REFCLK rising edge • Data-pipeline mode • Non-pipeline mode	 4.8 7.1	 3.9 6.1	 3.7 6.1	 4.8 7.0	 ns ns
33b	DP max delay from the 50% level of the REFCLK rising edge • Data-pipeline mode • Non-pipeline mode	 6.0 7.5	 5.3 6.5	 5.3 6.5	 6.2 7.4	 ns ns
34	Memory controller signals/ALE/$\overline{\text{CS}}$[0–4] max delay from the 50% level of the REFCLK rising edge	5.1	4.2	3.9	5.1	ns
35a	$\overline{\text{DBG}}/\overline{\text{BG}}/\overline{\text{BR}}/\overline{\text{DBB}}$ max delay from the 50% level of the REFCLK rising edge	6.0	4.7	4.7	5.6	ns
35b	$\overline{\text{AACK}}/\overline{\text{ABB}}/\overline{\text{TS}}/\overline{\text{CS}}$[5–7] max delay from the 50% level of the REFCLK rising edge	5.5	4.5	4.5	5.4	ns

Notes:
1. Values are measured from the 50% level of the REFCLK rising edge to the 50% signal level and assume a 20 pF load except where otherwise specified.
2. Except for specification 30, which is specified for a 10 pF load, all timings in this table are specified for a 20 pF load. Decreasing the load results in a timing decrease at the rate of 0.3 ns per 5 pF decrease in load. Increasing the load results in a timing increase at the rate of 0.15 ns per 5 pF increase in load.
3. The maximum bus frequency depends on the mode:
   • In 60x-compatible mode connected to another MSC8122 device, the frequency is determined by adding the input and output longest timing values, which results in the total delay for 20 pF output capacitance. You must also account for other influences that can affect timing, such as on-board clock skews, on-board noise delays, and so on.
   • In single-master mode, the frequency depends on the timing of the devices connected to the MSC8122.
   • To achieve maximum performance on the bus in single-master mode, disable the $\overline{\text{DBB}}$ signal by writing a 1 to the SIUMCR[BDD] bit. See the SIU chapter in the *MSC8122 Reference Manual* for details.

2.5.5.2 CLKIN to CLKOUT Skew

Table 17 describes the CLKOUT-to-CLKIN skew timing.

Table 16. CLKOUT Skew

No.	Characteristic	Min[1]	Max[1]	Units
20	Rise-to-rise skew			
	• V_{DD} = 1.1 V	0.0	0.95	ns
	• V_{DD} = 1.2 V	0.0	0.85	ns
21	Fall-to-fall skew			
	• V_{DD} = 1.1 V	–1.5	1.0	ns
	• V_{DD} = 1.2 V	–0.8	1.0	ns
22	CLKOUT phase (1.2 V, 133 MHz)			
	• Phase high	2.8	—	ns
	• Phase low	2.8	—	ns
23	CLKOUT phase (1.1 V, 133 MHz)			
	• Phase high	2.2	—	ns
	• Phase low	2.2	—	ns
24	CLKOUT phase (1.1 V, 100 MHz)			
	• Phase high	3.3	—	ns
	• Phase low	3.3	—	ns

Notes:
1. A positive number indicates that CLKOUT precedes CLKIN, A negative number indicates that CLKOUT follows CLKIN.
2. Skews are measured in clock mode 29, with a CLKIN:CLKOUT ratio of 1:1. The same skew is valid for all clock modes.
3. CLKOUT skews are measured using a load of 10 pF.
4. CLKOUT skews and phase are not measured for 500/166 Mhz parts because these parts only use CLKIN mode.

For designs that use the CLKOUT synchronization mode, use the skew values listed in **Table 16** to adjust the rise-to-fall timing values specified for CLKIN synchronization. **Figure 12** shows the relationship between the CLKOUT and CLKIN timings.

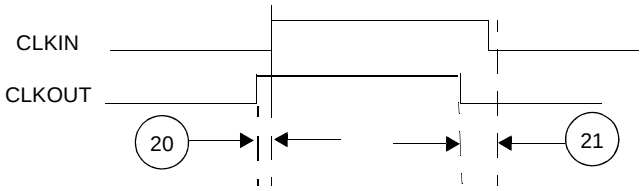


Figure 12. CLKOUT and CLKIN Signals.

2.5.5.3 DMA Data Transfers

Table 17 describes the DMA signal timing.

Table 17. DMA Signals

No.	Characteristic	Ref = CLKIN		Ref = CLKOUT (1.2 V only)		Units
		Min	Max	Min	Max	
37	DREQ set-up time before the 50% level of the falling edge of REFCLK	5.0	—	5.0	—	ns
38	DREQ hold time after the 50% level of the falling edge of REFCLK	0.5	—	0.5	—	ns
39	$\overline{\text{DONE}}$ set-up time before the 50% level of the rising edge of REFCLK	5.0	—	5.0	—	ns
40	$\overline{\text{DONE}}$ hold time after the 50% level of the rising edge of REFCLK	0.5	—	0.5	—	ns
41	$\overline{\text{DACK}}$/$\overline{\text{DRACK}}$/$\overline{\text{DONE}}$ delay after the 50% level of the REFCLK rising edge	0.5	7.5	0.5	8.4	ns

The DREQ signal is synchronized with REFCLK. To achieve fast response, a synchronized peripheral should assert DREQ according to the timings in **Table 17**. **Figure 13** shows synchronous peripheral interaction.

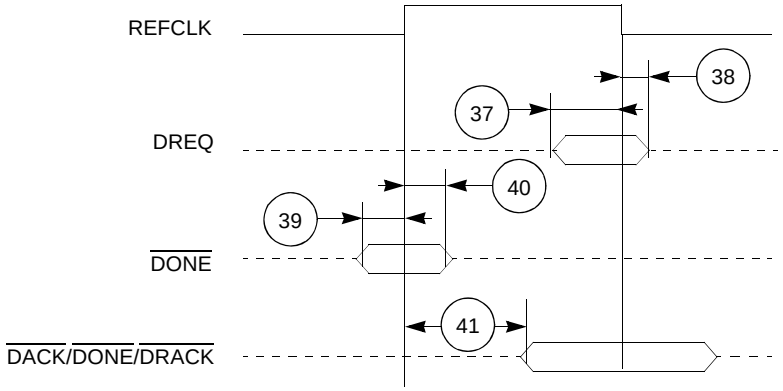


Figure 13. DMA Signals

2.5.8 UART Timing

Table 22. UART Timing

No.	Characteristics	Expression	Min	Max	Unit
400	URXD and UTXD inputs high/low duration	$16 \times T_{REFCLK}$	160.0	—	ns
401	URXD and UTXD inputs rise/fall time			10	ns
402	UTXD output rise/fall time			10	ns

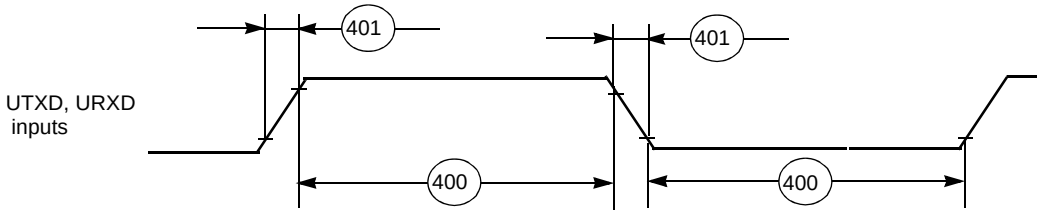


Figure 20. UART Input Timing

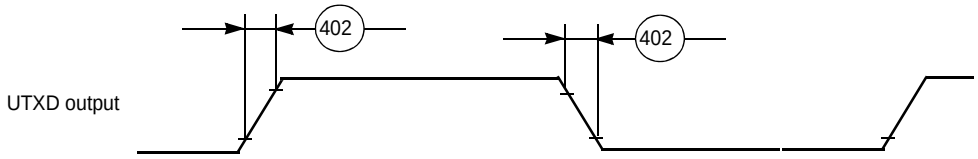


Figure 21. UART Output Timing

2.5.10.4 SMII Mode

Table 27. SMII Mode Signal Timing

No.	Characteristics	Min	Max	Unit
808	ETHSYNC_IN, ETHRXD to ETHCLOCK rising edge set-up time	1.0	—	ns
809	ETHCLOCK rising edge to ETHSYNC_IN, ETHRXD hold time	1.0	—	ns
810	ETHCLOCK rising edge to ETHSYNC, ETHTXD output delay • 1.1 V core. • 1.2 V core.	 1.5[1] 1.5[1]	 6.0[2] 5.0[2]	 ns ns
Notes:	**1.** Measured using a 5 pF load. **2.** Measured using a 15 pF load.			

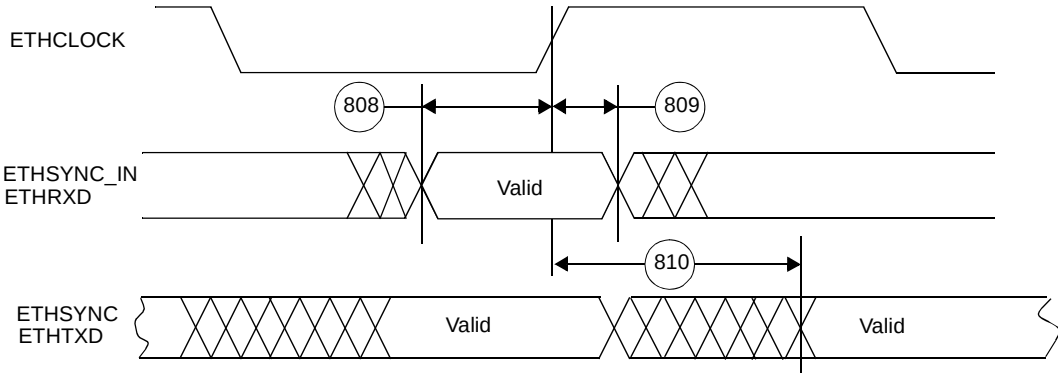


Figure 26. SMII Mode Signal Timing

2.5.11 GPIO Timing

Table 28. GPIO Timing

No.	Characteristics	Ref = CLKIN		Ref = CLKOUT (1.2 V only)		Unit
		Min	Max	Min	Max	
601	REFCLK edge to GPIO out valid (GPIO out delay time)	—	6.1	—	6.9	ns
602	REFCLK edge to GPIO out not valid (GPIO out hold time)	1.1	—	1.3	—	ns
603	REFCLK edge to high impedance on GPIO out	—	5.4	—	6.2	ns
604	GPIO in valid to REFCLK edge (GPIO in set-up time)	3.5	—	3.7	—	ns
605	REFCLK edge to GPIO in not valid (GPIO in hold time)	0.5	—	0.5	—	ns

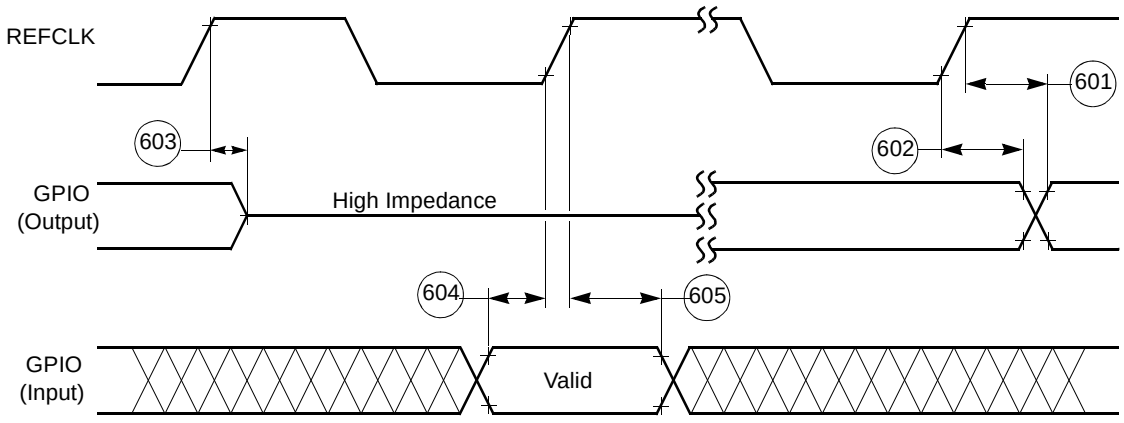


Figure 27. GPIO Timing

2.5.12 EE Signals

Table 29. EE Pin Timing

Number	Characteristics	Type	Min
65	EE0 (input)	Asynchronous	4 core clock periods
66	EE1 (output)	Synchronous to Core clock	1 core clock period

Notes: 1. The core clock is the SC140 core clock. The ratio between the core clock and CLKOUT is configured during power-on-reset.
2. Refer to **Table 1-4** on page 1-6 for details on EE pin functionality.

Figure 28 shows the signal behavior of the EE pins.

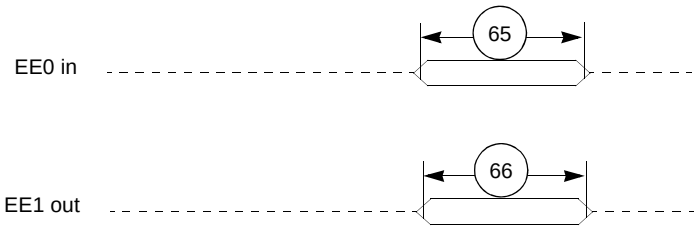


Figure 28. EE Pin Timing

2.5.13 JTAG Signals

Table 30. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
700	TCK frequency of operation (1/($T_C \times 4$); maximum 25 MHz)	0.0	25	MHz
701	TCK cycle time	40.0	—	ns
702	TCK clock pulse width measured at V_M = 1.6 V • High • Low	 20.0 16.0	 — —	 ns ns
703	TCK rise and fall times	0.0	3.0	ns

Table 30. JTAG Timing (continued)

No.	Characteristics	All frequencies		Unit
		Min	Max	
704	Boundary scan input data set-up time	5.0	—	ns
705	Boundary scan input data hold time	20.0	—	ns
706	TCK low to output data valid	0.0	30.0	ns
707	TCK low to output high impedance	0.0	30.0	ns
708	TMS, TDI data set-up time	5.0	—	ns
709	TMS, TDI data hold time	20.0	—	ns
710	TCK low to TDO data valid	0.0	20.0	ns
711	TCK low to TDO high impedance	0.0	20.0	ns
712	$\overline{\text{TRST}}$ assert time	100.0	—	ns
713	$\overline{\text{TRST}}$ set-up time to TCK low	30.0	—	ns
Note:	All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.			

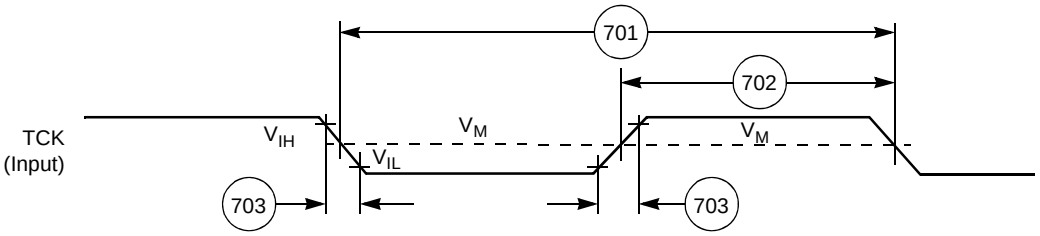


Figure 29. Test Clock Input Timing Diagram

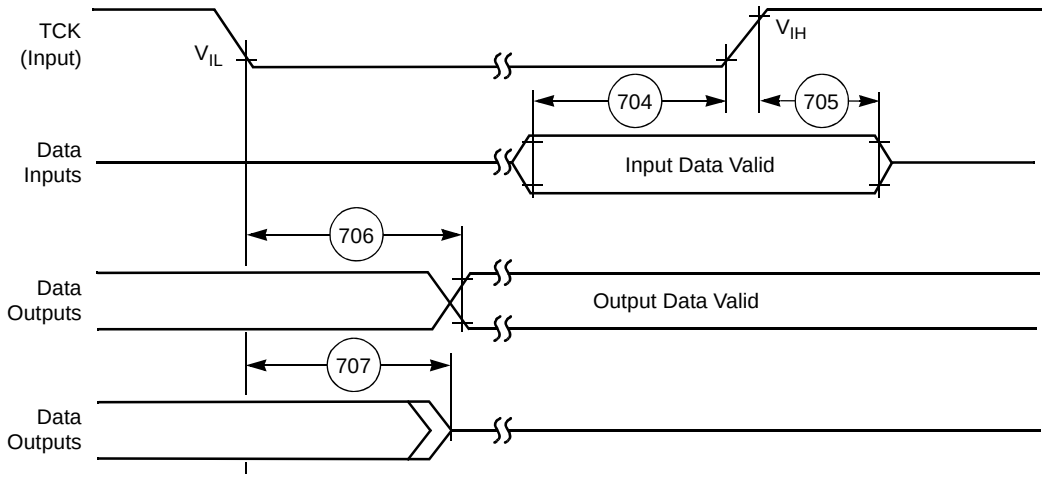


Figure 30. Boundary Scan (JTAG) Timing Diagram

- Never allow V_{DD} to exceed V_{DDH} + 0.8V.
- Design the V_{DDH} supply to prevent reverse current flow by adding a minimum 10 Ω resistor to GND to limit the current. Such a design yields an initial V_{DDH} level of V_{DD} – 0.8 V before it is enabled.

After power-up, V_{DDH} must not exceed V_{DD}/V_{CCSYN} by more than 2.6 V.

3.2 Power Supply Design Considerations

When used as a drop-in replacement in MSC8102 applications or when implementing a new design, use the guidelines described in *Migrating Designs from the MSC8102 to the MSC8122* (AN2716) and the *MSC8122 Design Checklist* (AN3374 for optimal system performance. *MSC8122 and MSC8126 Power Circuit Design Recommendations and Examples* (AN2937) provides detailed design information. See **Section 2.5.2** for start-up timing specifications.

Figure 33 shows the recommended power decoupling circuit for the core power supply. The voltage regulator and the decoupling capacitors should supply the required device current without any drop in voltage on the device pins. The voltage on the package pins should not drop below the minimum specified voltage level even for a very short spikes. This can be achieved by using the following guidelines:

- For the core supply, use a voltage regulator rated at 1.2 V with nominal rating of at least 3 A. This rating does not reflect actual average current draw, but is recommended because it resists changes imposed by transient spikes and has better voltage recovery time than supplies with lower current ratings.
- Decouple the supply using low-ESR capacitors mounted as close as possible to the socket. **Figure 33** shows three capacitors in parallel to reduce the resistance. Three capacitors is a recommended minimum number. If possible, mount at least one of the capacitors directly below the MSC8122 device.

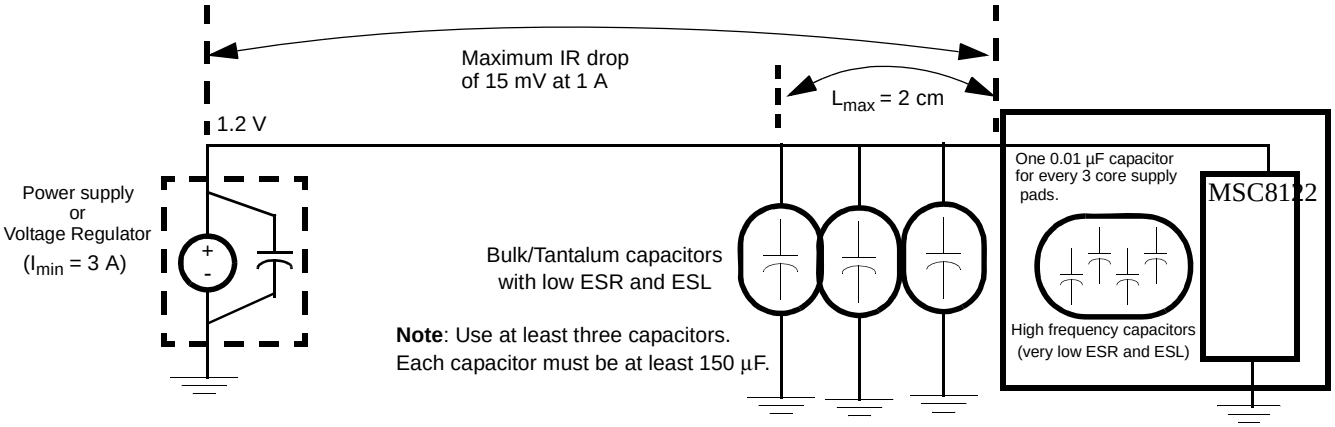


Figure 33. Core Power Supply Decoupling

Each V_{CC} and V_{DD} pin on the MSC8122 device should have a low-impedance path to the board power supply. Similarly, each GND pin should have a low-impedance path to the ground plane. The power supply pins drive distinct groups of logic on the chip. The V_{CC} power supply should have at least four 0.1 µF by-pass capacitors to ground located as closely as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC}, V_{DD}, and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MSC8122 have fast rise and fall times. PCB trace interconnection length should be minimized to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PCB trace lengths of six inches are recommended. For the DSI control signals in synchronous mode, ensure that the layout supports the DSI AC timing requirements and minimizes any signal crosstalk. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PCB traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC}, V_{DD}, and GND circuits. Pull up all unused inputs or signals that will be inputs during reset.

Special care should be taken to minimize the noise levels on the PLL supply pins. There is one pair of PLL supply pins: V_{CCSYN}-GND_{SYN}. To ensure internal clock stability, filter the power to the V_{CCSYN} input with a circuit similar to the one in

Note: The MSC8122 does not support DLL-enabled mode. For the following two clock schemes, ensure that the DLL is disabled (that is, the DLLDIS bit in the Hard Reset Configuration Word is set).

- If no system synchronization is required (for example, the design does not use SDRAM), you can use any of the available clock modes.
- In the CLKIN synchronization mode, use the following connections:
  - Connect the oscillator output through a buffer to CLKIN.
  - Connect the CLKIN buffer output to the slave device (for example, SDRAM) making sure that the delay path between the clock buffer to the MSC8122 and the SDRAM is equal (that is, has a skew less than 100 ps).
  - Valid clock modes in this scheme are: 0, 7, 15, 19, 21, 23, 28, 29, 30, and 31.
- In CLKOUT synchronization mode (for 1.2 V devices), CLKOUT is the main clock to SDRAM. Use the following connections:
  - Connect the oscillator output through a buffer to CLKIN.
  - Connect CLKOUT through a zero-delay buffer to the slave device (for example, SDRAM) using the following guidelines:
    - The maximum delay between the slave and CLKOUT must not exceed 0.7 ns.
    - The maximum load on CLKOUT must not exceed 10 pF.
    - Use a zero-delay buffer with a jitter less than 0.3 ns.
  - All clock modes are valid in this clock scheme.

Note: See the Clock chapter in the *MSC8122 Reference Manual* for details.

- If the 60x-compatible system bus is not used and SIUMCR[PBSE] is set, $\overline{\text{PPBS}}$ can be disconnected. Otherwise, it should be pulled up.
- The following signals: SWTE, DSISYNC, DSI64, MODCK[1–2], CNFGS, CHIPID[0–3], RSTCONF and BM[0–2] are used to configure the MSC8122 and are sampled on the deassertion of the $\overline{\text{PORESET}}$ signal. Therefore, they should be tied to GND or V_{DDH} or through a pull-down or a pull-up resistor until the deassertion of the $\overline{\text{PORESET}}$ signal.
- When they are used, $\overline{\text{INT\_OUT}}$ (if SIUMCR[INTODC] is cleared), $\overline{\text{NMI\_OUT}}$, and $\overline{\text{IRQxx}}$ (if not full drive) signals must be pulled up.
- When the Ethernet controller is enabled and the SMII mode is selected, GPIO10 and GPIO14 must not be connected externally to any signal line.

Note: For details on configuration, see the *MSC8122 User's Guide* and *MSC8122 Reference Manual*. For additional information, refer to the *MSC8122 Design Checklist* (AN2787).

3.4 External SDRAM Selection

The external bus speed implemented in a system determines the speed of the SDRAM used on that bus. However, because of differences in timing characteristics among various SDRAM manufacturers, you may have use a faster speed rated SDRAM to assure efficient data transfer across the bus. For example, for 166 MHz operation, you may have to use 183 or 200 MHz SDRAM. Always perform a detailed timing analysis using the MSC8122 bus timing values and the manufacturer specifications for the SDRAM to ensure correct operation within your system design. The output delay listed in SDRAM specifications is usually given for a load of 30 pF. Scale the number to your specific board load using the typical scaling number provided by the SDRAM manufacturer.

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