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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC140 Core
Interface	DSI, Ethernet, RS-232
Clock Rate	500MHz
Non-Volatile Memory	External
On-Chip RAM	1.436MB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	431-BFBGA, FCBGA
Supplier Device Package	431-FCPBGA (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmsc8122vt8000

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Top View

	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
B		V_{DD}	GND	GND	NMI OUT	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GPIO0	V_{DD}	V_{DD}	GND
C	GND	V_{DD}	TDO	S RESET	GPIO28	HCID1	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	GND	GPIO30	GPIO2	GPIO1	GPIO7	GPIO3	GPIO5	GPIO6
D	TDI	EE0	EE1	GND	V_{DDH}	HCID2	HCID3	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	V_{DD}	GPIO31	GPIO29	V_{DDH}	GPIO4	V_{DDH}	GND	GPIO8
E	TCK	TRST	TMS	HRESET	GPIO27	HCID0	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	GND	V_{DD}	GND	GND	GPIO9	GPIO13	GPIO10	GPIO12
F	PO RESET	RST CONF	NMI	HA29	HA22	GND	V_{DD}	V_{DD}	V_{DD}	GND	V_{DD}	GND	V_{DD}	ETHRX CLK	ETHTX CLK	GPIO20	GPIO18	GPIO16	GPIO11	GPIO14	GPIO19
G	HA24	HA27	HA25	HA23	HA17	PWE0	V_{DD}	V_{DD}	BADDR 31	BM0	ABB	V_{DD}	INT OUT	ETHCR S	V_{DD}	CS1	BCTL0	GPIO15	GND	GPIO17	GPIO22
H	HA20	HA28	V_{DD}	HA19	TEST	PSD CAS	PGTA	V_{DD}	BM1	ARTRY	AACK	DBB	HTA	V_{DD}	TT4	CS4	GPIO24	GPIO21	V_{DD}	V_{DDH}	A31
J	HA18	HA26	V_{DD}	HA13	GND	PSDA MUX	BADDR 27	V_{DD}	CLKIN	BM2	DBG	V_{DD}	GND	V_{DD}	TT3	PSDA10	BCTL1	GPIO23	GND	GPIO25	A30
K	HA15	HA21	HA16	PWE3	PWE1	POE	BADDR 30	Res.	GND	GND	GND	GND	CLKOUT	V_{DD}	TT2	ALE	CS2	GND	A26	A29	A28
L	HA12	HA14	HA11	V_{DDH}	V_{DDH}	BADDR 28	BADDR 29	GND	GND				GND	V_{DDH}	GND	GND	CS3	V_{DDH}	A27	A25	A22
M	HD28	HD31	V_{DDH}	GND	GND	GND	V_{DD}	V_{DDH}	GND		MSC8122		GND	V_{DDH}	HB RST	V_{DDH}	V_{DDH}	GND	V_{DDH}	A24	A21
N	HD26	HD30	HD29	HD24	PWE2	V_{DDH}	HWBS 0	HBCS	GND				GND	HRDS	BG	HCS	CS0	PSDWE	GPIO26	A23	A20
P	HD20	HD27	HD25	HD23	HWBS 3	HWBS 2	HWBS 1	HCLKIN	GND	GND_{SYN}	V_{CCSYN}	GND	GND	TA	BR	TEA	PSD VAL	DP0	V_{DDH}	GND	A19
R	HD18	V_{DDH}	GND	HD22	HWBS 6	HWBS 4	TSZ1	TSZ3	GBL	V_{DD}	V_{DD}	V_{DD}	TT0	DP7	DP6	DP3	TS	DP2	A17	A18	A16
T	HD17	HD21	HD1	HD0	HWBS 7	HWBS 5	TSZ0	TSZ2	TBST	V_{DD}	D16	TT1	D21	D23	DP5	DP4	DP1	D30	GND	A15	A14
U	HD16	HD19	HD2	D2	D3	D6	D8	D9	D11	D14	D15	D17	D19	D22	D25	D26	D28	D31	V_{DDH}	A12	A13
V	HD3	V_{DDH}	GND	D0	D1	D4	D5	D7	D10	D12	D13	D18	D20	GND	D24	D27	D29	A8	A9	A10	A11
W	HD6	HD5	HD4	GND	GND	V_{DDH}	V_{DDH}	GND	HDST1	HDST0	V_{DDH}	GND	HD40	V_{DDH}	HD33	V_{DDH}	HD32	GND	GND	A7	A6
Y	HD7	HD15	V_{DDH}	HD9	V_{DD}	HD60	HD58	GND	V_{DDH}	HD51	GND	V_{DDH}	HD43	GND	V_{DDH}	GND	HD37	HD34	V_{DDH}	A4	A5
AA	V_{DD}	HD14	HD12	HD10	HD63	HD59	GND	V_{DDH}	HD54	HD52	V_{DDH}	GND	V_{DDH}	HD46	GND	HD42	HD38	HD35	A0	A2	A3
AB	GND	HD13	HD11	HD8	HD62	HD61	HD57	HD56	HD55	HD53	HD50	HD49	HD48	HD47	HD45	HD44	HD41	HD39	HD36	A1	V_{DD}

Figure 3. MSC8122 Package, Top View

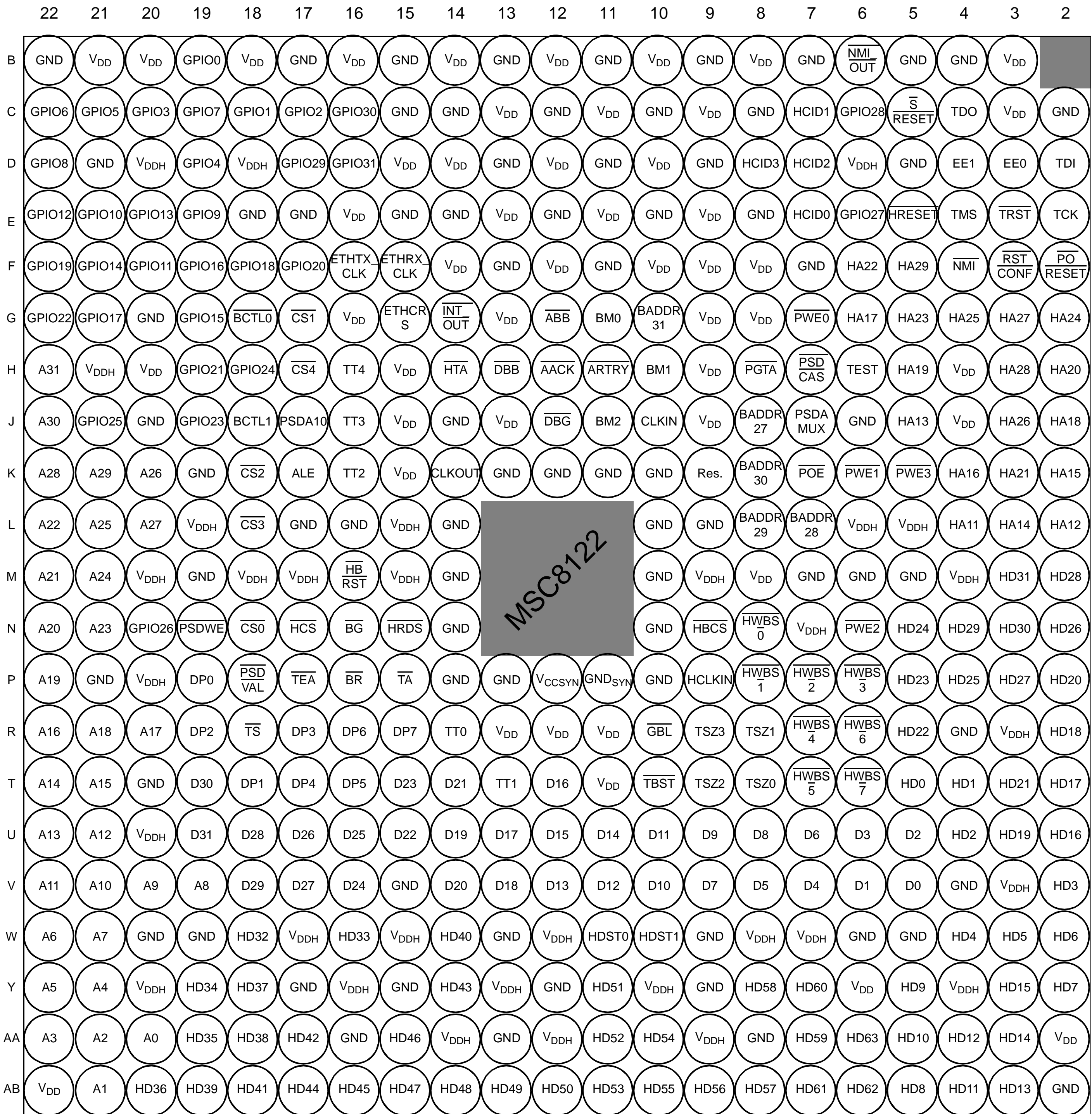


Figure 4. MSC8122 Package, Bottom View

Table 1. MSC8122 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
M15	V_{DDH}	P12	V_{CCSYN}
M16	HBRST	P13	GND
M17	V_{DDH}	P14	GND
M18	V_{DDH}	P15	TA
M19	GND	P16	BR
M20	V_{DDH}	P17	TEA
M21	A24	P18	PSDVAL
M22	A21	P19	DP0/DREQ1/EXT_BR2
N2	HD26	P20	V_{DDH}
N3	HD30	P21	GND
N4	HD29	P22	A19
N5	HD24	R2	HD18
N6	PWE2/PSDDQM2/PBS2	R3	V_{DDH}
N7	V_{DDH}	R4	GND
N8	HWBS0/HDBS0/HWBE0/HDBE0	R5	HD22
N9	HBCS	R6	HWBS6/HDBS6/HWBE6/HDBE6/PWE6/PSDDQM6/PBS6
N10	GND	R7	HWBS4/HDBS4/HWBE4/HDBE4/PWE4/PSDDQM4/PBS4
N14	GND	R8	TSZ1
N15	HRDS/HRW/HRDE	R9	TSZ3
N16	BG	R10	IRQ1/GBL
N17	HCS	R11	V_{DD}
N18	CS0	R12	V_{DD}
N19	PSDWE/PGPL1	R13	V_{DD}
N20	GPIO26/TDM0RDAT	R14	TT0/HA7
N21	A23	R15	IRQ7/DP7/DREQ4
N22	A20	R16	IRQ6/DP6/DREQ3
P2	HD20	R17	IRQ3/DP3/DREQ2/EXT_BR3
P3	HD27	R18	TS
P4	HD25	R19	IRQ2/DP2/DACK2/EXT_DBG2
P5	HD23	R20	A17
P6	HWBS3/HDBS3/HWBE3/HDBE3	R21	A18
P7	HWBS2/HDBS2/HWBE2/HDBE2	R22	A16
P8	HWBS1/HDBS1/HWBE1/HDBE1	T2	HD17
P9	HCLKIN	T3	HD21
P10	GND	T4	HD1/DSISYNC
P11	GND_{SYN}	T5	HD0/SWTE

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8122 Reference Manual*.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8122.

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core and PLL supply voltage	V_{DD}	–0.2 to 1.6	V
I/O supply voltage	V_{DDH}	–0.2 to 4.0	V
Input voltage	V_{IN}	–0.2 to 4.0	V
Maximum operating temperature: • Standard range • Extended range	T_J	 90 105	 °C °C
Minimum operating temperature • Standard range • Extended range	T_J	 0 –40	 °C °C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in **Table 3.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. **Section 3.5**, *Thermal Considerations* includes a formula for computing the chip junction temperature (T_J).

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core and PLL supply voltage: • Standard — 400 MHz — 500 MHz • Reduced (300 and 400 MHz)	V_{DD} V_{CCSYN}	 1.14 to 1.26 1.16 to 1.24 1.07 to 1.13	 V V V
I/O supply voltage	V_{DDH}	3.135 to 3.465	V
Input voltage	V_{IN}	–0.2 to V_{DDH}+0.2	V
Operating temperature range: • Standard • Extended	 T_J T_J	 0 to 90 –40 to 105	 °C °C

2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC8122 for the FC-PBGA packages.

Table 4. Thermal Characteristics for the MSC8122

Characteristic	Symbol	FC-PBGA 20 × 20 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	26	21	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	19	15	°C/W
Junction-to-board (bottom)[4]	$R_{\theta JB}$	9		°C/W
Junction-to-case[5]	$R_{\theta JC}$	0.9		°C/W
Junction-to-package-top[6]	Ψ_{JT}	1		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Section 3.5, *Thermal Considerations* provides a detailed explanation of these characteristics.

2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8122. The measurements in **Table 5** assume the following system conditions:

- T_A = 25 °C
- V_{DD} =
  - — 300/400 MHz 1.1 V nominal = 1.07–1.13 V_{DC}
  - — 400 MHz 1.2 V nominal = 1.14–1.26 V_{DC}
  - — 500 MHz 1.2 V nominal = 1.16–1.24 V_{DC}
- V_{DDH} = 3.3 V ± 5% V_{DC}
- GND = 0 V_{DC}

Note: The leakage current is measured for nominal V_{DDH} and V_{DD}.

Table 5. DC Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Input high voltage[1], all inputs except CLKIN	V_{IH}	2.0	—	3.465	V
Input low voltage[1]	V_{IL}	GND	0	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.0	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0	0.8	V
Input leakage current, $V_{IN} = V_{DDH}$	I_{IN}	–1.0	0.09	1	μA
Tri-state (high impedance off state) leakage current, $V_{IN} = V_{DDH}$	I_{OZ}	–1.0	0.09	1	μA
Signal low input current, V_{IL} = 0.8 V[2]	I_L	–1.0	0.09	1	μA
Signal high input current, V_{IH} = 2.0 V[2]	I_H	–1.0	0.09	1	μA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.0	3.0	—	V
Output low voltage, I_{OL}= 3.2 mA	V_{OL}	—	0	0.4	V
V_{CCSYN} PLL supply current	I_{VCCSYN}	—	2	4	mA
Internal supply current: • Wait mode • Stop mode	 I_{DDW} I_{DDS}	 — —	 375[3] 290[3]	 — —	 mA mA
Typical power 400 MHz at 1.2 V[4]	P	—	1.15	—	W

Notes:
1. See **Figure 5** for undershoot and overshoot voltages.
2. Not tested. Guaranteed by design.
3. Measured for 1.2 V core at 25°C junction temperature.
4. The typical power values were measured using an EFR code with the device running at a junction temperature of 25°C. No peripherals were enabled and the ICache was not enabled. The source code was optimized to use all the ALUs and AGUs and all four cores. It was created using CodeWarrior® 2.5. These values are provided as examples only. Power consumption is application dependent and varies widely. To assure proper board design with regard to thermal dissipation and maintaining proper operating temperatures, evaluate power consumption for your application and use the design guidelines in **Chapter 4** of this document and in *MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines* (AN2601).

2.5.5 System Bus Access Timing

2.5.5.1 Core Data Transfers

Generally, all MSC8122 bus and system output signals are driven from the rising edge of the reference clock (REFCLK). The REFCLK is the CLKIN signal. Memory controller signals, however, trigger on four points within a REFCLK cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge of REFCLK (and T3 at the falling edge), but the spacing of T2 and T4 depends on the PLL clock ratio selected, as **Table 13** shows.

Table 13. Tick Spacing for Memory Controller Signals

BCLK/SC140 clock	Tick Spacing (T1 Occurs at the Rising Edge of REFCLK)		
	T2	T3	T4
1:4, 1:6, 1:8, 1:10	1/4 REFCLK	1/2 REFCLK	3/4 REFCLK
1:3	1/6 REFCLK	1/2 REFCLK	4/6 REFCLK
1:5	2/10 REFCLK	1/2 REFCLK	7/10 REFCLK

Figure 10 is a graphical representation of **Table 13**.

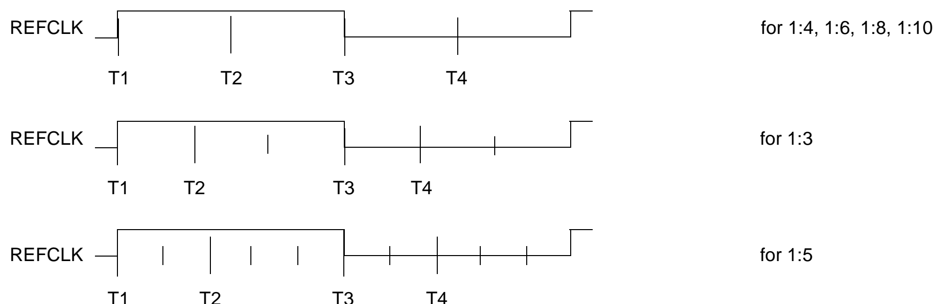


Figure 10. Internal Tick Spacing for Memory Controller Signals

Table 15. AC Timing for SIU Outputs

No.	Characteristic	Value for Bus Speed in MHz[3]				Units
		Ref = CLKIN			Ref = CLKOUT	
		1.1 V	1.2 V	1.2 V	1.2 V	
		100/ 133	133	166	100/133	
30[2]	Minimum delay from the 50% level of the REFCLK for all signals	0.9	0.8	0.8	1.0	ns
31	PSDVAL/TEA/TA max delay from the 50% level of the REFCLK rising edge	6.0	4.9	4.9	5.8	ns
32a	Address bus max delay from the 50% level of the REFCLK rising edge • Multi-master mode (SIUBCR[EBM] = 1) • Single-master mode (SIUBCR[EBM] = 0)	 6.4 5.3	 5.5 4.2	 5.5 3.9	 6.4 5.1	 ns ns
32b	Address attributes: TT[0–1]/TBST/TSZ/GBL max delay from the 50% level of the REFCLK rising edge	6.4	5.1	5.1	6.0	ns
32c	Address attributes: TT[2–4]/TC max delay from the 50% level of the REFCLK rising edge	6.9	5.7	5.7	6.6	ns
32d	BADDR max delay from the 50% level of the REFCLK rising edge	5.2	4.2	4.2	5.1	ns
33a	Data bus max delay from the 50% level of the REFCLK rising edge • Data-pipeline mode • Non-pipeline mode	 4.8 7.1	 3.9 6.1	 3.7 6.1	 4.8 7.0	 ns ns
33b	DP max delay from the 50% level of the REFCLK rising edge • Data-pipeline mode • Non-pipeline mode	 6.0 7.5	 5.3 6.5	 5.3 6.5	 6.2 7.4	 ns ns
34	Memory controller signals/ALE/CS[0–4] max delay from the 50% level of the REFCLK rising edge	5.1	4.2	3.9	5.1	ns
35a	DBG/BG/BR/DBB max delay from the 50% level of the REFCLK rising edge	6.0	4.7	4.7	5.6	ns
35b	AACK/ABB/TS/CS[5–7] max delay from the 50% level of the REFCLK rising edge	5.5	4.5	4.5	5.4	ns

Notes:

1. Values are measured from the 50% level of the REFCLK rising edge to the 50% signal level and assume a 20 pF load except where otherwise specified.
2. Except for specification 30, which is specified for a 10 pF load, all timings in this table are specified for a 20 pF load. Decreasing the load results in a timing decrease at the rate of 0.3 ns per 5 pF decrease in load. Increasing the load results in a timing increase at the rate of 0.15 ns per 5 pF increase in load.
3. The maximum bus frequency depends on the mode:
   - In 60x-compatible mode connected to another MSC8122 device, the frequency is determined by adding the input and output longest timing values, which results in the total delay for 20 pF output capacitance. You must also account for other influences that can affect timing, such as on-board clock skews, on-board noise delays, and so on.
   - In single-master mode, the frequency depends on the timing of the devices connected to the MSC8122.
   - To achieve maximum performance on the bus in single-master mode, disable the DBB signal by writing a 1 to the SIUMCR[BDD] bit. See the SIU chapter in the *MSC8122 Reference Manual* for details.

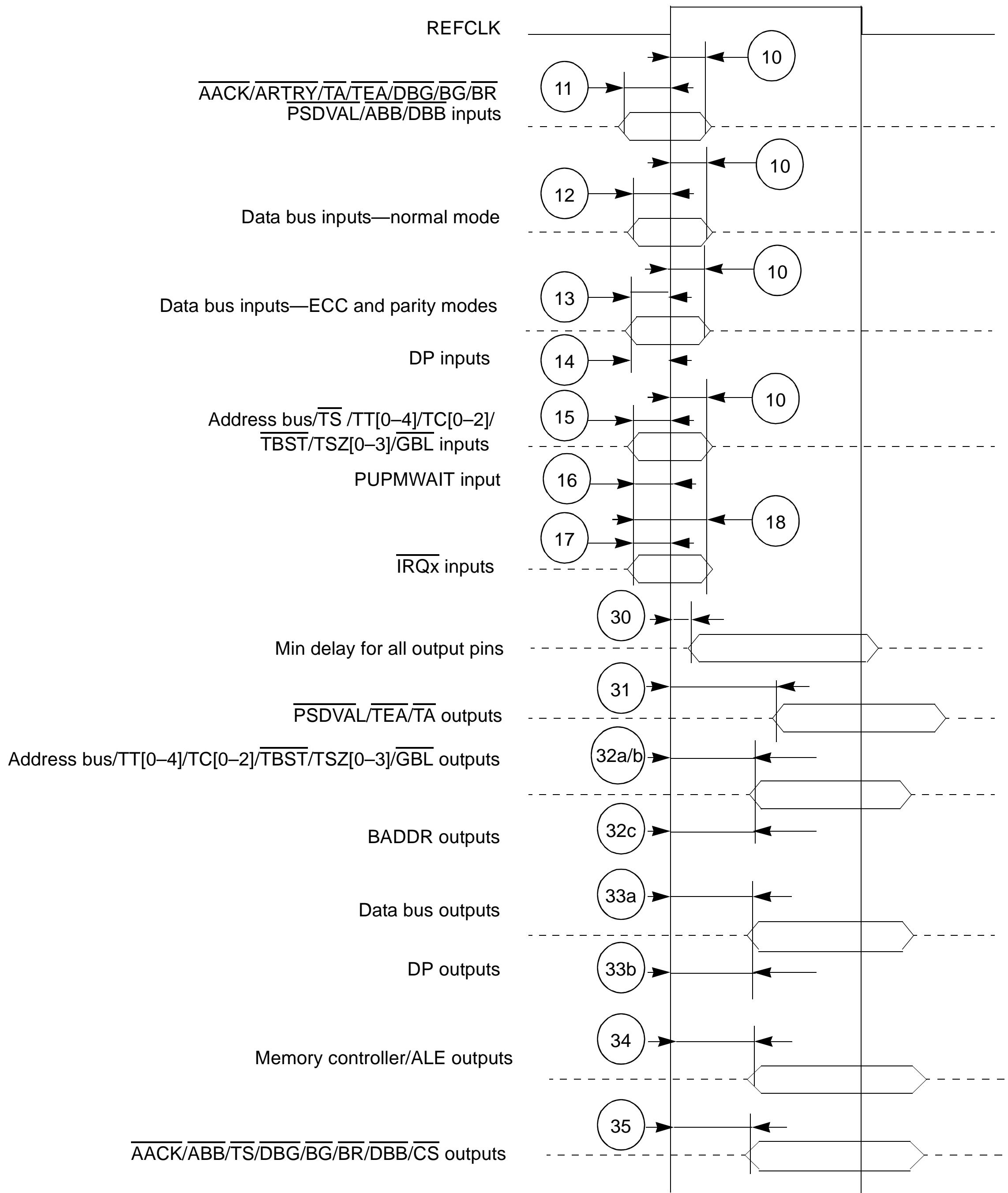


Figure 11. SIU Timing Diagram

2.5.6 DSI Timing

The timings in the following sections are based on a 20 pF capacitive load.

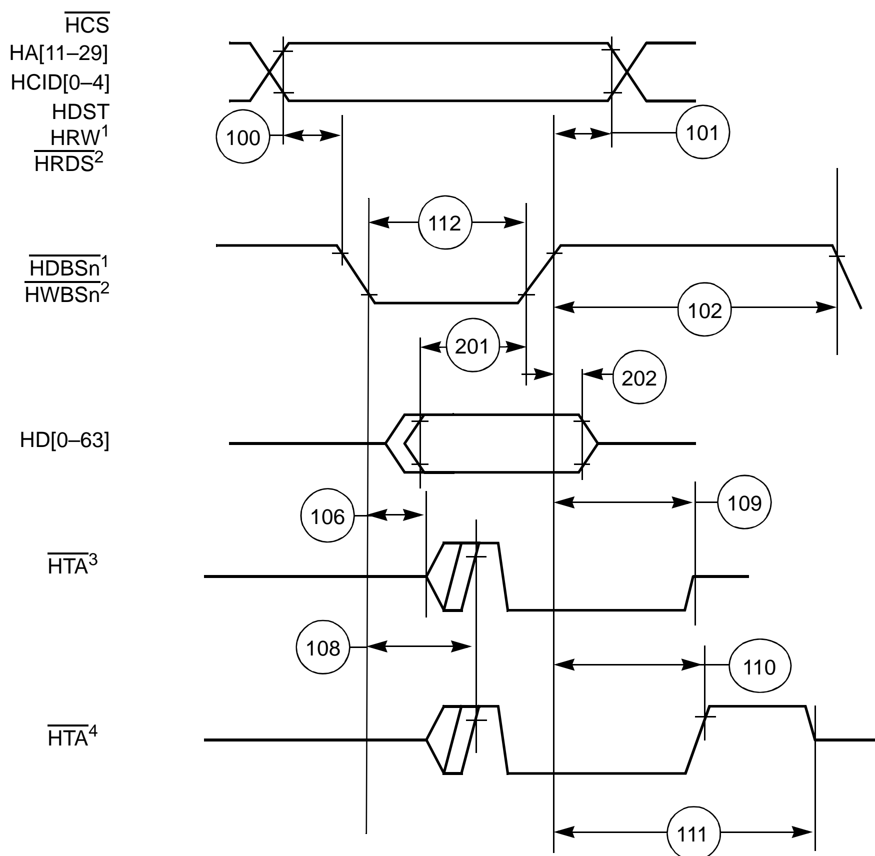
2.5.6.1 DSI Asynchronous Mode

Table 18. DSI Asynchronous Mode Timing

No.	Characteristics	Min	Max	Unit
100	Attributes[1] set-up time before strobe (HWBS[n]) assertion	1.5	—	ns
101	Attributes[1] hold time after data strobe deassertion	1.3	—	ns
102	Read/Write data strobe deassertion width: • DCR[HTAAD] = 1 — Consecutive access to the same DSI — Different device with DCR[HTADT] = 01 — Different device with DCR[HTADT] = 10 — Different device with DCR[HTADT] = 11 • DCR[HTAAD] = 0	 $1.8 + T_{REFCLK}$ $5 + T_{REFCLK}$ $5 + (1.5 \times T_{REFCLK})$ $5 + (2.5 \times T_{REFCLK})$ $1.8 + T_{REFCLK}$	—	 ns ns ns ns ns
103	Read data strobe deassertion to output data high impedance	—	8.5	ns
104	Read data strobe assertion to output data active from high impedance	2.0	—	ns
105	Output data hold time after read data strobe deassertion	2.2	—	ns
106	Read/Write data strobe assertion to HTA active from high impedance	2.2	—	ns
107	Output data valid to HTA assertion	3.2	—	ns
108	Read/Write data strobe assertion to HTA valid[2] • 1.1 V core • 1.2 V core	 — —	 7.4 6.7	 ns ns
109	Read/Write data strobe deassertion to output HTA high impedance. (DCR[HTAAD] = 0, HTA at end of access released at logic 0)	—	6.5	ns
110	Read/Write data strobe deassertion to output HTA deassertion. (DCR[HTAAD] = 1, HTA at end of access released at logic 1)	—	6.5	ns
111	Read/Write data strobe deassertion to output HTA high impedance. (DCR[HTAAD] = 1, HTA at end of access released at logic 1 • DCR[HTADT] = 01 • DCR[HTADT] = 10 • DCR[HTADT] = 11	—	 $5 + T_{REFCLK}$ $5 + (1.5 \times T_{REFCLK})$ $5 + (2.5 \times T_{REFCLK})$	 ns ns ns
112	Read/Write data strobe assertion width	$1.8 + T_{REFCLK}$	—	ns
201	Host data input set-up time before write data strobe deassertion	1.0	—	ns
202	Host data input hold time after write data strobe deassertion • 1.1 V core • 1.2 V core	 1.7 1.5	 — —	 ns ns

Notes:
1. *Attributes* refers to the following signals: HCS, HA[11–29], HCID[0–4], HDST, HRW, HRDS, and HWBSn.
2. This specification is tested in dual-strobe mode. Timing in single-strobe mode is guaranteed by design.
3. All values listed in this table are tested or guaranteed by design.

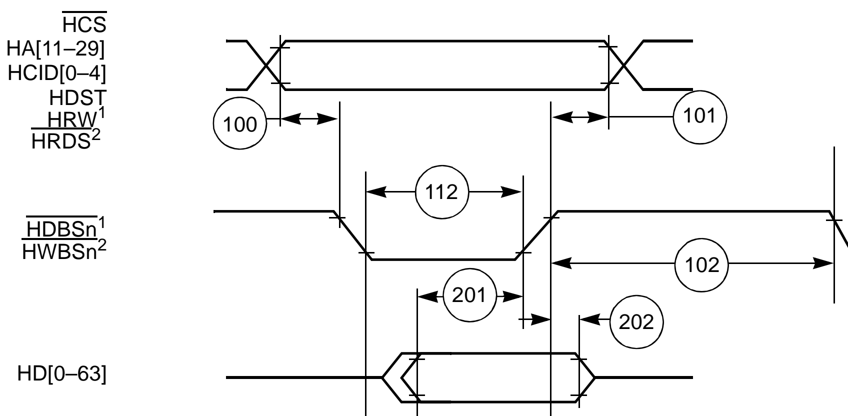
Figure 15 shows DSI asynchronous write signals timing.



Notes:
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.
3. HTA released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
4. HTA released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

Figure 15. Asynchronous Single- and Dual-Strobe Modes Write Timing Diagram

Figure 16 shows DSI asynchronous broadcast write signals timing.



Notes:
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.

Figure 16. Asynchronous Broadcast Write Timing Diagram

2.5.8 UART Timing

Table 22. UART Timing

No.	Characteristics	Expression	Min	Max	Unit
400	URXD and UTXD inputs high/low duration	$16 \times T_{REFCLK}$	160.0	—	ns
401	URXD and UTXD inputs rise/fall time			10	ns
402	UTXD output rise/fall time			10	ns

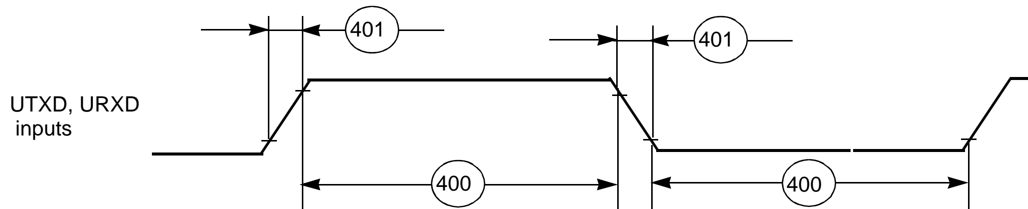


Figure 20. UART Input Timing

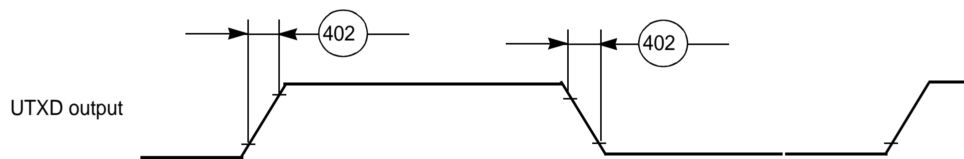


Figure 21. UART Output Timing

2.5.9 Timer Timing

Table 23. Timer Timing

No.	Characteristics	Ref = CLKIN		Unit
		Min	Max	
500	TIMERx frequency	10.0	—	ns
501	TIMERx Input high period	4.0	—	ns
502	TIMERx Output low period	4.0	—	ns
503	TIMERx Propagations delay from its clock input • 1.1 V core • 1.2 V core	 3.1 2.8	 9.5 8.1	 ns ns

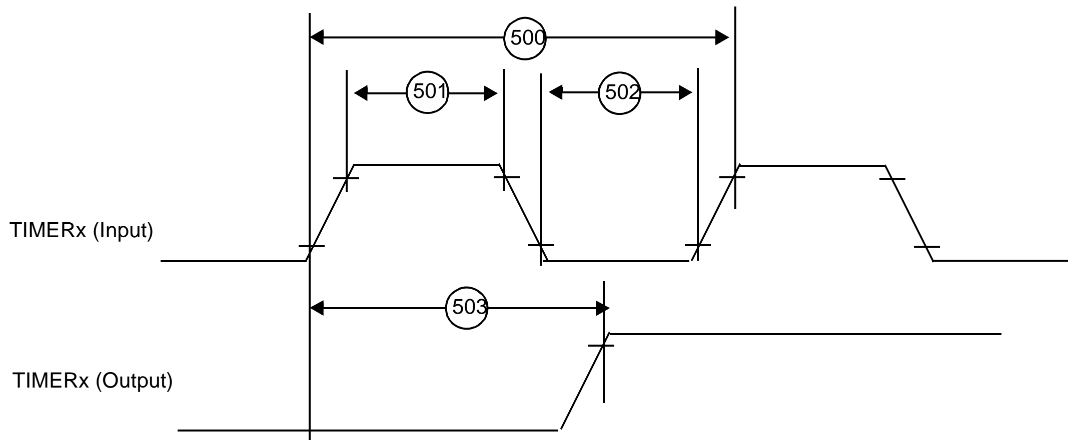


Figure 22. Timer Timing

2.5.10 Ethernet Timing

2.5.10.1 Management Interface Timing

Table 24. Ethernet Controller Management Interface Timing

No.	Characteristics	Min	Max	Unit
801	ETHMDIO to ETHMDC rising edge set-up time	10	—	ns
802	ETHMDC rising edge to ETHMDIO hold time	10	—	ns

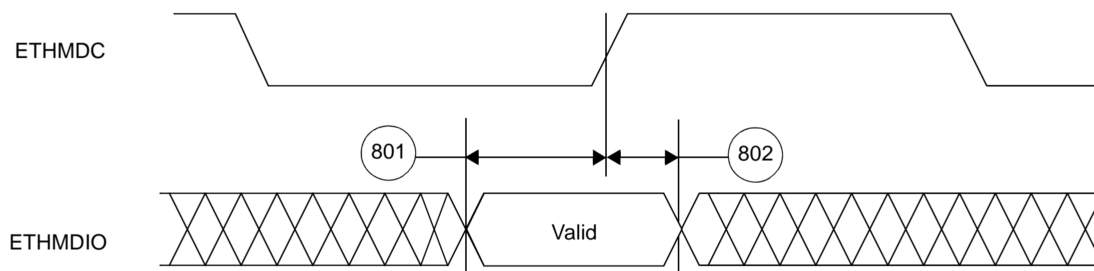


Figure 23. MDIO Timing Relationship to MDC

2.5.10.2 MII Mode Timing

Table 25. MII Mode Signal Timing

No.	Characteristics	Min	Max	Unit
803	ETHRX_DV, ETHRXD[0–3], ETHRX_ER to ETHRX_CLK rising edge set-up time	3.5	—	ns
804	ETHRX_CLK rising edge to ETHRX_DV, ETHRXD[0–3], ETHRX_ER hold time	3.5	—	ns
805	ETHTX_CLK to ETHTX_EN, ETHTXD[0–3], ETHTX_ER output delay • 1.1 V core • 1.2 V core	 1 1	 14.6 12.6	 ns ns

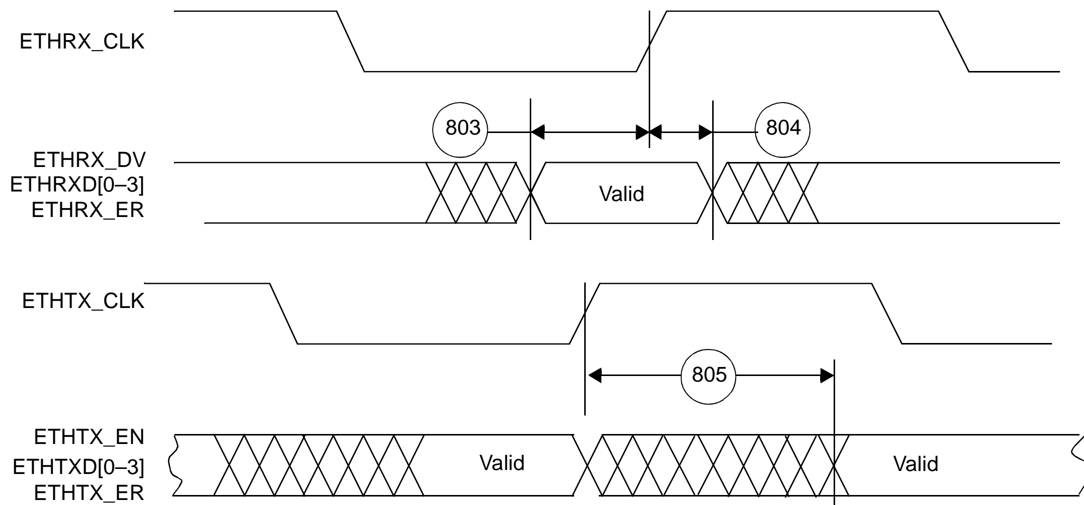


Figure 24. MII Mode Signal Timing

2.5.10.3 RMII Mode

Table 26. RMII Mode Signal Timing

No.	Characteristics	1.1 V Core		1.2 V Core		Unit
		Min	Max	Min	Max	
806	ETHTX_EN,ETHRXD[0–1], ETHCRS_DV, ETHRX_ER to ETHREF_CLK rising edge set-up time	1.6	—	2	—	ns
807	ETHREF_CLK rising edge to ETHRXD[0–1], ETHCRS_DV, ETHRX_ER hold time	1.6	—	1.6	—	ns
811	ETHREF_CLK rising edge to ETHTXD[0–1], ETHTX_EN output delay.	3	12.5	3	11	ns

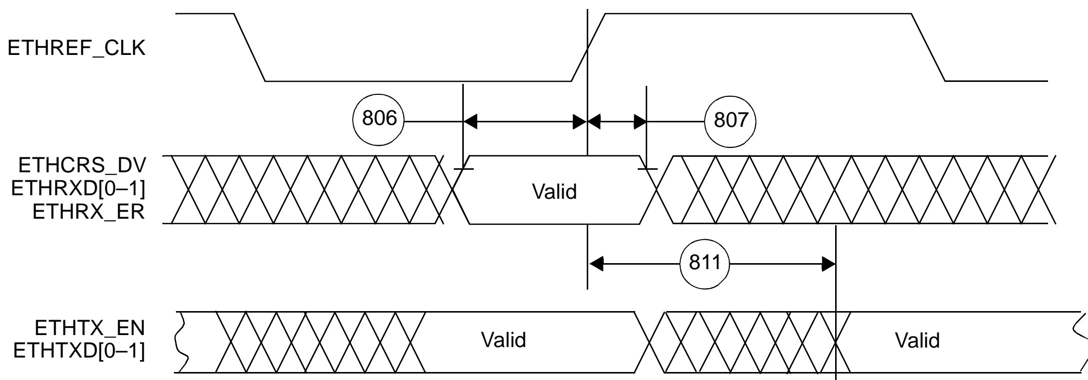


Figure 25. RMII Mode Signal Timing

2.5.10.4 SMII Mode

Table 27. SMII Mode Signal Timing

No.	Characteristics	Min	Max	Unit
808	ETHSYNC_IN, ETHRXD to ETHCLOCK rising edge set-up time	1.0	—	ns
809	ETHCLOCK rising edge to ETHSYNC_IN, ETHRXD hold time	1.0	—	ns
810	ETHCLOCK rising edge to ETHSYNC, ETHTXD output delay • 1.1 V core. • 1.2 V core.	 1.5[1] 1.5[1]	 6.0[2] 5.0[2]	 ns ns
Notes:	**1.** Measured using a 5 pF load. **2.** Measured using a 15 pF load.			

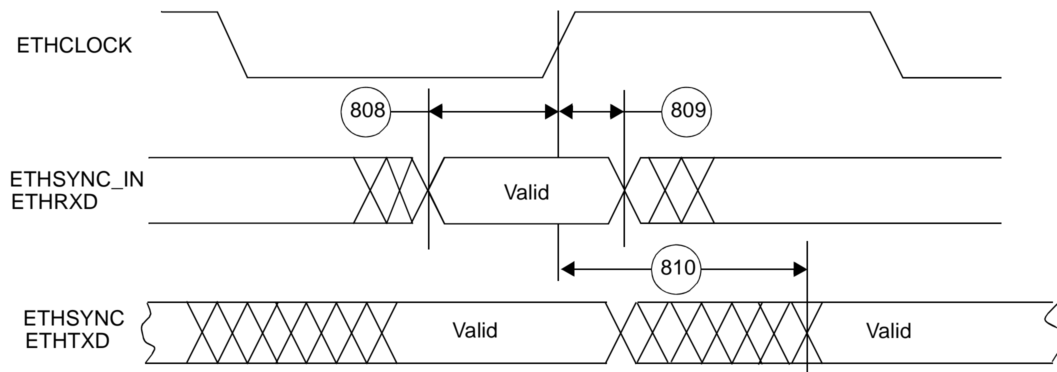


Figure 26. SMII Mode Signal Timing

2.5.11 GPIO Timing

Table 28. GPIO Timing

No.	Characteristics	Ref = CLKIN		Ref = CLKOUT (1.2 V only)		Unit
		Min	Max	Min	Max	
601	REFCLK edge to GPIO out valid (GPIO out delay time)	—	6.1	—	6.9	ns
602	REFCLK edge to GPIO out not valid (GPIO out hold time)	1.1	—	1.3	—	ns
603	REFCLK edge to high impedance on GPIO out	—	5.4	—	6.2	ns
604	GPIO in valid to REFCLK edge (GPIO in set-up time)	3.5	—	3.7	—	ns
605	REFCLK edge to GPIO in not valid (GPIO in hold time)	0.5	—	0.5	—	ns

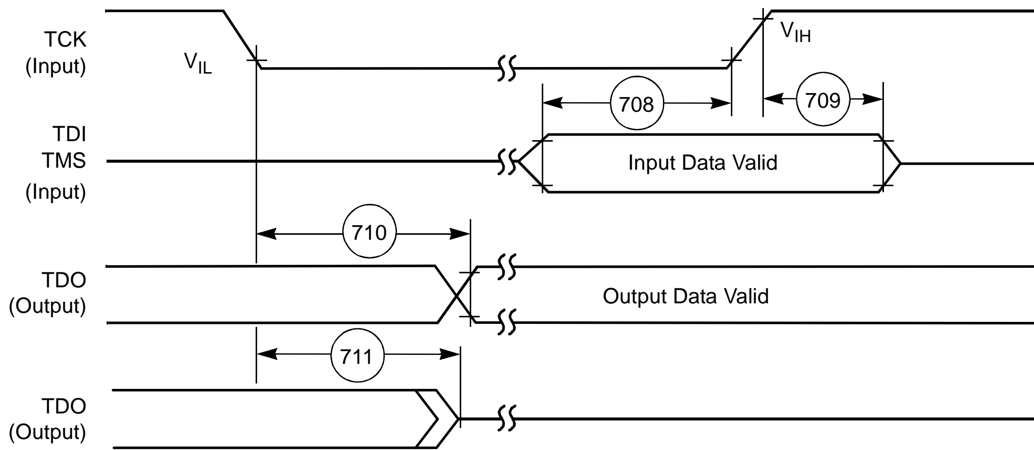


Figure 31. Test Access Port Timing Diagram

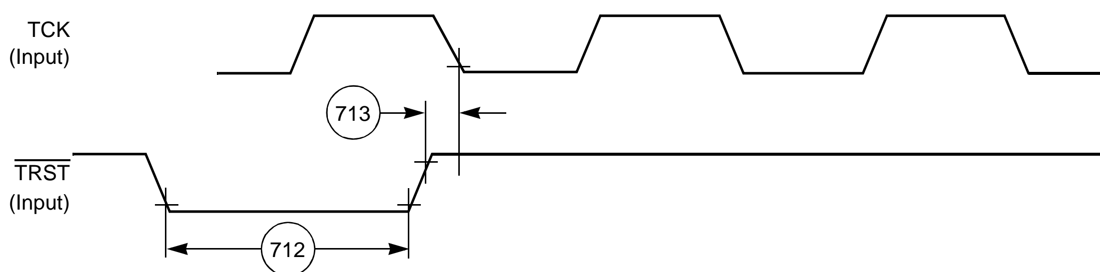


Figure 32. $\overline{TRST}$ Timing Diagram

3 Hardware Design Considerations

The following sections discuss areas to consider when the MSC8122 device is designed into a system.

3.1 Start-up Sequencing Recommendations

Use the following guidelines for start-up and power-down sequences:

- Assert $\overline{PORESET}$ and $\overline{TRST}$ before applying power and keep the signals driven low until the power reaches the required minimum power levels. This can be implemented via weak pull-down resistors.
- CLKIN can be held low or allowed to toggle during the beginning of the power-up sequence. However, CLKIN must start toggling before the deassertion of $\overline{PORESET}$ and after both power supplies have reached nominal voltage levels.
- If possible, bring up V_{DD}/V_{CCSYN} and V_{DDH} together. If it is not possible, raise V_{DD}/V_{CCSYN} first and then bring up V_{DDH}. V_{DDH} should not exceed V_{DD}/V_{CCSYN} until V_{DD}/V_{CCSYN} reaches its nominal voltage level. Similarly, bring both voltage levels down together. If that is not possible reverse the power-up sequence, with V_{DDH} going down first and then V_{DD}/V_{CCSYN}.

Note: This recommended power sequencing for the MSC8122 is different from the MSC8102. See **Section 2.5.2** for start-up timing specifications.

External voltage applied to any input line must not exceed the I/O supply V_{DDH} by more than 0.8 V at any time, including during power-up. Some designs require pull-up voltages applied to selected input lines during power-up for configuration purposes. This is an acceptable exception to the rule. However, each such input can draw up to 80 mA per input pin per device in the system during start-up.

During the power-up sequence, if V_{DD} rises before V_{DDH} (see **Figure 6**), current can pass from the V_{DD} supply through the device ESD protection circuits to the V_{DDH} supply. The ESD protection diode can allow this to occur when V_{DD} exceeds V_{DDH} by more than 0.8 V. Design the power supply to prevent or minimize this effect using one of the following optional methods:

- Never allow V_{DD} to exceed V_{DDH} + 0.8V.
- Design the V_{DDH} supply to prevent reverse current flow by adding a minimum 10 Ω resistor to GND to limit the current. Such a design yields an initial V_{DDH} level of V_{DD} – 0.8 V before it is enabled.

After power-up, V_{DDH} must not exceed V_{DD}/V_{CCSYN} by more than 2.6 V.

3.2 Power Supply Design Considerations

When used as a drop-in replacement in MSC8102 applications or when implementing a new design, use the guidelines described in *Migrating Designs from the MSC8102 to the MSC8122* (AN2716) and the *MSC8122 Design Checklist* (AN3374 for optimal system performance. *MSC8122 and MSC8126 Power Circuit Design Recommendations and Examples* (AN2937) provides detailed design information. See **Section 2.5.2** for start-up timing specifications.

Figure 33 shows the recommended power decoupling circuit for the core power supply. The voltage regulator and the decoupling capacitors should supply the required device current without any drop in voltage on the device pins. The voltage on the package pins should not drop below the minimum specified voltage level even for a very short spikes. This can be achieved by using the following guidelines:

- For the core supply, use a voltage regulator rated at 1.2 V with nominal rating of at least 3 A. This rating does not reflect actual average current draw, but is recommended because it resists changes imposed by transient spikes and has better voltage recovery time than supplies with lower current ratings.
- Decouple the supply using low-ESR capacitors mounted as close as possible to the socket. **Figure 33** shows three capacitors in parallel to reduce the resistance. Three capacitors is a recommended minimum number. If possible, mount at least one of the capacitors directly below the MSC8122 device.

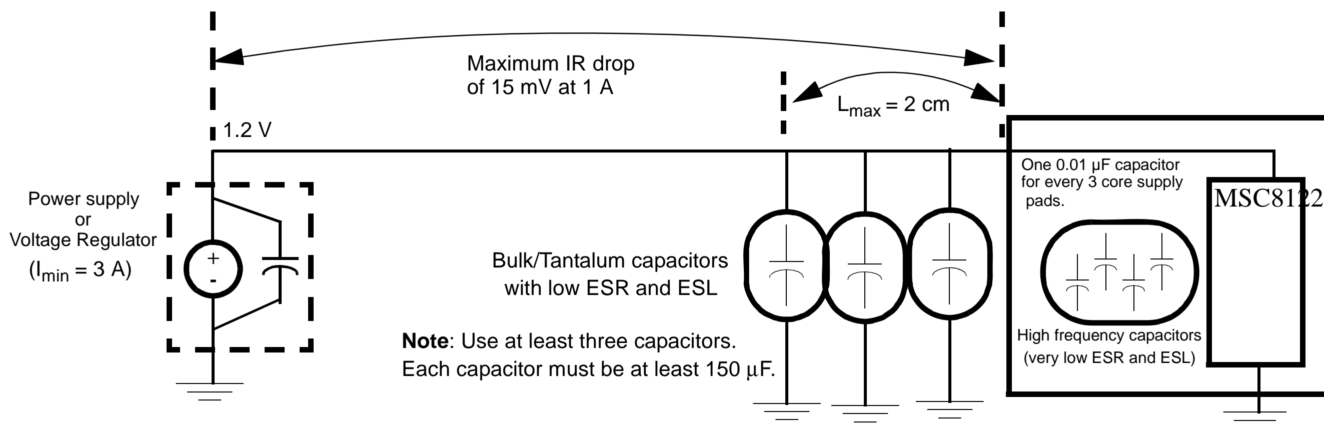


Figure 33. Core Power Supply Decoupling

Each V_{CC} and V_{DD} pin on the MSC8122 device should have a low-impedance path to the board power supply. Similarly, each GND pin should have a low-impedance path to the ground plane. The power supply pins drive distinct groups of logic on the chip. The V_{CC} power supply should have at least four 0.1 µF by-pass capacitors to ground located as closely as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC}, V_{DD}, and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MSC8122 have fast rise and fall times. PCB trace interconnection length should be minimized to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PCB trace lengths of six inches are recommended. For the DSI control signals in synchronous mode, ensure that the layout supports the DSI AC timing requirements and minimizes any signal crosstalk. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PCB traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC}, V_{DD}, and GND circuits. Pull up all unused inputs or signals that will be inputs during reset.

Special care should be taken to minimize the noise levels on the PLL supply pins. There is one pair of PLL supply pins: V_{CCSYN}-GND_{SYN}. To ensure internal clock stability, filter the power to the V_{CCSYN} input with a circuit similar to the one in

Figure 34. For optimal noise filtering, place the circuit as close as possible to V_{CCSYN}. The 0.01-µF capacitor should be closest to V_{CCSYN}, followed by the 10-µF capacitor, the 10-nH inductor, and finally the 10-Ω resistor to V_{DD}. These traces should be kept short and direct. Provide an extremely low impedance path to the ground plane for GND_{SYN}. Bypass GND_{SYN} to V_{CCSYN} by a 0.01-µF capacitor located as close as possible to the chip package. For best results, place this capacitor on the backside of the PCB aligned with the depopulated void on the MSC8122 located in the square defined by positions, L11, L12, L13, M11, M12, M13, N11, N12, and N13.

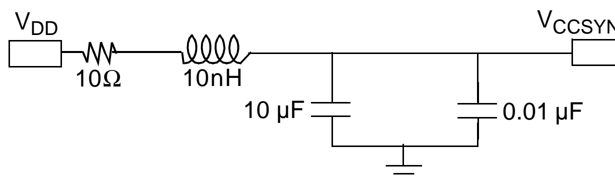


Figure 34. V_{CCSYN} Bypass

3.3 Connectivity Guidelines

Unused output pins can be disconnected, and unused input pins should be connected to the non-active value, via resistors to V_{DDH} or GND, except for the following:

- If the DSI is unused (DDR[DSIDIS] is set), $\overline{\text{HCS}}$ and $\overline{\text{HBCS}}$ must pulled up and all the rest of the DSI signals can be disconnected.
- When the DSI uses synchronous mode, $\overline{\text{HTA}}$ must be pulled up. In asynchronous mode, $\overline{\text{HTA}}$ should be pulled either up or down, depending on design requirements.
- $\overline{\text{HDST}}$ can be disconnected if the DSI is in big-endian mode, or if the DSI is in little-endian mode and the DCR[DSRFA] bit is set.
- When the DSI is in 64-bit data bus mode and DCR[BEM] is cleared, pull up $\overline{\text{HWBS[1–3]}}$/$\overline{\text{HDBS[1–3]}}$/$\overline{\text{HWBE[1–3]}}$/$\overline{\text{HDBE[1–3]}}$ and $\overline{\text{HWBS[4–7]}}$/$\overline{\text{HDBS[4–7]}}$/$\overline{\text{HWBE[4–7]}}$/$\overline{\text{HDBE[4–7]}}$/$\overline{\text{PWE[4–7]}}$/$\overline{\text{PSDDQM[4–7]}}$/$\overline{\text{PBS[4–7]}}$.
- When the DSI is in 32-bit data bus mode and DCR[BEM] is cleared, $\overline{\text{HWBS[1–3]}}$/$\overline{\text{HDBS[1–3]}}$/$\overline{\text{HWBE[1–3]}}$/$\overline{\text{HDBE[1–3]}}$ must be pulled up.
- When the DSI is in asynchronous mode, $\overline{\text{HBRST}}$ and HCLKIN should either be disconnected or pulled up.
- When the DSI uses sliding window address mode (DCR[SLDWA] = 1), the external HA[11–13] signals must be connected (tied) to the correct voltage levels so that the host can perform the first access to the DCR. After reset, the DSI expects full address mode (DCR[SLDWA] = 0). The DCR address in the DSI memory map is 0x1BE000, which requires the following connections:
  - HA11 must be pulled high (1)
  - HA12 must be pulled high (1)
  - HA13 must be pulled low (0)
- The following signals must be pulled up: $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, $\overline{\text{ARTRY}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{PSDVAL}}$, and $\overline{\text{AACK}}$.
- In single-master mode (BCR[EBM] = 0) with internal arbitration (PPC_ACR[EARB] = 0):
  - $\overline{\text{BG}}$, $\overline{\text{DBG}}$, and $\overline{\text{TS}}$ can be left unconnected.
  - $\overline{\text{EXT_BG[2–3]}}$, $\overline{\text{EXT_DBG[2–3]}}$, and $\overline{\text{GBL}}$ can be left unconnected if they are multiplexed to the system bus functionality. For any other functionality, connect the signal lines based on the multiplexed functionality.
  - $\overline{\text{BR}}$ must be pulled up.
  - $\overline{\text{EXT_BR[2–3]}}$ must be pulled up if multiplexed to the system bus functionality.
- If there is an external bus master (BCR[EBM] = 1):
  - $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{DBG}}$, and $\overline{\text{TS}}$ must be pulled up.
  - $\overline{\text{EXT_BR[2–3]}}$, $\overline{\text{EXT_BG[2–3]}}$, and $\overline{\text{EXT_DBG[2–3]}}$ must be pulled up if multiplexed to the system bus functionality.
- In single-master mode, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ can be selected as $\overline{\text{IRQ}}$ inputs and be connected to the non-active value. In other modes, they must be pulled up.

Note: The MSC8122 does not support DLL-enabled mode. For the following two clock schemes, ensure that the DLL is disabled (that is, the DLLDIS bit in the Hard Reset Configuration Word is set).

- If no system synchronization is required (for example, the design does not use SDRAM), you can use any of the available clock modes.
- In the CLKIN synchronization mode, use the following connections:
  - — Connect the oscillator output through a buffer to CLKIN.
  - — Connect the CLKIN buffer output to the slave device (for example, SDRAM) making sure that the delay path between the clock buffer to the MSC8122 and the SDRAM is equal (that is, has a skew less than 100 ps).
  - — Valid clock modes in this scheme are: 0, 7, 15, 19, 21, 23, 28, 29, 30, and 31.
- In CLKOUT synchronization mode (for 1.2 V devices), CLKOUT is the main clock to SDRAM. Use the following connections:
  - — Connect the oscillator output through a buffer to CLKIN.
  - — Connect CLKOUT through a zero-delay buffer to the slave device (for example, SDRAM) using the following guidelines:
    - – The maximum delay between the slave and CLKOUT must not exceed 0.7 ns.
    - – The maximum load on CLKOUT must not exceed 10 pF.
    - – Use a zero-delay buffer with a jitter less than 0.3 ns.
  - — All clock modes are valid in this clock scheme.

Note: See the Clock chapter in the *MSC8122 Reference Manual* for details.

- If the 60x-compatible system bus is not used and SIUMCR[PBSE] is set, $\overline{\text{PPBS}}$ can be disconnected. Otherwise, it should be pulled up.
- The following signals: SWTE, DSISYNC, DSI64, MODCK[1–2], CNFGS, CHIPID[0–3], RSTCONF and BM[0–2] are used to configure the MSC8122 and are sampled on the deassertion of the $\overline{\text{PORESET}}$ signal. Therefore, they should be tied to GND or V_{DDH} or through a pull-down or a pull-up resistor until the deassertion of the $\overline{\text{PORESET}}$ signal.
- When they are used, $\overline{\text{INT_OUT}}$ (if SIUMCR[INTODC] is cleared), $\overline{\text{NMI_OUT}}$, and $\overline{\text{IRQxx}}$ (if not full drive) signals must be pulled up.
- When the Ethernet controller is enabled and the SMII mode is selected, GPIO10 and GPIO14 must not be connected externally to any signal line.

Note: For details on configuration, see the *MSC8122 User's Guide* and *MSC8122 Reference Manual*. For additional information, refer to the *MSC8122 Design Checklist* (AN2787).

3.4 External SDRAM Selection

The external bus speed implemented in a system determines the speed of the SDRAM used on that bus. However, because of differences in timing characteristics among various SDRAM manufacturers, you may have use a faster speed rated SDRAM to assure efficient data transfer across the bus. For example, for 166 MHz operation, you may have to use 183 or 200 MHz SDRAM. Always perform a detailed timing analysis using the MSC8122 bus timing values and the manufacturer specifications for the SDRAM to ensure correct operation within your system design. The output delay listed in SDRAM specifications is usually given for a load of 30 pF. Scale the number to your specific board load using the typical scaling number provided by the SDRAM manufacturer.