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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	I ² C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f325ar9t6

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Address	Block	Register Label	Register Name	Reset Status	Remarks
002Ch 002Dh	MCC	MCCSR MCCBCR	Main Clock Control / Status Register Main Clock Controller: Beep Control Register	00h 00h	R/W R/W
002Eh to 0030h	Reserved Area (3 Bytes)				
0031h 0032h 0033h 0034h 0035h 0036h 0037h 0038h 0039h 003Ah 003Bh 003Ch 003Dh 003Eh 003Fh	TIMER A	TACR2 TACR1 TACSR TAIC1HR TAIC1LR TAOC1HR TAOC1LR TACHR TACLR TAACHR TAACLR TAIC2HR TAIC2LR TAOC2HR TAOC2LR	Timer A Control Register 2 Timer A Control Register 1 Timer A Control/Status Register Timer A Input Capture 1 High Register Timer A Input Capture 1 Low Register Timer A Output Compare 1 High Register Timer A Output Compare 1 Low Register Timer A Counter High Register Timer A Counter Low Register Timer A Alternate Counter High Register Timer A Alternate Counter Low Register Timer A Input Capture 2 High Register Timer A Input Capture 2 Low Register Timer A Output Compare 2 High Register Timer A Output Compare 2 Low Register	00h 00h xxxx x0xx b xxh xxh 80h 00h FFh FCh FFh FCh xxh xxh 80h 00h	R/W R/W R/W Read Only Read Only R/W R/W Read Only Read Only Read Only Read Only Read Only Read Only R/W R/W
0040h	Reserved Area (1 Byte)				
0041h 0042h 0043h 0044h 0045h 0046h 0047h 0048h 0049h 004Ah 004Bh 004Ch 004Dh 004Eh 004Fh	TIMER B	TBCR2 TBCR1 TBCSR TBIC1HR TBIC1LR TBOC1HR TBOC1LR TBCHR TBCLR TBACHR TBACLR TBIC2HR TBIC2LR TBOC2HR TBOC2LR	Timer B Control Register 2 Timer B Control Register 1 Timer B Control/Status Register Timer B Input Capture 1 High Register Timer B Input Capture 1 Low Register Timer B Output Compare 1 High Register Timer B Output Compare 1 Low Register Timer B Counter High Register Timer B Counter Low Register Timer B Alternate Counter High Register Timer B Alternate Counter Low Register Timer B Input Capture 2 High Register Timer B Input Capture 2 Low Register Timer B Output Compare 2 High Register Timer B Output Compare 2 Low Register	00h 00h xxxx x0xx b xxh xxh 80h 00h FFh FCh FFh FCh xxh xxh 80h 00h	R/W R/W R/W Read Only Read Only R/W R/W Read Only Read Only Read Only Read Only Read Only Read Only R/W R/W
0050h 0051h 0052h 0053h 0054h 0055h 0056h 0057h	SCI	SCISR SCIDR SCIBRR SCICR1 SCICR2 SCIERP SCIETPR	SCI Status Register SCI Data Register SCI Baud Rate Register SCI Control Register 1 SCI Control Register 2 SCI Extended Receive Prescaler Register Reserved area SCI Extended Transmit Prescaler Register	C0h xxh 00h x000 0000b 00h 00h ---	Read Only R/W R/W R/W R/W R/W R/W

5 CENTRAL PROCESSING UNIT

5.1 INTRODUCTION

This CPU has a full 8-bit architecture and contains six internal registers allowing efficient 8-bit data manipulation.

5.2 MAIN FEATURES

- Enable executing 63 basic instructions
- Fast 8-bit by 8-bit multiply
- 17 main addressing modes (with indirect addressing mode)
- Two 8-bit index registers
- 16-bit stack pointer
- Low power HALT and WAIT modes
- Priority maskable hardware interrupts
- Non-maskable software/hardware interrupts

5.3 CPU REGISTERS

The six CPU registers shown in Figure 1 are not present in the memory mapping and are accessed by specific instructions.

Accumulator (A)

The Accumulator is an 8-bit general purpose register used to hold operands and the results of the arithmetic and logic calculations and to manipulate data.

Index Registers (X and Y)

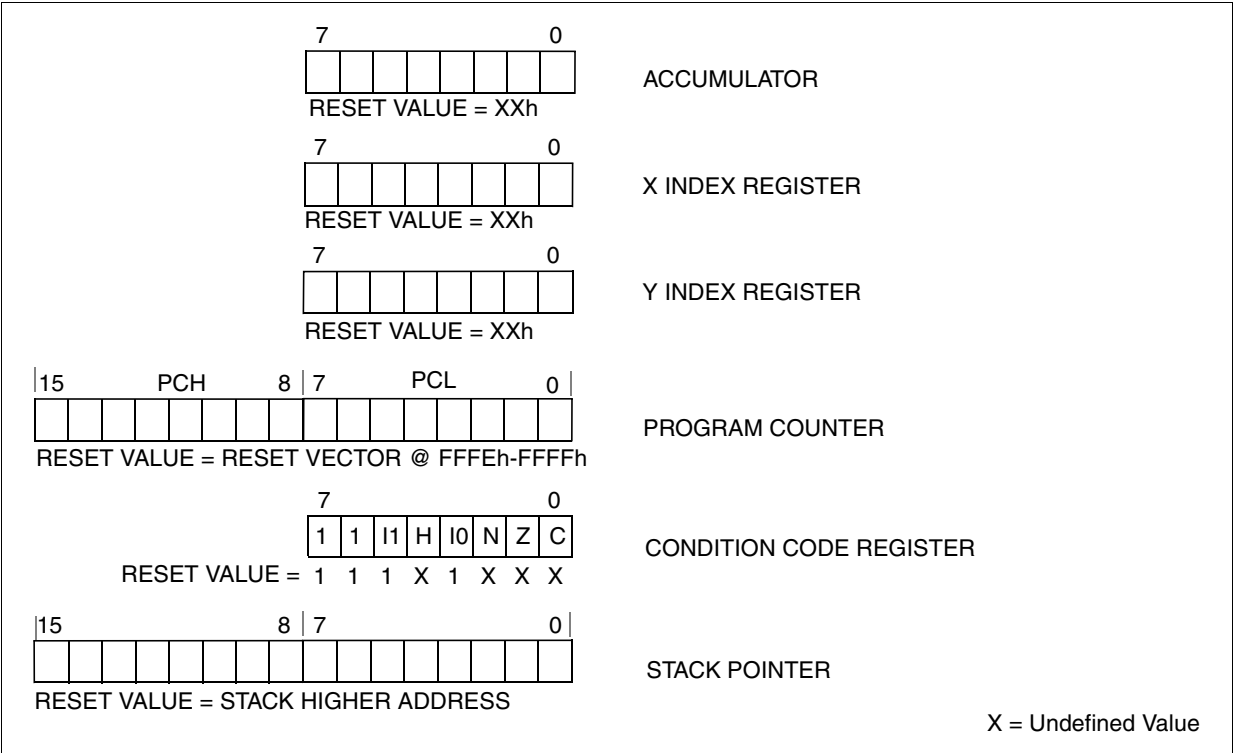
These 8-bit registers are used to create effective addresses or as temporary storage areas for data manipulation. (The Cross-Assembler generates a precede instruction (PRE) to indicate that the following instruction refers to the Y register.)

The Y register is not affected by the interrupt automatic procedures.

Program Counter (PC)

The program counter is a 16-bit register containing the address of the next instruction to be executed by the CPU. It is made of two 8-bit registers PCL (Program Counter Low which is the LSB) and PCH (Program Counter High which is the MSB).

Figure 10. CPU Registers



6 SUPPLY, RESET AND CLOCK MANAGEMENT

The device includes a range of utility features for securing the application in critical situations (for example in case of a power brown-out), and reducing the number of external components. An overview is shown in Figure 13.

For more details, refer to dedicated parametric section.

Main features

- Optional PLL for multiplying the frequency by 2 (not to be used with internal RC oscillator)
- Reset Sequence Manager (RSM)
- Multi-Oscillator Clock Management (MO)
 - 5 Crystal/Ceramic resonator oscillators
 - 1 Internal RC oscillator
- System Integrity Management (SI)
 - Main supply Low voltage detection (LVD)
 - Auxiliary Voltage detector (AVD) with interrupt capability for monitoring the main supply
 - Clock Security System (CSS) with Clock Filter and Backup Safe Oscillator (enabled by option byte)

6.1 PHASE LOCKED LOOP

If the clock frequency input to the PLL is in the range 2 to 4 MHz, the PLL can be used to multiply the frequency by two to obtain an f_{OSC2} of 4 to 8 MHz. The PLL is enabled by option byte. If the PLL is disabled, then $f_{OSC2} = f_{OSC}/2$.

Caution: The PLL is not recommended for applications where timing accuracy is required. See “PLL Characteristics” on page 154.

Figure 12. PLL Block Diagram

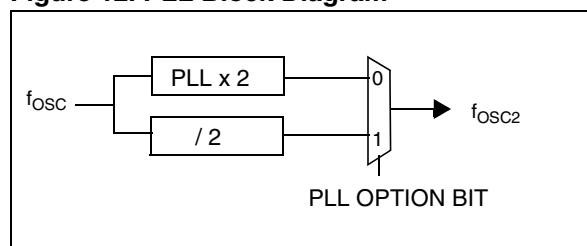
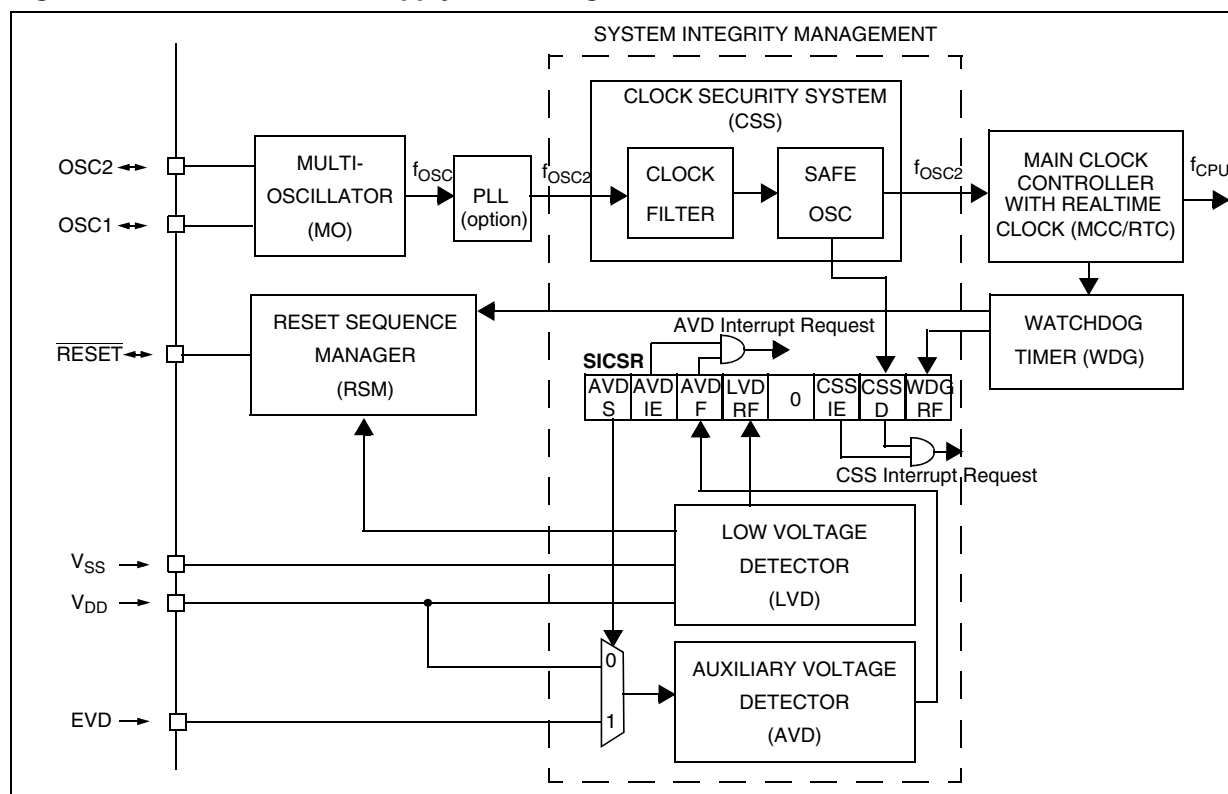


Figure 13. Clock, Reset and Supply Block Diagram



RESET SEQUENCE MANAGER (Cont'd)

The $\overline{\text{RESET}}$ pin is an asynchronous signal which plays a major role in EMS performance. In a noisy environment, it is recommended to follow the guidelines mentioned in the electrical characteristics section.

If the external $\overline{\text{RESET}}$ pulse is shorter than $t_{w(\text{RSTL})\text{out}}$ (see short ext. Reset in Figure 16), the signal on the $\overline{\text{RESET}}$ pin may be stretched. Otherwise the delay will not be applied (see long ext. Reset in Figure 16). Starting from the external $\overline{\text{RESET}}$ pulse recognition, the device $\overline{\text{RESET}}$ pin acts as an output that is pulled low during at least $t_{w(\text{RSTL})\text{out}}$.

6.3.3 External Power-On RESET

If the LVD is disabled by option byte, to start up the microcontroller correctly, the user must ensure by means of an external reset circuit that the reset signal is held low until V_{DD} is over the minimum level specified for the selected f_{OSC} frequency. (see "OPERATING CONDITIONS" on page 144)

A proper reset signal for a slow rising V_{DD} supply can generally be provided by an external RC network connected to the $\overline{\text{RESET}}$ pin.

6.3.4 Internal Low Voltage Detector (LVD) RESET

Two different RESET sequences caused by the internal LVD circuitry can be distinguished:

- Power-On RESET
- Voltage Drop RESET

The device $\overline{\text{RESET}}$ pin acts as an output that is pulled low when $V_{DD} < V_{IT+}$ (rising edge) or $V_{DD} < V_{IT-}$ (falling edge) as shown in Figure 16.

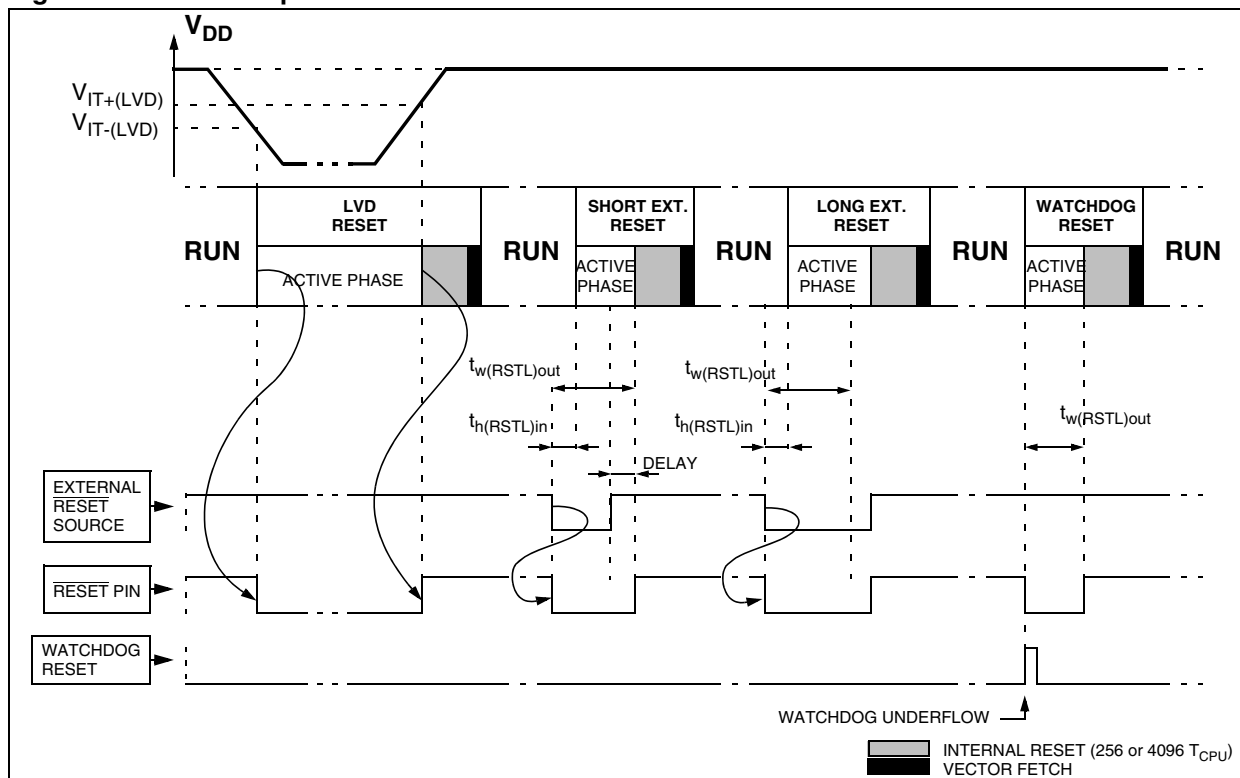
The LVD filters spikes on V_{DD} larger than $t_g(V_{DD})$ to avoid parasitic resets.

6.3.5 Internal Watchdog RESET

The RESET sequence generated by a internal Watchdog counter overflow is shown in Figure 16.

Starting from the Watchdog counter underflow, the device $\overline{\text{RESET}}$ pin acts as an output that is pulled low during at least $t_{w(\text{RSTL})\text{out}}$.

Figure 16. RESET Sequences



MAIN CLOCK CONTROLLER WITH REAL TIME CLOCK (Cont'd)

10.2.5 Low Power Modes

Mode	Description
WAIT	No effect on MCC/RTC peripheral. MCC/RTC interrupt cause the device to exit from WAIT mode.
ACTIVE-HALT	No effect on MCC/RTC counter (OIE bit is set), the registers are frozen. MCC/RTC interrupt cause the device to exit from ACTIVE-HALT mode.
HALT	MCC/RTC counter and registers are frozen. MCC/RTC operation resumes when the MCU is woken up by an interrupt with "exit from HALT" capability.

10.2.6 Interrupts

The MCC/RTC interrupt event generates an interrupt if the OIE bit of the MCCR register is set and the interrupt mask in the CC register is not active (RIM instruction).

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
Time base overflow event	OIF	OIE	Yes	No ¹⁾

Note:

The MCC/RTC interrupt wakes up the MCU from ACTIVE-HALT mode, not from HALT mode.

10.2.7 Register Description

MCC CONTROL/STATUS REGISTER (MCCR)

Read/Write

Reset Value: 0000 0000 (00h)

7

0

MCO	CP1	CP0	SMS	TB1	TB0	OIE	OIF
-----	-----	-----	-----	-----	-----	-----	-----

Bit 7 = **MCO** Main clock out selection

This bit enables the MCO alternate function on the PF0 I/O port. It is set and cleared by software.

0: MCO alternate function disabled (I/O pin free for general-purpose I/O)

1: MCO alternate function enabled (f_{CPU} on I/O port)

Note: To reduce power consumption, the MCO function is not active in ACTIVE-HALT mode.

Bit 6:5 = **CP[1:0]** CPU clock prescaler

These bits select the CPU clock prescaler which is applied in the different slow modes. Their action is conditioned by the setting of the SMS bit. These two bits are set and cleared by software

f_{CPU} in SLOW mode	CP1	CP0
$f_{OSC2} / 2$	0	0
$f_{OSC2} / 4$	0	1
$f_{OSC2} / 8$	1	0
$f_{OSC2} / 16$	1	1

Bit 4 = **SMS** Slow mode select

This bit is set and cleared by software.

0: Normal mode. $f_{CPU} = f_{OSC2}$

1: Slow mode. f_{CPU} is given by CP1, CP0

See Section 8.2 SLOW MODE and Section 10.2 MAIN CLOCK CONTROLLER WITH REAL TIME CLOCK AND BEEPER (MCC/RTC) for more details.

Bit 3:2 = **TB[1:0]** Time base control

These bits select the programmable divider time base. They are set and cleared by software.

Counter Prescaler	Time Base		TB1	TB0
	$f_{OSC2}=4MHz$	$f_{OSC2}=8MHz$		
16000	4ms	2ms	0	0
32000	8ms	4ms	0	1
80000	20ms	10ms	1	0
200000	50ms	25ms	1	1

A modification of the time base is taken into account at the end of the current period (previously set) to avoid an unwanted time shift. This allows to use this time base as a real time clock.

Bit 1 = **OIE** Oscillator interrupt enable

This bit set and cleared by software.

0: Oscillator interrupt disabled

1: Oscillator interrupt enabled

This interrupt can be used to exit from ACTIVE-HALT mode.

When this bit is set, calling the ST7 software HALT instruction enters the ACTIVE-HALT power saving mode.

10.3 PWM AUTO-RELOAD TIMER (ART)

10.3.1 Introduction

The Pulse Width Modulated Auto-Reload Timer on-chip peripheral consists of an 8-bit auto reload counter with compare/capture capabilities and of a 7-bit prescaler clock source.

These resources allow five possible operating modes:

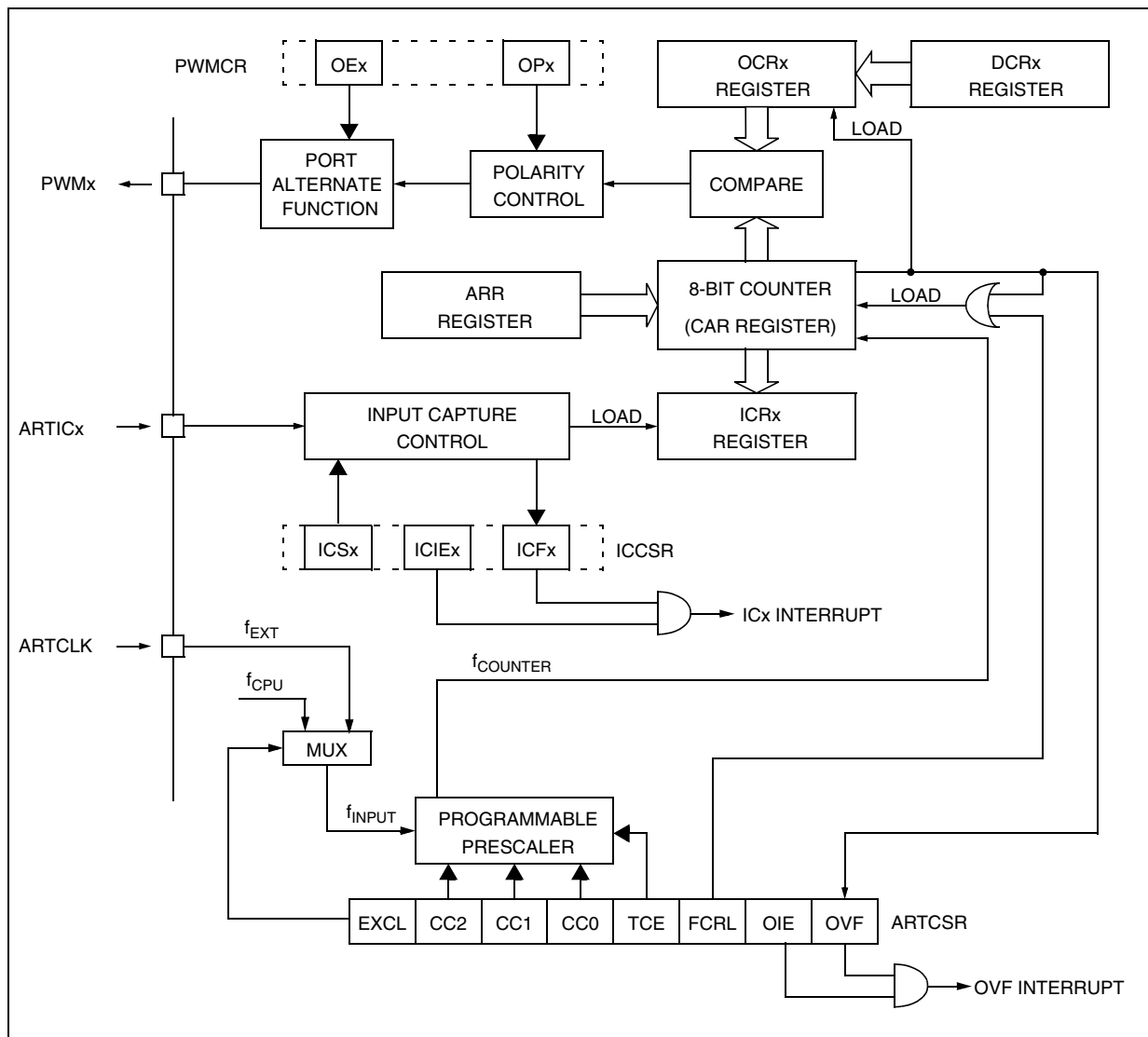
- Generation of up to 4 independent PWM signals
- Output compare and Time base interrupt

- Up to two input capture functions
- External event detector
- Up to two external interrupt sources

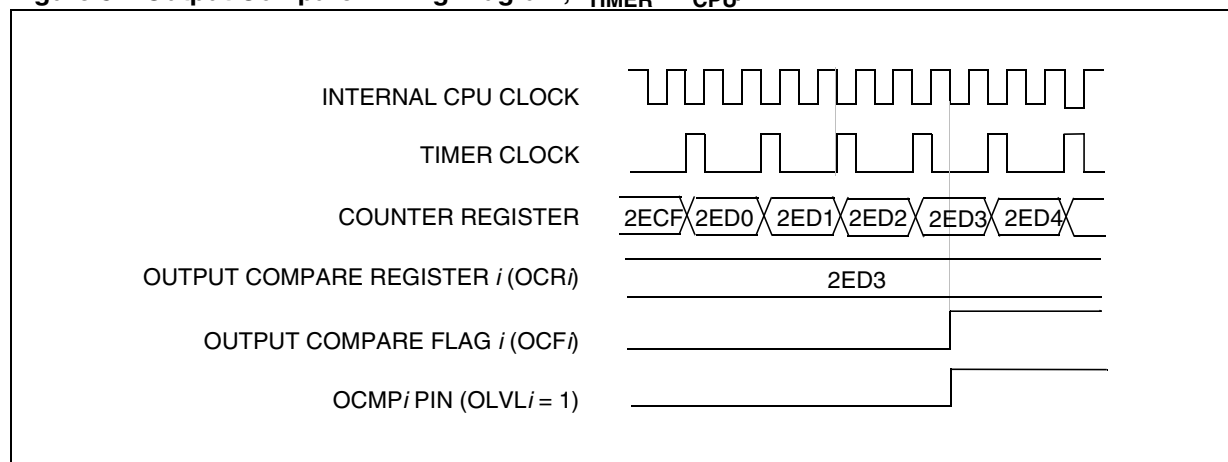
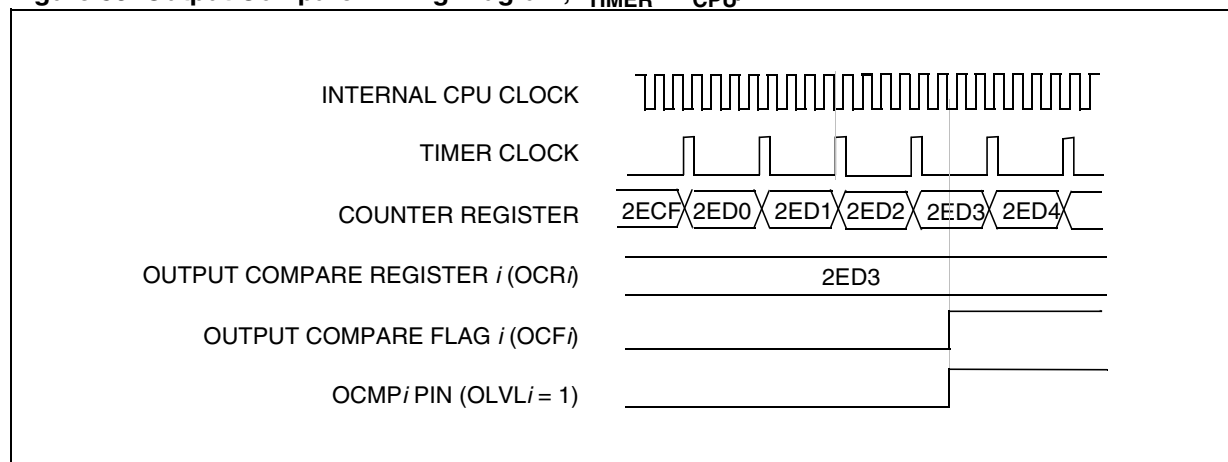
The three first modes can be used together with a single counter frequency.

The timer can be used to wake up the MCU from WAIT and HALT modes.

Figure 39. PWM Auto-Reload Timer Block Diagram



16-BIT TIMER (Cont'd)

Figure 52. Output Compare Timing Diagram, $f_{\text{TIMER}} = f_{\text{CPU}}/2$ Figure 53. Output Compare Timing Diagram, $f_{\text{TIMER}} = f_{\text{CPU}}/4$ 

16-BIT TIMER (Cont'd)**10.4.3.5 One Pulse Mode**

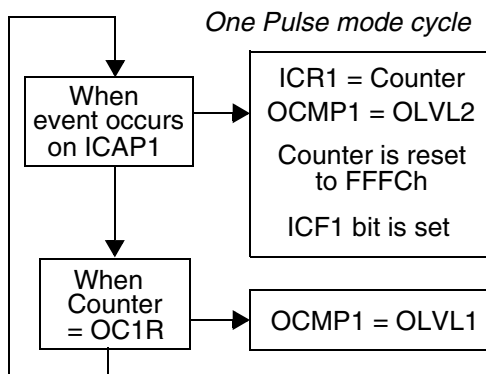
One Pulse mode enables the generation of a pulse when an external event occurs. This mode is selected via the OPM bit in the CR2 register.

The One Pulse mode uses the Input Capture1 function and the Output Compare1 function.

Procedure:

To use One Pulse mode:

1. Load the OC1R register with the value corresponding to the length of the pulse (see the formula in the opposite column).
2. Select the following in the CR1 register:
 - Using the OLVL1 bit, select the level to be applied to the OCMP1 pin after the pulse.
 - Using the OLVL2 bit, select the level to be applied to the OCMP1 pin during the pulse.
 - Select the edge of the active transition on the ICAP1 pin with the IEDG1 bit (the ICAP1 pin must be configured as floating input).
3. Select the following in the CR2 register:
 - Set the OC1E bit, the OCMP1 pin is then dedicated to the Output Compare 1 function.
 - Set the OPM bit.
 - Select the timer clock CC[1:0] (see Table 1).



Then, on a valid event on the ICAP1 pin, the counter is initialized to FFFCh and OLVL2 bit is loaded on the OCMP1 pin, the ICF1 bit is set and the value FFFDh is loaded in the IC1R register.

Because the ICF1 bit is set when an active edge occurs, an interrupt can be generated if the ICIE bit is set.

Clearing the Input Capture interrupt request (that is, clearing the ICF1 bit) is done in two steps:

1. Reading the SR register while the ICF1 bit is set.
2. An access (read or write) to the IC1LR register.

The OC1R register value required for a specific timing application can be calculated using the following formula:

$$\text{OC1R Value} = \frac{t \cdot f_{\text{CPU}}}{\text{PRESC}} - 5$$

Where:

t = Pulse period (in seconds)

f_{CPU} = CPU clock frequency (in hertz)

PRESC = Timer prescaler factor (2, 4 or 8 depending on the CC[1:0] bits, see Table 1)

If the timer clock is an external clock the formula is:

$$\text{OC1R} = t \cdot f_{\text{EXT}} - 5$$

Where:

t = Pulse period (in seconds)

f_{EXT} = External timer clock frequency (in hertz)

When the value of the counter is equal to the value of the contents of the OC1R register, the OLVL1 bit is output on the OCMP1 pin, (See Figure 10).

Notes:

1. The OCF1 bit cannot be set by hardware in One Pulse mode but the OCF2 bit can generate an Output Compare interrupt.
2. When the Pulse Width Modulation (PWM) and One Pulse mode (OPM) bits are both set, the PWM mode is the only active one.
3. If OLVL1 = OLVL2 a continuous signal will be seen on the OCMP1 pin.
4. The ICAP1 pin can not be used to perform input capture. The ICAP2 pin can be used to perform input capture (ICF2 can be set and IC2R can be loaded) but the user must take care that the counter is reset each time a valid edge occurs on the ICAP1 pin and ICF1 can also generates interrupt if ICIE is set.
5. When One Pulse mode is used OC1R is dedicated to this mode. Nevertheless OC2R and OCF2 can be used to indicate a period of time has been elapsed but cannot generate an output waveform because the level OLVL2 is dedicated to the One Pulse mode.

16-BIT TIMER (Cont'd)**CONTROL REGISTER 2 (CR2)**

Read/Write

Reset Value: 0000 0000 (00h)

7							0
OC1E	OC2E	OPM	PWM	CC1	CC0	IEDG2	EXEDG

Bit 7 = **OC1E** *Output Compare 1 Pin Enable*.

This bit is used only to output the signal from the timer on the OCMP1 pin (OLV1 in Output Compare mode, both OLV1 and OLV2 in PWM and one-pulse mode). Whatever the value of the OC1E bit, the Output Compare 1 function of the timer remains active.

0: OCMP1 pin alternate function disabled (I/O pin free for general-purpose I/O).

1: OCMP1 pin alternate function enabled.

Bit 6 = **OC2E** *Output Compare 2 Pin Enable*.

This bit is used only to output the signal from the timer on the OCMP2 pin (OLV2 in Output Compare mode). Whatever the value of the OC2E bit, the Output Compare 2 function of the timer remains active.

0: OCMP2 pin alternate function disabled (I/O pin free for general-purpose I/O).

1: OCMP2 pin alternate function enabled.

Bit 5 = **OPM** *One Pulse Mode*.

0: One Pulse mode is not active.

1: One Pulse mode is active, the ICAP1 pin can be used to trigger one pulse on the OCMP1 pin; the active transition is given by the IEDG1 bit. The length of the generated pulse depends on the contents of the OC1R register.

Bit 4 = **PWM** *Pulse Width Modulation*.

0: PWM mode is not active.

1: PWM mode is active, the OCMP1 pin outputs a programmable cyclic signal; the length of the pulse depends on the value of OC1R register; the period depends on the value of OC2R register.

Bit 3, 2 = **CC[1:0]** *Clock Control*.

The timer clock mode depends on these bits:

Table 18. Clock Control Bits

Timer Clock	CC1	CC0
$f_{CPU} / 4$	0	0
$f_{CPU} / 2$		1
$f_{CPU} / 8$	1	0
External Clock (where available)		1

Note: If the external clock pin is not available, programming the external clock configuration stops the counter.

Bit 1 = **IEDG2** *Input Edge 2*.

This bit determines which type of level transition on the ICAP2 pin will trigger the capture.

0: A falling edge triggers the capture.

1: A rising edge triggers the capture.

Bit 0 = **EXEDG** *External Clock Edge*.

This bit determines which type of level transition on the external clock pin EXTCLK will trigger the counter register.

0: A falling edge triggers the counter register.

1: A rising edge triggers the counter register.

SERIAL PERIPHERAL INTERFACE (Cont'd)**Table 21. SPI Register Map and Reset Values**

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0021h	SPIDR Reset Value	MSB x	x	x	x	x	x	x	LSB x
0022h	SPICR Reset Value	SPIE 0	SPE 0	SPR2 0	MSTR 0	CPOL x	CPHA x	SPR1 x	SPR0 x
0023h	SPICSR Reset Value	SPIF 0	WCOL 0	OVR 0	MODF 0	0	SOD 0	SSM 0	SSI 0

10.7 I²C BUS INTERFACE (I2C)

10.7.1 Introduction

The I²C Bus Interface serves as an interface between the microcontroller and the serial I²C bus. It provides both multimaster and slave functions, and controls all I²C bus-specific sequencing, protocol, arbitration and timing. It supports fast I²C mode (400kHz).

10.7.2 Main Features

- Parallel-bus/I²C protocol converter
- Multi-master capability
- 7-bit/10-bit Addressing
- SMBus V1.1 Compliant
- Transmitter/Receiver flag
- End-of-byte transmission flag
- Transfer problem detection

I²C Master Features:

- Clock generation
- I²C bus busy flag
- Arbitration Lost Flag
- End of byte transmission flag
- Transmitter/Receiver Flag
- Start bit detection flag
- Start and Stop generation

I²C Slave Features:

- Stop bit detection
- I²C bus busy flag
- Detection of misplaced start or stop condition
- Programmable I²C Address detection
- Transfer problem detection
- End-of-byte transmission flag
- Transmitter/Receiver flag

10.7.3 General Description

In addition to receiving and transmitting data, this interface converts it from serial to parallel format

and vice versa, using either an interrupt or polled handshake. The interrupts are enabled or disabled by software. The interface is connected to the I²C bus by a data pin (SDAI) and by a clock pin (SCLI). It can be connected both with a standard I²C bus and a Fast I²C bus. This selection is made by software.

Mode Selection

The interface can operate in the four following modes:

- Slave transmitter/receiver
- Master transmitter/receiver

By default, it operates in slave mode.

The interface automatically switches from slave to master after it generates a START condition and from master to slave in case of arbitration loss or a STOP generation, allowing then Multi-Master capability.

Communication Flow

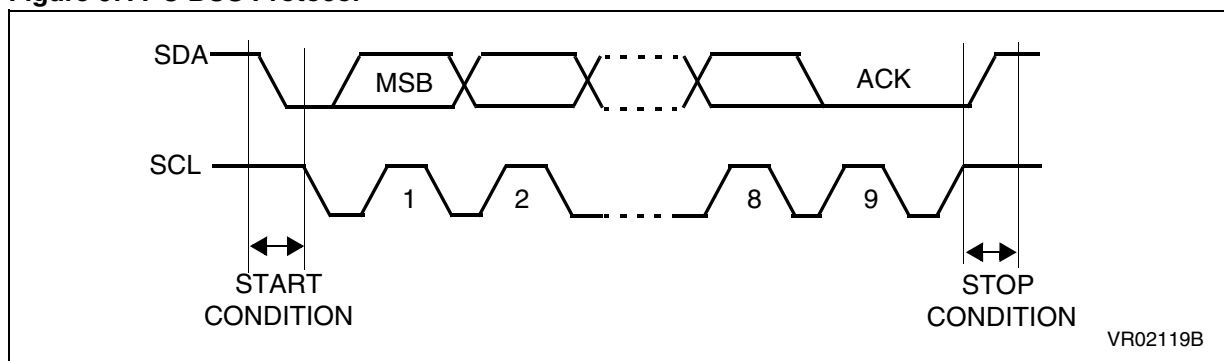
In Master mode, it initiates a data transfer and generates the clock signal. A serial data transfer always begins with a start condition and ends with a stop condition. Both start and stop conditions are generated in master mode by software.

In Slave mode, the interface is capable of recognising its own address (7 or 10-bit), and the General Call address. The General Call address detection may be enabled or disabled by software.

Data and addresses are transferred as 8-bit bytes, MSB first. The first byte(s) following the start condition contain the address (one in 7-bit mode, two in 10-bit mode). The address is always transmitted in Master mode.

A 9th clock pulse follows the 8 clock cycles of a byte transfer, during which the receiver must send an acknowledge bit to the transmitter. Refer to Figure 67.

Figure 67. I²C BUS Protocol



I²C BUS INTERFACE (Cont'd)**10.7.7 Register Description****I²C CONTROL REGISTER (CR)**

Read / Write

Reset Value: 0000 0000 (00h)

7							0
0	0	PE	ENGCG	START	ACK	STOP	ITE

Bit 7:6 = Reserved. Forced to 0 by hardware.

Bit 5 = **PE** *Peripheral enable*.

This bit is set and cleared by software.

0: Peripheral disabled

1: Master/Slave capability

Notes:

- When PE=0, all the bits of the CR register and the SR register except the Stop bit are reset. All outputs are released while PE=0
- When PE=1, the corresponding I/O pins are selected by hardware as alternate functions.
- To enable the I²C interface, write the CR register **TWICE** with PE=1 as the first write only activates the interface (only PE is set).

Bit 4 = **ENGCG** *Enable General Call*.

This bit is set and cleared by software. It is also cleared by hardware when the interface is disabled (PE=0). The 00h General Call address is acknowledged (01h ignored).

0: General Call disabled

1: General Call enabled

Note: In accordance with the I2C standard, when GCAL addressing is enabled, an I2C slave can only receive data. It will not transmit data to the master.

Bit 3 = **START** *Generation of a Start condition*. This bit is set and cleared by software. It is also cleared by hardware when the interface is disabled (PE=0) or when the Start condition is sent (with interrupt generation if ITE=1).

– In master mode:

0: No start generation

1: Repeated start generation

– In slave mode:

0: No start generation

1: Start generation when the bus is free

Bit 2 = **ACK** *Acknowledge enable*.

This bit is set and cleared by software. It is also cleared by hardware when the interface is disabled (PE=0).

0: No acknowledge returned

1: Acknowledge returned after an address byte or a data byte is received

Bit 1 = **STOP** *Generation of a Stop condition*.

This bit is set and cleared by software. It is also cleared by hardware in master mode. Note: This bit is not cleared when the interface is disabled (PE=0).

– In master mode:

0: No stop generation

1: Stop generation after the current byte transfer or after the current Start condition is sent. The STOP bit is cleared by hardware when the Stop condition is sent.

– In slave mode:

0: No stop generation

1: Release the SCL and SDA lines after the current byte transfer (BTF=1). In this mode the STOP bit has to be cleared by software.

Bit 0 = **ITE** *Interrupt enable*.

This bit is set and cleared by software and cleared by hardware when the interface is disabled (PE=0).

0: Interrupts disabled

1: Interrupts enabled

Refer to Figure 70 for the relationship between the events and the interrupt.

SCL is held low when the ADD10, SB, BTF or ADSL flags or an EV6 event (See Figure 69) is detected.

INSTRUCTION SET OVERVIEW (Cont'd)

11.1.1 Inherent

All Inherent instructions consist of a single byte. The opcode fully specifies all the required information for the CPU to process the operation.

Inherent Instruction	Function
NOP	No operation
TRAP	S/W Interrupt
WFI	Wait For Interrupt (Low Power Mode)
HALT	Halt Oscillator (Lowest Power Mode)
RET	Sub-routine Return
IRET	Interrupt Sub-routine Return
SIM	Set Interrupt Mask (level 3)
RIM	Reset Interrupt Mask (level 0)
SCF	Set Carry Flag
RCF	Reset Carry Flag
RSP	Reset Stack Pointer
LD	Load
CLR	Clear
PUSH/POP	Push/Pop to/from the stack
INC/DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
MUL	Byte Multiplication
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles

11.1.2 Immediate

Immediate instructions have 2 bytes, the first byte contains the opcode, the second byte contains the operand value.

Immediate Instruction	Function
LD	Load
CP	Compare
BCP	Bit Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Operations

11.1.3 Direct

In Direct instructions, the operands are referenced by their memory address.

The direct addressing mode consists of two sub-modes:

Direct (short)

The address is a byte, thus requires only one byte after the opcode, but only allows 00 - FF addressing space.

Direct (long)

The address is a word, thus allowing 64 Kbyte addressing space, but requires 2 bytes after the opcode.

11.1.4 Indexed (No Offset, Short, Long)

In this mode, the operand is referenced by its memory address, which is defined by the unsigned addition of an index register (X or Y) with an offset.

The indirect addressing mode consists of three submodes:

Indexed (No Offset)

There is no offset, (no extra byte after the opcode), and allows 00 - FF addressing space.

Indexed (Short)

The offset is a byte, thus requires only one byte after the opcode and allows 00 - 1FE addressing space.

Indexed (long)

The offset is a word, thus allowing 64 Kbyte addressing space and requires 2 bytes after the opcode.

11.1.5 Indirect (Short, Long)

The required data byte to do the operation is found by its memory address, located in memory (pointer).

The pointer address follows the opcode. The indirect addressing mode consists of two submodes:

Indirect (short)

The pointer address is a byte, the pointer size is a byte, thus allowing 00 - FF addressing space, and requires 1 byte after the opcode.

Indirect (long)

The pointer address is a word, the pointer size is a word, thus allowing 64 Kbyte addressing space, and requires 1 byte after the opcode.

OPERATING CONDITIONS (Cont'd)**12.3.2 Operating Conditions with Low Voltage Detector (LVD)**Subject to general operating conditions for V_{DD} , f_{CPU} , and T_A .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IT+(LVD)}$	Reset release threshold (V_{DD} rise)	VD level = High in option byte	4.0 ¹⁾	4.2	4.5	V
		VD level = Med. in option byte ²⁾	3.55 ¹⁾	3.75	4.0 ¹⁾	
		VD level = Low in option byte ²⁾	2.95 ¹⁾	3.15	3.35 ¹⁾	
$V_{IT-(LVD)}$	Reset generation threshold (V_{DD} fall)	VD level = High in option byte	3.8	4.0	4.25 ¹⁾	
		VD level = Med. in option byte ²⁾	3.35 ¹⁾	3.55	3.75 ¹⁾	
		VD level = Low in option byte ²⁾	2.8 ¹⁾	3.0	3.15 ¹⁾	
$V_{hys(LVD)}$	LVD voltage threshold hysteresis	$V_{IT+(LVD)} - V_{IT-(LVD)}$		200		mV
V_{tPOR}	V_{DD} rise time ³⁾	LVD enabled	6 μ s/V		100ms/V	
$t_g(V_{DD})$	V_{DD} glitches filtered (not detected) by LVD ³⁾				40	ns

Notes:

1. Data based on characterization results, tested in production for ROM devices only.
2. If the medium or low thresholds are selected, the detection may occur outside the specified operating voltage range. Below 3.8V, device operation is not guaranteed.
3. Data based on characterization results, not tested in production.

12.3.3 Auxiliary Voltage Detector (AVD) ThresholdsSubject to general operating conditions for V_{DD} , f_{CPU} , and T_A .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IT+(AVD)}$	1 \Rightarrow 0 AVDF flag toggle threshold (V_{DD} rise)	VD level = High in option byte	4.4 ¹⁾	4.6	4.9 ¹⁾	V
		VD level = Med. in option byte	3.95 ¹⁾	4.15	4.4 ¹⁾	
		VD level = Low in option byte	3.4 ¹⁾	3.6	3.8 ¹⁾	
$V_{IT-(AVD)}$	0 \Rightarrow 1 AVDF flag toggle threshold (V_{DD} fall)	VD level = High in option byte	4.2 ¹⁾	4.4	4.65 ¹⁾	
		VD level = Med. in option byte	3.75 ¹⁾	4.0	4.2 ¹⁾	
		VD level = Low in option byte	3.2 ¹⁾	3.4	3.6 ¹⁾	
$V_{hys(AVD)}$	AVD voltage threshold hysteresis	$V_{IT+(AVD)} - V_{IT-(AVD)}$		200		mV
ΔV_{IT-}	Voltage drop between AVD flag set and LVD reset activated	$V_{IT-(AVD)} - V_{IT-(LVD)}$		450		mV

1. Data based on characterization results, tested in production for ROM devices only.

12.3.4 External Voltage Detector (EVD) ThresholdsSubject to general operating conditions for V_{DD} , f_{CPU} , and T_A .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IT+(EVD)}$	1 \Rightarrow 0 AVDF flag toggle threshold (V_{DD} rise) ¹⁾		1.15	1.26	1.35	V
$V_{IT-(EVD)}$	0 \Rightarrow 1 AVDF flag toggle threshold (V_{DD} fall) ¹⁾		1.1	1.2	1.3	
$V_{hys(EVD)}$	EVD voltage threshold hysteresis	$V_{IT+(EVD)} - V_{IT-(EVD)}$		200		mV

1. Data based on characterization results, not tested in production.

12.6 MEMORY CHARACTERISTICS

12.6.1 RAM and Hardware Registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode ¹⁾	HALT mode (or RESET)	1.6			V

12.6.2 FLASH Memory

DUAL VOLTAGE HDFLASH MEMORY						
Symbol	Parameter	Conditions	Min ²⁾	Typ	Max ²⁾	Unit
f_{CPU}	Operating frequency	Read mode	0		8	MHz
		Write / Erase mode	1		8	
V_{PP}	Programming voltage ³⁾	$4.5V \leq V_{DD} \leq 5.5V$	11.4		12.6	V
I_{DD}	Supply current ⁴⁾	RUN mode ($f_{CPU} = 4MHz$)			3	mA
		Write / Erase		0		
		Power down mode / HALT		1	10	μA
I_{PP}	V_{PP} current ⁴⁾	Read ($V_{PP}=12V$)			200	μA
		Write / Erase			30	mA
t_{VPP}	Internal V_{PP} stabilization time			10		μs
t_{RET}	Data retention	$T_A=85^\circ C$	40			years
		$T_A=105^\circ C$	15			
		$T_A=125^\circ C$	7			
N_{RW}	Write erase cycles	$T_A= 55^\circ C$	1000			cycles
		$T_A= 85^\circ C$	100			cycles
T_{PROG} T_{ERASE}	Programming or erasing temperature range		-40	25	85	$^\circ C$

Notes:

1. Minimum V_{DD} supply voltage without losing data stored in RAM (in HALT mode or under RESET) or in hardware registers (only in HALT mode). Not tested in production.
2. Data based on characterization results, not tested in production.
3. V_{PP} must be applied only during the programming or erasing operation and not permanently for reliability reasons.
4. Data based on simulation results, not tested in production.

Warning: Do not connect 12V to V_{PP} before V_{DD} is powered on, as this may damage the device.

I/O PORT PIN CHARACTERISTICS (Cont'd)

12.8.2 Output Driving Current

Subject to general operating conditions for V_{DD} , f_{CPU} , and T_A unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{1)}$	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time (see Figure 81)	$I_{IO}=+5mA$		1.2	V
		$I_{IO}=+2mA$		0.5	
	Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time (see Figure 82 and Figure 84)	$I_{IO}=+20mA, T_A \leq 85^\circ C$ $T_A \geq 85^\circ C$		1.3 1.5	
		$I_{IO}=+8mA$		0.6	
$V_{OH}^{2)}$	Output high level voltage for an I/O pin when 4 pins are sourced at same time (see Figure 83 and Figure 86)	$I_{IO}=-5mA, T_A \leq 85^\circ C$ $T_A \geq 85^\circ C$	$V_{DD}-1.4$ $V_{DD}-1.6$		
		$I_{IO}=-2mA$	$V_{DD}-0.7$		

Figure 81. Typical V_{OL} at $V_{DD}=5V$ (standard)

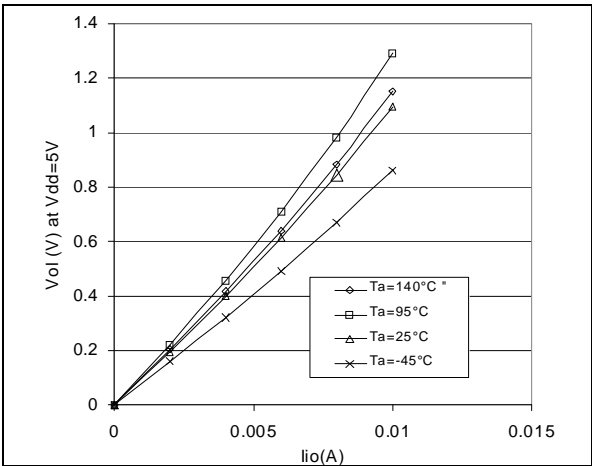


Figure 83. Typical V_{OH} at $V_{DD}=5V$

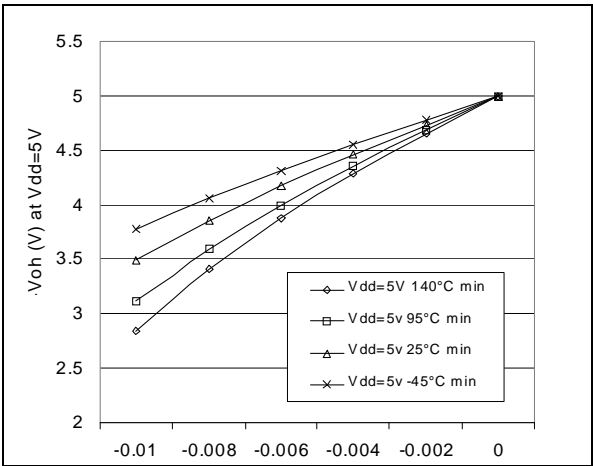
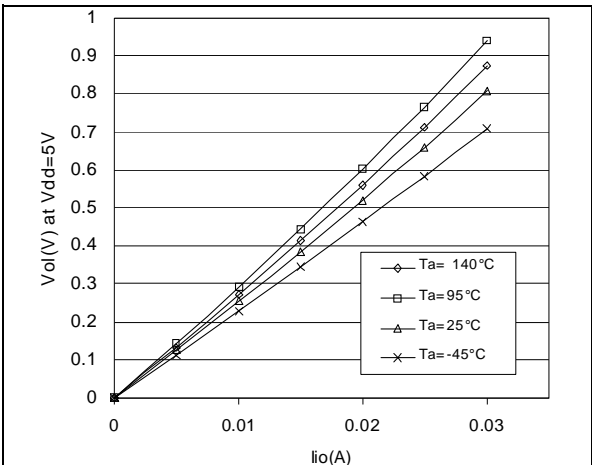


Figure 82. Typical V_{OL} at $V_{DD}=5V$ (high-sink)



Notes:

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in Section 12.2.2 and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in Section 12.2.2 and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} . True open drain I/O pins do not have V_{OH} .

10-BIT ADC CHARACTERISTICS (Cont'd)

12.12.3 ADC Accuracy

Conditions: $V_{DD}=5V$ ¹⁾

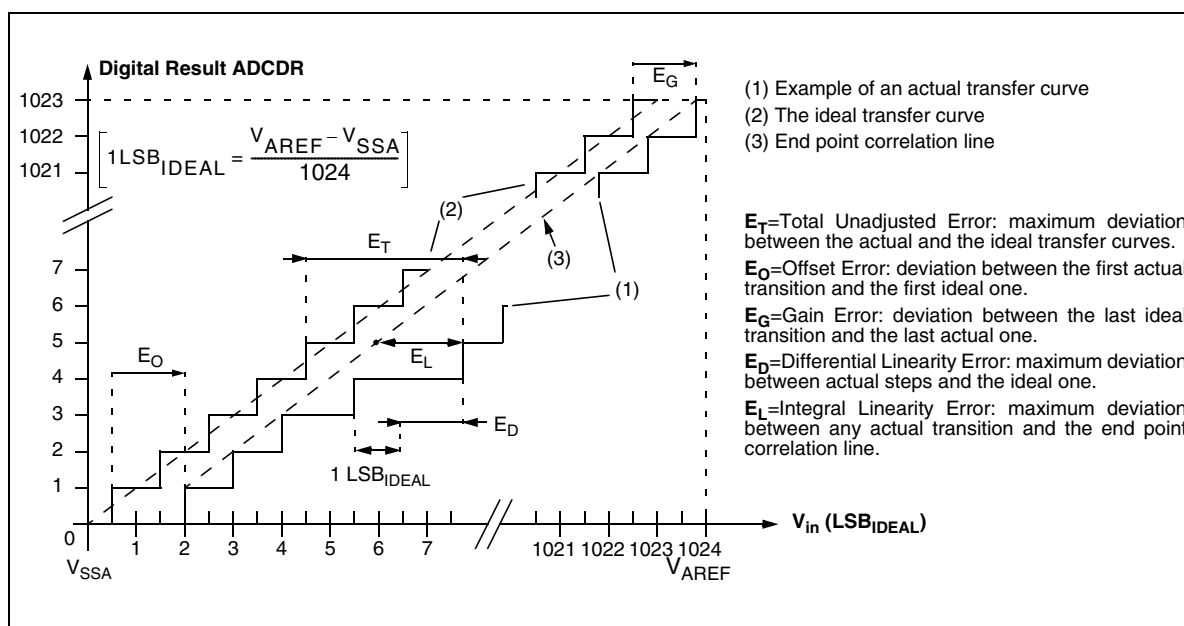
Symbol	Parameter	Conditions	Typ	Max ²⁾	Unit
$ E_T $	Total unadjusted error ¹⁾		3	4	LSB
$ E_O $	Offset error ¹⁾		2	3	
$ E_G $	Gain Error ¹⁾		0.5	3	
$ E_D $	Differential linearity error ¹⁾	CPU in run mode @ f_{ADC} 2 MHz.	1	2	
$ E_L $	Integral linearity error ¹⁾	CPU in run mode @ f_{ADC} 2 MHz.	1	2	

Notes:

1. ADC Accuracy vs. Negative Injection Current: Injecting negative current may reduce the accuracy of the conversion being performed on another analog input.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 12.8 does not affect the ADC accuracy.

2. Data based on characterization results, monitored in production to guarantee 99.73% within \pm max value from -40°C to 125°C ($\pm 3\sigma$ distribution limits).

Figure 98. ADC Accuracy Characteristics

13.2 THERMAL CHARACTERISTICS

Symbol	Ratings	Value	Unit
R_{thJA}	Package thermal resistance (junction to ambient)		
	LQFP64 10x10	50	°C/W
	LQFP48 7x7	80	
	LQFP44 10x10	52	
	SDIP42	55	
	LQFP32 7x7	70	
	SDIP32	50	
P_D	Power dissipation ¹⁾	500	mW
T_{Jmax}	Maximum junction temperature ²⁾	150	°C

Notes:

1. The maximum chip-junction temperature is based on technology characteristics.

2. The maximum power dissipation is obtained from the formula $P_D = (T_J - T_A) / R_{thJA}$.

The power dissipation of an application can be defined by the user with the formula: $P_D = P_{INT} + P_{PORT}$ where P_{INT} is the chip internal power ($I_{DD} \times V_{DD}$) and P_{PORT} is the port power dissipation depending on the ports used in the application.