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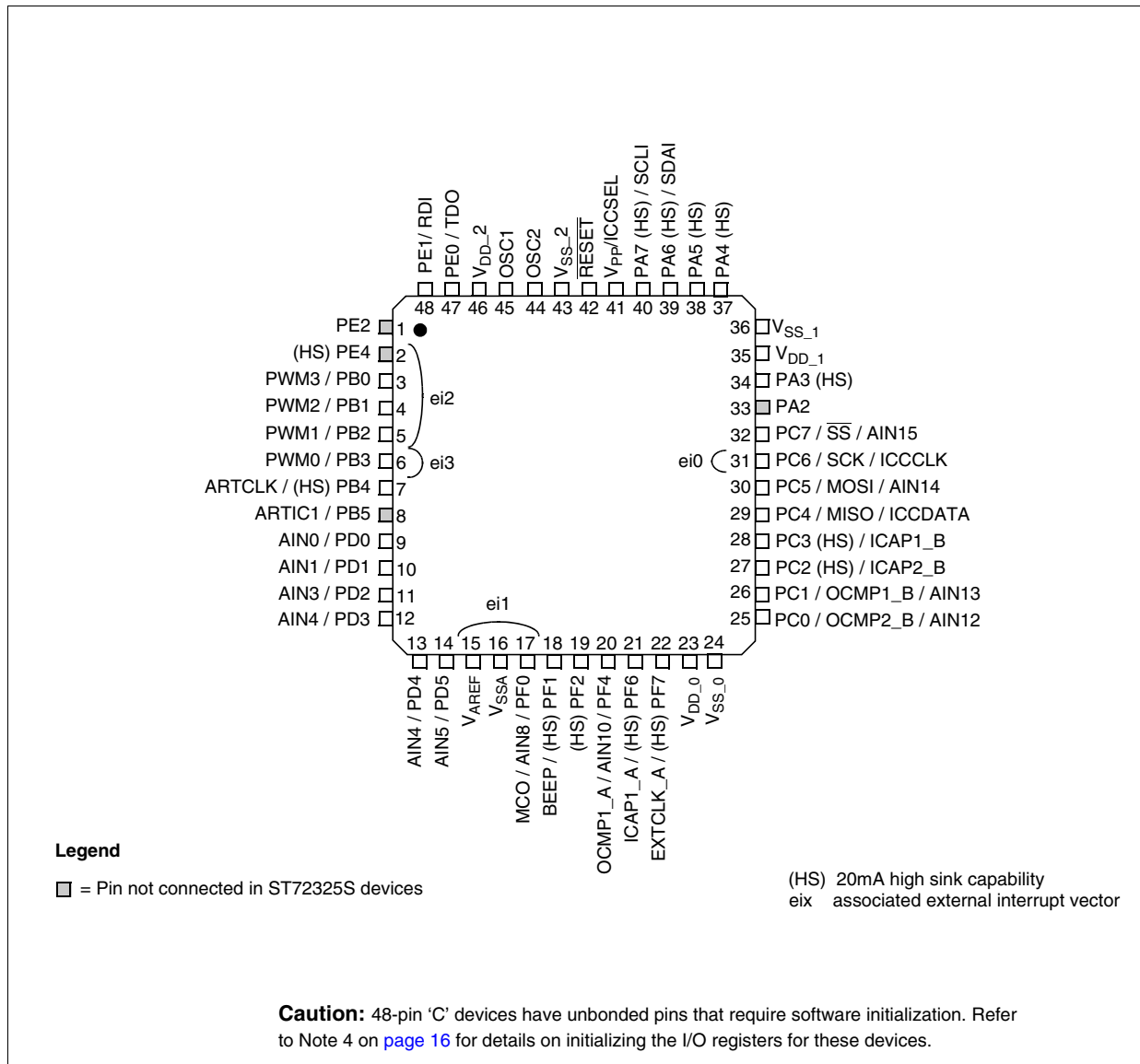
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	I <sup>2</sup> C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	32
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/st72f325j7t6">https://www.e-xfl.com/product-detail/stmicroelectronics/st72f325j7t6</a>

Figure 3. 48-Pin LQFP 7x7 Device Pinout



Address	Block	Register Label	Register Name	Reset Status	Remarks
002Ch 002Dh	MCC	MCCSR MCCBCR	Main Clock Control / Status Register Main Clock Controller: Beep Control Register	00h 00h	R/W R/W
002Eh to 0030h	Reserved Area (3 Bytes)				
0031h 0032h 0033h 0034h 0035h 0036h 0037h 0038h 0039h 003Ah 003Bh 003Ch 003Dh 003Eh 003Fh	TIMER A	TACR2 TACR1 TACSR TAIC1HR TAIC1LR TAOC1HR TAOC1LR TACHR TACL TAACHR TAACL TAIC2HR TAIC2LR TAOC2HR TAOC2LR	Timer A Control Register 2 Timer A Control Register 1 Timer A Control/Status Register Timer A Input Capture 1 High Register Timer A Input Capture 1 Low Register Timer A Output Compare 1 High Register Timer A Output Compare 1 Low Register Timer A Counter High Register Timer A Counter Low Register Timer A Alternate Counter High Register Timer A Alternate Counter Low Register Timer A Input Capture 2 High Register Timer A Input Capture 2 Low Register Timer A Output Compare 2 High Register Timer A Output Compare 2 Low Register	00h 00h xxxx x0xx b xxh xxh 80h 00h FFh FCh FFh FCh xxh xxh 80h 00h	R/W R/W R/W Read Only Read Only R/W R/W Read Only Read Only Read Only Read Only Read Only Read Only R/W R/W
0040h	Reserved Area (1 Byte)				
0041h 0042h 0043h 0044h 0045h 0046h 0047h 0048h 0049h 004Ah 004Bh 004Ch 004Dh 004Eh 004Fh	TIMER B	TBCR2 TBCR1 TBCSR TBIC1HR TBIC1LR TBOC1HR TBOC1LR TBCHR TBCLR TBACHR TBACL TBIC2HR TBIC2LR TBOC2HR TBOC2LR	Timer B Control Register 2 Timer B Control Register 1 Timer B Control/Status Register Timer B Input Capture 1 High Register Timer B Input Capture 1 Low Register Timer B Output Compare 1 High Register Timer B Output Compare 1 Low Register Timer B Counter High Register Timer B Counter Low Register Timer B Alternate Counter High Register Timer B Alternate Counter Low Register Timer B Input Capture 2 High Register Timer B Input Capture 2 Low Register Timer B Output Compare 2 High Register Timer B Output Compare 2 Low Register	00h 00h xxxx x0xx b xxh xxh 80h 00h FFh FCh FFh FCh xxh xxh 80h 00h	R/W R/W R/W Read Only Read Only R/W R/W Read Only Read Only Read Only Read Only Read Only Read Only R/W R/W
0050h 0051h 0052h 0053h 0054h 0055h 0056h 0057h	SCI	SCISR SCIDR SCIBRR SCICR1 SCICR2 SCIERP SCIETPR	SCI Status Register SCI Data Register SCI Baud Rate Register SCI Control Register 1 SCI Control Register 2 SCI Extended Receive Prescaler Register Reserved area SCI Extended Transmit Prescaler Register	C0h xxh 00h x000 0000b 00h 00h ---	Read Only R/W R/W R/W R/W R/W ---

**SYSTEM INTEGRITY MANAGEMENT (Cont'd)**

**6.4.3 Clock Security System (CSS)**

The Clock Security System (CSS) protects the ST7 against breakdowns, spikes and overfrequencies occurring on the main clock source ( $f_{OSC}$ ). It is based on a clock filter and a clock detection control with an internal safe oscillator ( $f_{SFOSC}$ ).

**6.4.3.1 Clock Filter Control**

The PLL has an integrated glitch filtering capability making it possible to protect the internal clock from overfrequencies created by individual spikes. This feature is available only when the PLL is enabled. If glitches occur on  $f_{OSC}$  (for example, due to loose connection or noise), the CSS filters these automatically, so the internal CPU frequency ( $f_{CPU}$ ) continues deliver a glitch-free signal (see Figure 20).

**6.4.3.2 Clock detection Control**

If the clock signal disappears (due to a broken or disconnected resonator...), the safe oscillator delivers a low frequency clock signal ( $f_{SFOSC}$ ) which allows the ST7 to perform some rescue operations.

Automatically, the ST7 clock source switches back from the safe oscillator ( $f_{SFOSC}$ ) if the main clock source ( $f_{OSC}$ ) recovers.

When the internal clock ( $f_{CPU}$ ) is driven by the safe oscillator ( $f_{SFOSC}$ ), the application software is notified by hardware setting the CSSD bit in the SICSR register. An interrupt can be generated if the

CSSIE bit has been previously set. These two bits are described in the SICSR register description.

**6.4.4 Low Power Modes**

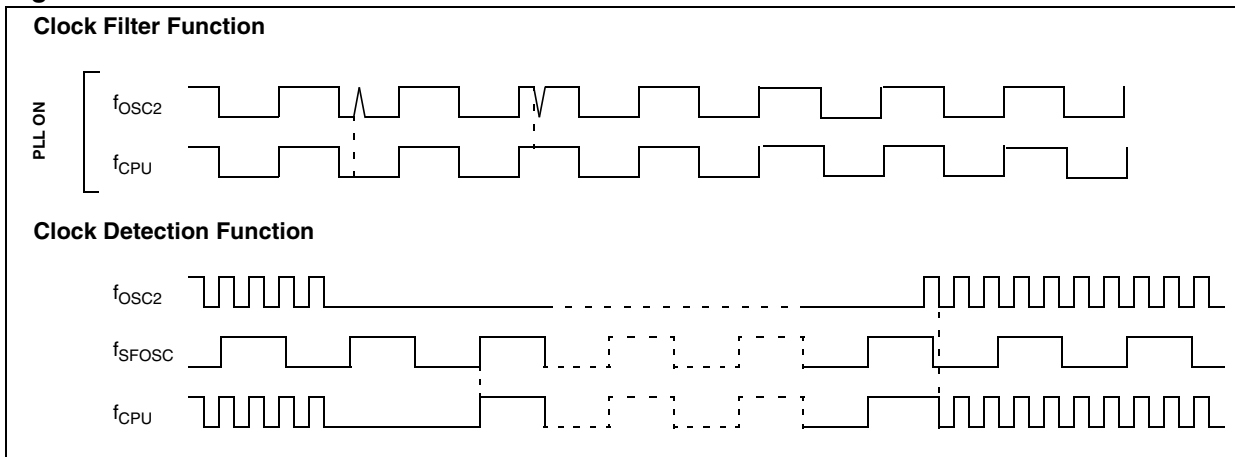
Mode	Description
WAIT	No effect on SI. CSS and AVD interrupts cause the device to exit from Wait mode.
HALT	The SICSR register is frozen. The CSS (including the safe oscillator) is disabled until HALT mode is exited. The previous CSS configuration resumes when the MCU is woken up by an interrupt with "exit from HALT mode" capability or from the counter reset value when the MCU is woken up by a RESET.

**6.4.4.1 Interrupts**

The CSS orAVD interrupt events generate an interrupt if the corresponding Enable Control Bit (CSSIE or AVDIE) is set and the interrupt mask in the CC register is reset (RIM instruction).

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
CSS event detection (safe oscillator activated as main clock)	CSSD	CSSIE	Yes	No
AVD event	AVDF	AVDIE	Yes	No

**Figure 20. Clock Filter Function**



## INTERRUPTS (Cont'd)

Table 9. Interrupt Mapping

N°	Source Block	Description	Register Label	Priority Order	Exit from HALT/ACTIVE HALT	Address Vector
	RESET	Reset	N/A		yes	FFFEh-FFFFh
	TRAP	Software interrupt			no	FFFCh-FFFDh
0	TLI	External top level interrupt	EICR		yes	FFFAh-FFFBh
1	MCC/RTC/CSS	Main clock controller time base interrupt Safe oscillator activation interrupt	MCCSR-SICSR	Higher Priority  ↓  Lower Priority	yes	FFF8h-FFF9h
2	ei0	External interrupt port A3..0	N/A		yes	FFF6h-FFF7h
3	ei1	External interrupt port F2..0			yes	FFF4h-FFF5h
4	ei2	External interrupt port B3..0			yes	FFF2h-FFF3h
5	ei3	External interrupt port B7..4			yes	FFF0h-FFF1h
6	Not used					FFEEh-FFEFh
7	SPI	SPI peripheral interrupts	SPICSR	yes <sup>1</sup>	FFEC h-FFEDh	
8	TIMER A	TIMER A peripheral interrupts	TASR	no	FFEAh-FFEBh	
9	TIMER B	TIMER B peripheral interrupts	TBSR	no	FFE8h-FFE9h	
10	SCI	SCI Peripheral interrupts	SCISR	no	FFE6h-FFE7h	
11	AVD	Auxiliary Voltage detector interrupt	SICSR	no	FFE4h-FFE5h	
12	I2C	I2C Peripheral interrupts	(see periph)	no	FFE2h-FFE3h	
13	PWM ART	PWM ART interrupt	ARTCSR	yes <sup>2</sup>	FFE0h-FFE1h	

## Notes:

- Exit from HALT possible when SPI is in slave mode.
- Exit from HALT possible when PWM ART is in external clock mode.

## 7.6 EXTERNAL INTERRUPTS

## 7.6.1 I/O Port Interrupt Sensitivity

The external interrupt sensitivity is controlled by the IPA, IPB and ISxx bits of the EICR register (Figure 25). This control allows to have up to 4 fully independent external interrupt source sensitivities.

Each external interrupt source can be generated on four (or five) different events on the pin:

- Falling edge
- Rising edge
- Falling and rising edge

- Falling edge and low level
- Rising edge and high level (only for ei0 and ei2)

To guarantee correct functionality, the sensitivity bits in the EICR register can be modified only when the I1 and I0 bits of the CC register are both set to 1 (level 3). This means that interrupts must be disabled before changing sensitivity.

The pending interrupts are cleared by writing a different value in the ISx[1:0], IPA or IPB bits of the EICR.

## 9 I/O PORTS

### 9.1 INTRODUCTION

The I/O ports offer different functional modes:

- transfer of data through digital inputs and outputs and for specific pins:
- external interrupt generation
- alternate signal input/output for the on-chip peripherals.

An I/O port contains up to 8 pins. Each pin can be programmed independently as digital input (with or without interrupt generation) or digital output.

### 9.2 FUNCTIONAL DESCRIPTION

Each port has two main registers:

- Data Register (DR)
- Data Direction Register (DDR)

and one optional register:

- Option Register (OR)

Each I/O pin may be programmed using the corresponding register bits in the DDR and OR registers: Bit X corresponding to pin X of the port. The same correspondence is used for the DR register.

The following description takes into account the OR register, (for specific ports which do not provide this register refer to the I/O Port Implementation section). The generic I/O block diagram is shown in [Figure 1](#)

#### 9.2.1 Input Modes

The input configuration is selected by clearing the corresponding DDR register bit.

In this case, reading the DR register returns the digital value applied to the external I/O pin.

Different input modes can be selected by software through the OR register.

#### Notes:

1. Writing the DR register modifies the latch value but does not affect the pin status.
2. When switching from input to output mode, the DR register has to be written first to drive the correct level on the pin as soon as the port is configured as an output.
3. Do not use read/modify/write instructions (BSET or BRES) to modify the DR register as this might corrupt the DR content for I/Os configured as input.

#### External interrupt function

When an I/O is configured as Input with Interrupt, an event on this I/O can generate an external interrupt request to the CPU.

Each pin can independently generate an interrupt request. The interrupt sensitivity is independently programmable using the sensitivity bits in the EICR register.

Each external interrupt vector is linked to a dedicated group of I/O port pins (see pinout description and interrupt section). If several input pins are selected simultaneously as interrupt sources, these are first detected according to the sensitivity bits in the EICR register and then logically ORed.

The external interrupts are hardware interrupts, which means that the request latch (not accessible directly by the application) is automatically cleared when the corresponding interrupt vector is fetched. To clear an unwanted pending interrupt by software, the sensitivity bits in the EICR register must be modified.

#### 9.2.2 Output Modes

The output configuration is selected by setting the corresponding DDR register bit. In this case, writing the DR register applies this digital value to the I/O pin through the latch. Then reading the DR register returns the previously stored value.

Two different output modes can be selected by software through the OR register: Output push-pull and open-drain.

DR register value and output pin status:

DR	Push-pull	Open-drain
0	V <sub>SS</sub>	V <sub>SS</sub>
1	V <sub>DD</sub>	Floating

#### 9.2.3 Alternate Functions

When an on-chip peripheral is configured to use a pin, the alternate function is automatically selected. This alternate function takes priority over the standard I/O programming.

When the signal is coming from an on-chip peripheral, the I/O pin is automatically configured in output mode (push-pull or open drain according to the peripheral).

When the signal is going to an on-chip peripheral, the I/O pin must be configured in input mode. In this case, the pin state is also digitally readable by addressing the DR register.

**Note:** Input pull-up configuration can cause unexpected value at the input of the alternate peripheral input. When an on-chip peripheral use a pin as input and output, this pin has to be configured in input floating mode.

**MAIN CLOCK CONTROLLER WITH REAL TIME CLOCK (Cont'd)**

**10.2.5 Low Power Modes**

Mode	Description
WAIT	No effect on MCC/RTC peripheral. MCC/RTC interrupt cause the device to exit from WAIT mode.
ACTIVE-HALT	No effect on MCC/RTC counter (OIE bit is set), the registers are frozen. MCC/RTC interrupt cause the device to exit from ACTIVE-HALT mode.
HALT	MCC/RTC counter and registers are frozen. MCC/RTC operation resumes when the MCU is woken up by an interrupt with "exit from HALT" capability.

**10.2.6 Interrupts**

The MCC/RTC interrupt event generates an interrupt if the OIE bit of the MCCR register is set and the interrupt mask in the CC register is not active (RIM instruction).

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
Time base overflow event	OIF	OIE	Yes	No <sup>1)</sup>

**Note:**

The MCC/RTC interrupt wakes up the MCU from ACTIVE-HALT mode, not from HALT mode.

**10.2.7 Register Description**

**MCC CONTROL/STATUS REGISTER (MCCR)**

Read/Write

Reset Value: 0000 0000 (00h)

7 0

MCO	CP1	CP0	SMS	TB1	TB0	OIE	OIF
-----	-----	-----	-----	-----	-----	-----	-----

**Bit 7 = MCO Main clock out selection**

This bit enables the MCO alternate function on the PF0 I/O port. It is set and cleared by software.

0: MCO alternate function disabled (I/O pin free for general-purpose I/O)

1: MCO alternate function enabled ( $f_{CPU}$  on I/O port)

**Note:** To reduce power consumption, the MCO function is not active in ACTIVE-HALT mode.

**Bit 6:5 = CP[1:0] CPU clock prescaler**

These bits select the CPU clock prescaler which is applied in the different slow modes. Their action is conditioned by the setting of the SMS bit. These two bits are set and cleared by software

$f_{CPU}$ in SLOW mode	CP1	CP0
$f_{OSC2} / 2$	0	0
$f_{OSC2} / 4$	0	1
$f_{OSC2} / 8$	1	0
$f_{OSC2} / 16$	1	1

**Bit 4 = SMS Slow mode select**

This bit is set and cleared by software.

0: Normal mode.  $f_{CPU} = f_{OSC2}$

1: Slow mode.  $f_{CPU}$  is given by CP1, CP0

See [Section 8.2 SLOW MODE](#) and [Section 10.2 MAIN CLOCK CONTROLLER WITH REAL TIME CLOCK AND BEEPER \(MCC/RTC\)](#) for more details.

**Bit 3:2 = TB[1:0] Time base control**

These bits select the programmable divider time base. They are set and cleared by software.

Counter Prescaler	Time Base		TB1	TB0
	$f_{OSC2}=4MHz$	$f_{OSC2}=8MHz$		
16000	4ms	2ms	0	0
32000	8ms	4ms	0	1
80000	20ms	10ms	1	0
200000	50ms	25ms	1	1

A modification of the time base is taken into account at the end of the current period (previously set) to avoid an unwanted time shift. This allows to use this time base as a real time clock.

**Bit 1 = OIE Oscillator interrupt enable**

This bit set and cleared by software.

0: Oscillator interrupt disabled

1: Oscillator interrupt enabled

This interrupt can be used to exit from ACTIVE-HALT mode.

When this bit is set, calling the ST7 software HALT instruction enters the ACTIVE-HALT power saving mode.

**ON-CHIP PERIPHERALS (Cont'd)**

**PWM CONTROL REGISTER (PWMCr)**

Read/Write

Reset Value: 0000 0000 (00h)

7							0
OE3	OE2	OE1	OE0	OP3	OP2	OP1	OP0

Bit 7:4 = **OE[3:0]** *PWM Output Enable*  
 These bits are set and cleared by software. They enable or disable the PWM output channels independently acting on the corresponding I/O pin.  
 0: PWM output disabled.  
 1: PWM output enabled.

Bit 3:0 = **OP[3:0]** *PWM Output Polarity*  
 These bits are set and cleared by software. They independently select the polarity of the four PWM output signals.

PWMx output level		OPx
Counter <= OCRx	Counter > OCRx	
1	0	0
0	1	1

**Note:** When an OPx bit is modified, the PWMx output signal polarity is immediately reversed.

**DUTY CYCLE REGISTERS (PWMDCr<sub>x</sub>)**

Read/Write

Reset Value: 0000 0000 (00h)

7							0
DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0

Bit 7:0 = **DC[7:0]** *Duty Cycle Data*  
 These bits are set and cleared by software.  
 A PWMDCr<sub>x</sub> register is associated with the OCR<sub>x</sub> register of each PWM channel to determine the second edge location of the PWM signal (the first edge location is common to all channels and given by the ARTARR register). These PWMDCr registers allow the duty cycle to be set independently for each PWM channel.



**16-BIT TIMER (Cont'd)****CONTROL REGISTER 2 (CR2)**

Read/Write

Reset Value: 0000 0000 (00h)

7							0
OC1E	OC2E	OPM	PWM	CC1	CC0	IEDG2	EXEDG

**Bit 7 = OC1E Output Compare 1 Pin Enable.**

This bit is used only to output the signal from the timer on the OCMP1 pin (OLV1 in Output Compare mode, both OLV1 and OLV2 in PWM and one-pulse mode). Whatever the value of the OC1E bit, the Output Compare 1 function of the timer remains active.

0: OCMP1 pin alternate function disabled (I/O pin free for general-purpose I/O).

1: OCMP1 pin alternate function enabled.

**Bit 6 = OC2E Output Compare 2 Pin Enable.**

This bit is used only to output the signal from the timer on the OCMP2 pin (OLV2 in Output Compare mode). Whatever the value of the OC2E bit, the Output Compare 2 function of the timer remains active.

0: OCMP2 pin alternate function disabled (I/O pin free for general-purpose I/O).

1: OCMP2 pin alternate function enabled.

**Bit 5 = OPM One Pulse Mode.**

0: One Pulse mode is not active.

1: One Pulse mode is active, the ICAP1 pin can be used to trigger one pulse on the OCMP1 pin; the active transition is given by the IEDG1 bit. The length of the generated pulse depends on the contents of the OC1R register.

**Bit 4 = PWM Pulse Width Modulation.**

0: PWM mode is not active.

1: PWM mode is active, the OCMP1 pin outputs a programmable cyclic signal; the length of the pulse depends on the value of OC1R register; the period depends on the value of OC2R register.

**Bit 3, 2 = CC[1:0] Clock Control.**

The timer clock mode depends on these bits:

**Table 18. Clock Control Bits**

Timer Clock	CC1	CC0
$f_{CPU} / 4$	0	0
$f_{CPU} / 2$		1
$f_{CPU} / 8$	1	0
External Clock (where available)		1

**Note:** If the external clock pin is not available, programming the external clock configuration stops the counter.

**Bit 1 = IEDG2 Input Edge 2.**

This bit determines which type of level transition on the ICAP2 pin will trigger the capture.

0: A falling edge triggers the capture.

1: A rising edge triggers the capture.

**Bit 0 = EXEDG External Clock Edge.**

This bit determines which type of level transition on the external clock pin EXTCLK will trigger the counter register.

0: A falling edge triggers the counter register.

1: A rising edge triggers the counter register.

## 16-BIT TIMER (Cont'd)

Table 19. 16-Bit Timer Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
Timer A: 32 Timer B: 42	<b>CR1</b> Reset Value	ICIE 0	OCIE 0	TOIE 0	FOLV2 0	FOLV1 0	OLVL2 0	IEDG1 0	OLVL1 0
Timer A: 31 Timer B: 41	<b>CR2</b> Reset Value	OC1E 0	OC2E 0	OPM 0	PWM 0	CC1 0	CC0 0	IEDG2 0	EXEDG 0
Timer A: 33 Timer B: 43	<b>CSR</b> Reset Value	ICF1 x	OCF1 x	TOF x	ICF2 x	OCF2 x	TIMD 0	- x	- x
Timer A: 34 Timer B: 44	<b>IC1HR</b> Reset Value	MSB x	x	x	x	x	x	x	LSB x
Timer A: 35 Timer B: 45	<b>IC1LR</b> Reset Value	MSB x	x	x	x	x	x	x	LSB x
Timer A: 36 Timer B: 46	<b>OC1HR</b> Reset Value	MSB 1	0	0	0	0	0	0	LSB 0
Timer A: 37 Timer B: 47	<b>OC1LR</b> Reset Value	MSB 0	0	0	0	0	0	0	LSB 0
Timer A: 3E Timer B: 4E	<b>OC2HR</b> Reset Value	MSB 1	0	0	0	0	0	0	LSB 0
Timer A: 3F Timer B: 4F	<b>OC2LR</b> Reset Value	MSB 0	0	0	0	0	0	0	LSB 0
Timer A: 38 Timer B: 48	<b>CHR</b> Reset Value	MSB 1	1	1	1	1	1	1	LSB 1
Timer A: 39 Timer B: 49	<b>CLR</b> Reset Value	MSB 1	1	1	1	1	1	0	LSB 0
Timer A: 3A Timer B: 4A	<b>ACHR</b> Reset Value	MSB 1	1	1	1	1	1	1	LSB 1
Timer A: 3B Timer B: 4B	<b>ACLR</b> Reset Value	MSB 1	1	1	1	1	1	0	LSB 0
Timer A: 3C Timer B: 4C	<b>IC2HR</b> Reset Value	MSB x	x	x	x	x	x	x	LSB x
Timer A: 3D Timer B: 4D	<b>IC2LR</b> Reset Value	MSB x	x	x	x	x	x	x	LSB x

**Related Documentation**

AN 973: SCI software communications using 16-bit timer

AN 974: Real Time Clock with ST7 Timer Output Compare

AN 976: Driving a buzzer through the ST7 Timer PWM function

AN1041: Using ST7 PWM signal to generate analog input (sinusoid)

AN1046: UART emulation software

AN1078: PWM duty cycle switch implementing true 0 or 100 per cent duty cycle

AN1504: Starting a PWM signal directly at high level using the ST7 16-Bit timer

**SERIAL PERIPHERAL INTERFACE (Cont'd)**–  $\overline{SS}$ : Slave select:

This input signal acts as a 'chip select' to let the SPI master communicate with slaves individually and to avoid contention on the data lines. Slave  $\overline{SS}$  inputs can be driven by standard I/O ports on the master MCU.

**10.5.3.1 Functional Description**

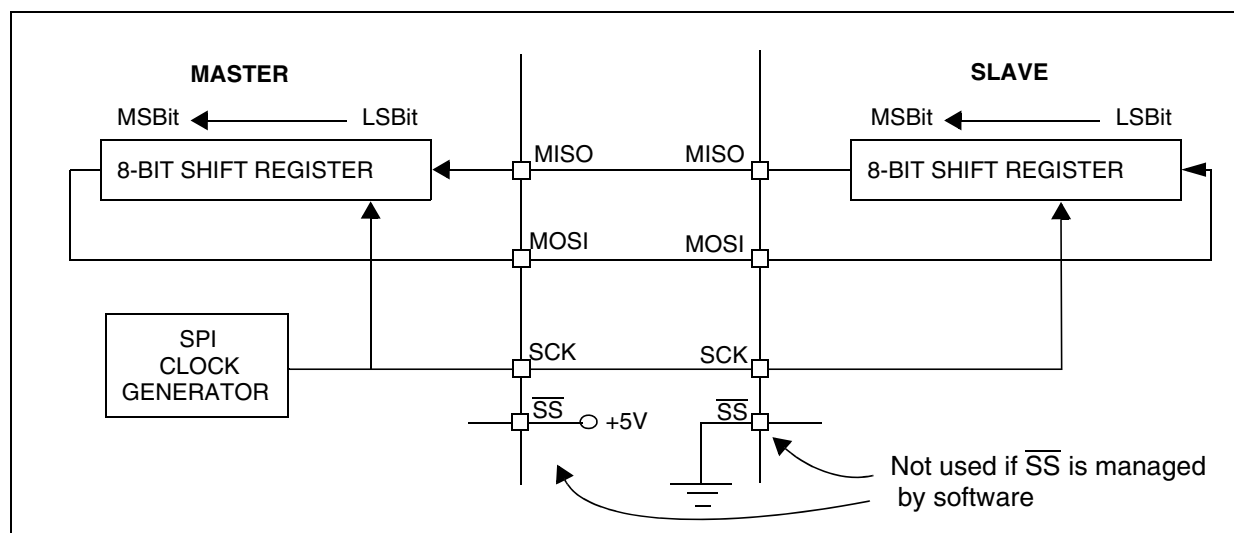
A basic example of interconnections between a single master and a single slave is illustrated in Figure 57.

The MOSI pins are connected together and the MISO pins are connected together. In this way data is transferred serially between master and slave (most significant bit first).

The communication is always initiated by the master. When the master device transmits data to a slave device via MOSI pin, the slave device responds by sending data to the master device via the MISO pin. This implies full duplex communication with both data out and data in synchronized with the same clock signal (which is provided by the master device via the SCK pin).

To use a single data line, the MISO and MOSI pins must be connected at each node ( in this case only simplex communication is possible).

Four possible data/clock timing relationships may be chosen (see Figure 60) but master and slave must be programmed with the same timing mode.

**Figure 57. Single Master/ Single Slave Application**

**SERIAL PERIPHERAL INTERFACE (Cont'd)**

**10.5.3.2 Slave Select Management**

As an alternative to using the  $\overline{SS}$  pin to control the Slave Select signal, the application can choose to manage the Slave Select signal by software. This is configured by the SSM bit in the SPICSR register (see Figure 59)

In software management, the external  $\overline{SS}$  pin is free for other application uses and the internal  $\overline{SS}$  signal level is driven by writing to the SSI bit in the SPICSR register.

**In Master mode:**

- $\overline{SS}$  internal must be held high continuously

**In Slave Mode:**

There are two cases depending on the data/clock timing relationship (see Figure 58):

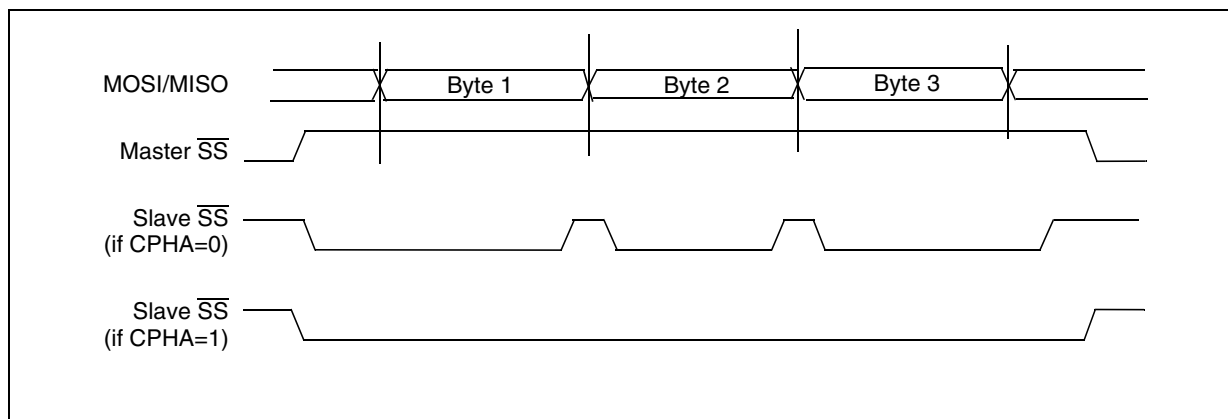
If CPHA=1 (data latched on 2nd clock edge):

- $\overline{SS}$  internal must be held low during the entire transmission. This implies that in single slave applications the  $\overline{SS}$  pin either can be tied to  $V_{SS}$ , or made free for standard I/O by managing the  $\overline{SS}$  function by software (SSM= 1 and SSI=0 in the in the SPICSR register)

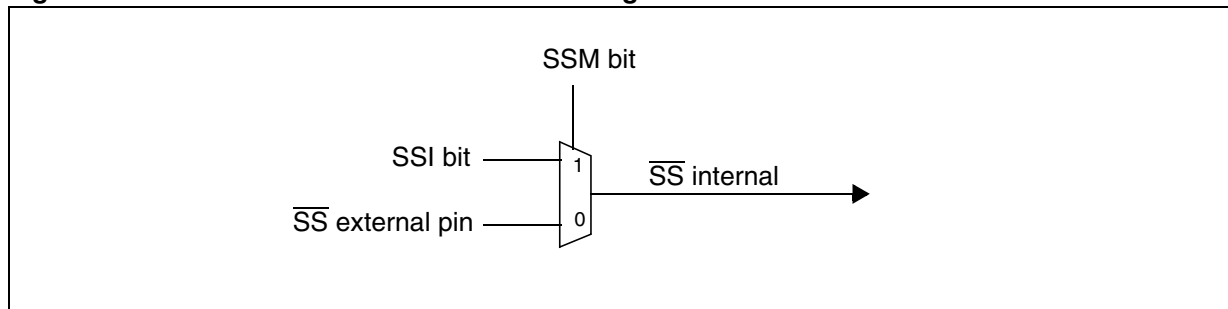
If CPHA=0 (data latched on 1st clock edge):

- $\overline{SS}$  internal must be held low during byte transmission and pulled high between each byte to allow the slave to write to the shift register. If  $\overline{SS}$  is not pulled high, a Write Collision error will occur when the slave writes to the shift register (see Section 10.5.5.3).

**Figure 58. Generic  $\overline{SS}$  Timing Diagram**



**Figure 59. Hardware/Software Slave Select Management**



**SERIAL PERIPHERAL INTERFACE (Cont'd)****CONTROL/STATUS REGISTER (SPICSR)**

Read/Write (some bits Read Only)

Reset Value: 0000 0000 (00h)

7							0
SPIF	WCOL	OVR	MODF	-	SOD	SSM	SSI

Bit 7 = **SPIF** *Serial Peripheral Data Transfer Flag (Read only)*.

This bit is set by hardware when a transfer has been completed. An interrupt is generated if SPIE=1 in the SPICR register. It is cleared by a software sequence (an access to the SPICSR register followed by a write or a read to the SPIDR register).

0: Data transfer is in progress or the flag has been cleared.

1: Data transfer between the device and an external device has been completed.

**Note:** While the SPIF bit is set, all writes to the SPIDR register are inhibited until the SPICSR register is read.

Bit 6 = **WCOL** *Write Collision status (Read only)*.

This bit is set by hardware when a write to the SPIDR register is done during a transmit sequence. It is cleared by a software sequence (see [Figure 61](#)).

0: No write collision occurred

1: A write collision has been detected

Bit 5 = **OVR** *SPI Overrun error (Read only)*.

This bit is set by hardware when the byte currently being received in the shift register is ready to be transferred into the SPIDR register while SPIF = 1 (See [Section 10.5.5.2](#)). An interrupt is generated if SPIE = 1 in SPICR register. The OVR bit is cleared by software reading the SPICSR register.

0: No overrun error

1: Overrun error detected

Bit 4 = **MODF** *Mode Fault flag (Read only)*.

This bit is set by hardware when the  $\overline{SS}$  pin is pulled low in master mode (see [Section 10.5.5.1 Master Mode Fault \(MODF\)](#)). An SPI interrupt can be generated if SPIE=1 in the SPICSR register. This bit is cleared by a software sequence (An access to the SPICR register while MODF=1 followed by a write to the SPICR register).

0: No master mode fault detected

1: A fault in master mode has been detected

Bit 3 = Reserved, must be kept cleared.

Bit 2 = **SOD** *SPI Output Disable*.

This bit is set and cleared by software. When set, it disables the alternate function of the SPI output (MOSI in master mode / MISO in slave mode)

0: SPI output enabled (if SPE=1)

1: SPI output disabled

Bit 1 = **SSM**  $\overline{SS}$  *Management*.

This bit is set and cleared by software. When set, it disables the alternate function of the SPI  $\overline{SS}$  pin and uses the SSI bit value instead. See [Section 10.5.3.2 Slave Select Management](#).

0: Hardware management ( $\overline{SS}$  managed by external pin)

1: Software management (internal  $\overline{SS}$  signal controlled by SSI bit. External  $\overline{SS}$  pin free for general-purpose I/O)

Bit 0 = **SSI**  $\overline{SS}$  *Internal Mode*.

This bit is set and cleared by software. It acts as a 'chip select' by controlling the level of the  $\overline{SS}$  slave select signal when the SSM bit is set.

0 : Slave selected

1 : Slave deselected

**DATA I/O REGISTER (SPIDR)**

Read/Write

Reset Value: Undefined

7							0
D7	D6	D5	D4	D3	D2	D1	D0

The SPIDR register is used to transmit and receive data on the serial bus. In a master device, a write to this register will initiate transmission/reception of another byte.

**Notes:** During the last clock cycle the SPIF bit is set, a copy of the received data byte in the shift register is moved to a buffer. When the user reads the serial peripheral data I/O register, the buffer is actually being read.

While the SPIF bit is set, all writes to the SPIDR register are inhibited until the SPICSR register is read.

**Warning:** A write to the SPIDR register places data directly into the shift register for transmission.

A read to the SPIDR register returns the value located in the buffer and not the content of the shift register (see [Figure 56](#)).

## I<sup>2</sup>C BUS INTERFACE (Cont'd)

### Master Transmitter

Following the address transmission and after SR1 register has been read, the master sends bytes from the DR register to the SDA line via the internal shift register.

The master waits for a read of the SR1 register followed by a write in the DR register, **holding the SCL line low** (see Figure 69 Transfer sequencing EV8).

When the acknowledge bit is received, the interface sets:

- EVF and BTF bits with an interrupt if the ITE bit is set.

To close the communication: after writing the last byte to the DR register, set the STOP bit to generate the Stop condition. The interface goes automatically back to slave mode (M/SL bit cleared).

### Error Cases

- **BERR**: Detection of a Stop or a Start condition during a byte transfer. In this case, the EVF and BERR bits are set by hardware with an interrupt if ITE is set.

Note that BERR will not be set if an error is detected during the first or second pulse of each 9-bit transaction:

#### *Single Master Mode*

If a Start or Stop is issued during the first or second pulse of a 9-bit transaction, the BERR flag will not be set and transfer will continue however the BUSY flag will be reset. To work around this, slave devices should issue a NACK when they receive a misplaced Start or Stop. The reception of a NACK or BUSY by the master in the middle

of communication gives the possibility to reinitiate transmission.

#### *Multimaster Mode*

Normally the BERR bit would be set whenever unauthorized transmission takes place while transfer is already in progress. However, an issue will arise if an external master generates an unauthorized Start or Stop while the I<sup>2</sup>C master is on the first or second pulse of a 9-bit transaction. It is possible to work around this by polling the BUSY bit during I<sup>2</sup>C master mode transmission. The resetting of the BUSY bit can then be handled in a similar manner as the BERR flag being set.

- **AF**: Detection of a non-acknowledge bit. In this case, the EVF and AF bits are set by hardware with an interrupt if the ITE bit is set. To resume, set the Start or Stop bit.  
The AF bit is cleared by reading the I2CSR2 register. However, if read before the completion of the transmission, the AF flag will be set again, thus possibly generating a new interrupt. Software must ensure either that the SCL line is back at 0 before reading the SR2 register, or be able to correctly handle a second interrupt during the 9th pulse of a transmitted byte.
- **ARLO**: Detection of an arbitration lost condition. In this case the ARLO bit is set by hardware (with an interrupt if the ITE bit is set and the interface goes automatically back to slave mode (the M/SL bit is cleared).

**Note:** In all these cases, the SCL line is not held low; however, the SDA line can remain low due to possible «0» bits transmitted last. It is then necessary to release both lines by software.

**I<sup>2</sup>C BUS INTERFACE** (Cont'd)**10.7.7 Register Description****I<sup>2</sup>C CONTROL REGISTER (CR)**

Read / Write

Reset Value: 0000 0000 (00h)

7							0
0	0	PE	ENGC	START	ACK	STOP	ITE

Bit 7:6 = Reserved. Forced to 0 by hardware.

Bit 5 = **PE** *Peripheral enable*.

This bit is set and cleared by software.

0: Peripheral disabled

1: Master/Slave capability

Notes:

- When PE=0, all the bits of the CR register and the SR register except the Stop bit are reset. All outputs are released while PE=0
- When PE=1, the corresponding I/O pins are selected by hardware as alternate functions.
- To enable the I<sup>2</sup>C interface, write the CR register **TWICE** with PE=1 as the first write only activates the interface (only PE is set).

Bit 4 = **ENGC** *Enable General Call*.

This bit is set and cleared by software. It is also cleared by hardware when the interface is disabled (PE=0). The 00h General Call address is acknowledged (01h ignored).

0: General Call disabled

1: General Call enabled

**Note:** In accordance with the I2C standard, when GCAL addressing is enabled, an I2C slave can only receive data. It will not transmit data to the master.

Bit 3 = **START** *Generation of a Start condition*.

This bit is set and cleared by software. It is also cleared by hardware when the interface is disabled (PE=0) or when the Start condition is sent (with interrupt generation if ITE=1).

– In master mode:

0: No start generation

1: Repeated start generation

– In slave mode:

0: No start generation

1: Start generation when the bus is free

Bit 2 = **ACK** *Acknowledge enable*.

This bit is set and cleared by software. It is also cleared by hardware when the interface is disabled (PE=0).

0: No acknowledge returned

1: Acknowledge returned after an address byte or a data byte is received

Bit 1 = **STOP** *Generation of a Stop condition*.

This bit is set and cleared by software. It is also cleared by hardware in master mode. Note: This bit is not cleared when the interface is disabled (PE=0).

– In master mode:

0: No stop generation

1: Stop generation after the current byte transfer or after the current Start condition is sent. The STOP bit is cleared by hardware when the Stop condition is sent.

– In slave mode:

0: No stop generation

1: Release the SCL and SDA lines after the current byte transfer (BTF=1). In this mode the STOP bit has to be cleared by software.

Bit 0 = **ITE** *Interrupt enable*.

This bit is set and cleared by software and cleared by hardware when the interface is disabled (PE=0).

0: Interrupts disabled

1: Interrupts enabled

Refer to [Figure 70](#) for the relationship between the events and the interrupt.

SCL is held low when the ADD10, SB, BTF or ADSL flags or an EV6 event (See [Figure 69](#)) is detected.

**I<sup>2</sup>C BUS INTERFACE** (Cont'd)**I<sup>2</sup>C STATUS REGISTER 1 (SR1)**

Read Only

Reset Value: 0000 0000 (00h)

7							0
EVF	ADD10	TRA	BUSY	BTF	ADSL	M/SL	SB

Bit 7 = **EVF** *Event flag*.

This bit is set by hardware as soon as an event occurs. It is cleared by software reading SR2 register in case of error event or as described in [Figure 69](#). It is also cleared by hardware when the interface is disabled (PE=0).

0: No event

1: One of the following events has occurred:

- BTF=1 (Byte received or transmitted)
- ADSL=1 (Address matched in Slave mode while ACK=1)
- SB=1 (Start condition generated in Master mode)
- AF=1 (No acknowledge received after byte transmission)
- STOPF=1 (Stop condition detected in Slave mode)
- ARLO=1 (Arbitration lost in Master mode)
- BERR=1 (Bus error, misplaced Start or Stop condition detected)
- ADD10=1 (Master has sent header byte)
- Address byte successfully transmitted in Master mode.

Bit 6 = **ADD10** *10-bit addressing in Master mode*.

This bit is set by hardware when the master has sent the first byte in 10-bit address mode. It is cleared by software reading SR2 register followed by a write in the DR register of the second address byte. It is also cleared by hardware when the peripheral is disabled (PE=0).

0: No ADD10 event occurred.

1: Master has sent first address byte (header)

Bit 5 = **TRA** *Transmitter/Receiver*.

When BTF is set, TRA=1 if a data byte has been transmitted. It is cleared automatically when BTF is cleared. It is also cleared by hardware after detection of Stop condition (STOPF=1), loss of bus arbitration (ARLO=1) or when the interface is disabled (PE=0).

0: Data byte received (if BTF=1)

1: Data byte transmitted

Bit 4 = **BUSY** *Bus busy*.

This bit is set by hardware on detection of a Start condition and cleared by hardware on detection of a Stop condition. It indicates a communication in progress on the bus. The BUSY flag of the I2CSR1 register is cleared if a Bus Error occurs.

0: No communication on the bus

1: Communication ongoing on the bus

Note:

- The BUSY flag is NOT updated when the interface is disabled (PE=0). This can have consequences when operating in Multimaster mode; i.e. a second active I<sup>2</sup>C master commencing a transfer with an unset BUSY bit can cause a conflict resulting in lost data. A software workaround consists of checking that the I<sup>2</sup>C is not busy before enabling the I<sup>2</sup>C Multimaster cell.

Bit 3 = **BTF** *Byte transfer finished*.

This bit is set by hardware as soon as a byte is correctly received or transmitted with interrupt generation if ITE=1. It is cleared by software reading SR1 register followed by a read or write of DR register. It is also cleared by hardware when the interface is disabled (PE=0).

- Following a byte transmission, this bit is set after reception of the acknowledge clock pulse. In case an address byte is sent, this bit is set only after the EV6 event (See [Figure 69](#)). BTF is cleared by reading SR1 register followed by writing the next byte in DR register.

- Following a byte reception, this bit is set after transmission of the acknowledge clock pulse if ACK=1. BTF is cleared by reading SR1 register followed by reading the byte from DR register.

The SCL line is held low while BTF=1.

0: Byte transfer not done

1: Byte transfer succeeded

Bit 2 = **ADSL** *Address matched (Slave mode)*.

This bit is set by hardware as soon as the received slave address matched with the OAR register content or a general call is recognized. An interrupt is generated if ITE=1. It is cleared by software reading SR1 register or by hardware when the interface is disabled (PE=0).

The SCL line is held low while ADSL=1.

0: Address mismatched or not received

1: Received address matched



### 10.8 10-BIT A/D CONVERTER (ADC)

#### 10.8.1 Introduction

The on-chip Analog to Digital Converter (ADC) peripheral is a 10-bit, successive approximation converter with internal sample and hold circuitry. This peripheral has up to 16 multiplexed analog input channels (refer to device pin out description) that allow the peripheral to convert the analog voltage levels from up to 16 different sources.

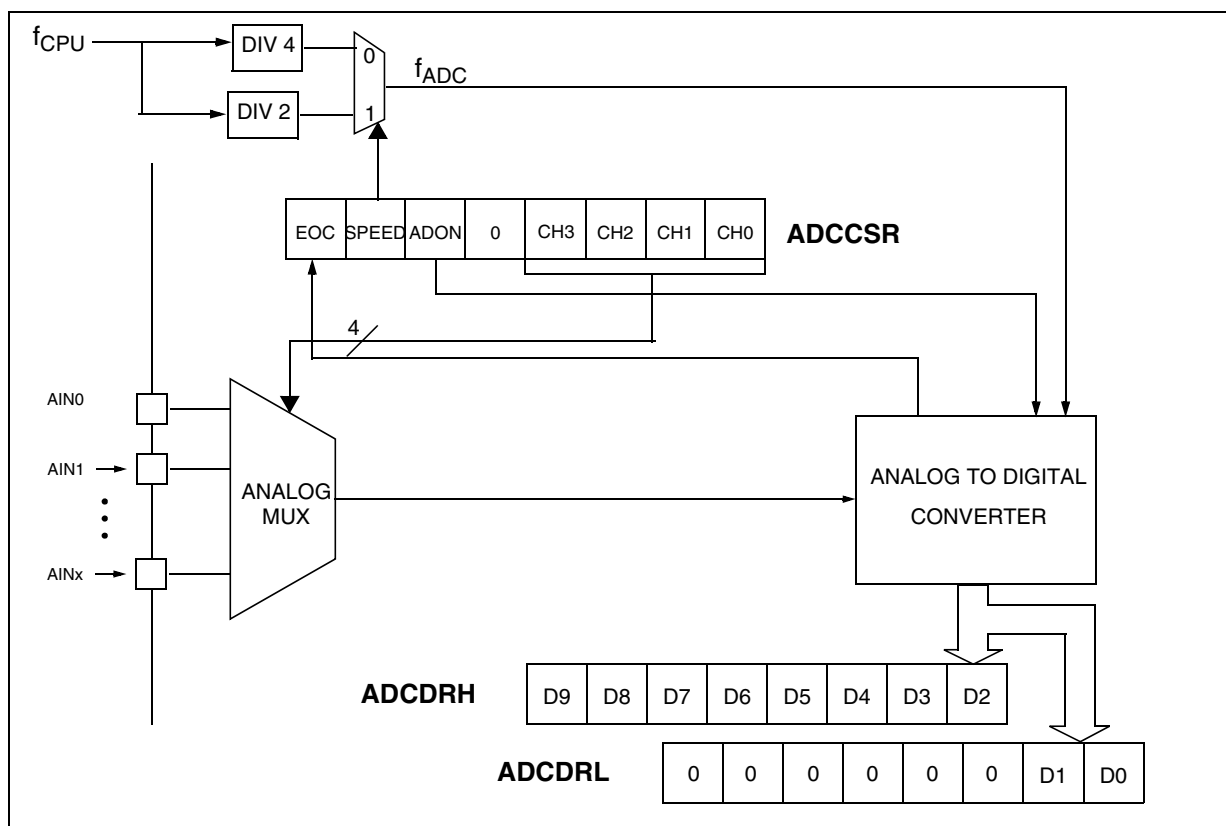
The result of the conversion is stored in a 10-bit Data Register. The A/D converter is controlled through a Control/Status Register.

#### 10.8.2 Main Features

- 10-bit conversion
- Up to 16 channels with multiplexed input
- Linear successive approximation
- Data register (DR) which contains the results
- Conversion complete status flag
- On/off bit (to reduce consumption)

The block diagram is shown in [Figure 71](#).

Figure 71. ADC Block Diagram



## 12.6 MEMORY CHARACTERISTICS

### 12.6.1 RAM and Hardware Registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{RM}$	Data retention mode <sup>1)</sup>	HALT mode (or RESET)	1.6			V

### 12.6.2 FLASH Memory

DUAL VOLTAGE HDFLASH MEMORY						
Symbol	Parameter	Conditions	Min <sup>2)</sup>	Typ	Max <sup>2)</sup>	Unit
$f_{CPU}$	Operating frequency	Read mode	0		8	MHz
		Write / Erase mode	1		8	
$V_{PP}$	Programming voltage <sup>3)</sup>	$4.5V \leq V_{DD} \leq 5.5V$	11.4		12.6	V
$I_{DD}$	Supply current <sup>4)</sup>	RUN mode ( $f_{CPU} = 4MHz$ )			3	mA
		Write / Erase		0		
		Power down mode / HALT		1	10	$\mu A$
$I_{PP}$	$V_{PP}$ current <sup>4)</sup>	Read ( $V_{PP}=12V$ )			200	$\mu A$
		Write / Erase			30	mA
$t_{VPP}$	Internal $V_{PP}$ stabilization time			10		$\mu s$
$t_{RET}$	Data retention	$T_A=85^\circ C$	40			years
		$T_A=105^\circ C$	15			
		$T_A=125^\circ C$	7			
$N_{RW}$	Write erase cycles	$T_A= 55^\circ C$	1000			cycles
		$T_A= 85^\circ C$	100			cycles
$T_{PROG}$ $T_{ERASE}$	Programming or erasing temperature range		-40	25	85	$^\circ C$

#### Notes:

1. Minimum  $V_{DD}$  supply voltage without losing data stored in RAM (in HALT mode or under RESET) or in hardware registers (only in HALT mode). Not tested in production.
2. Data based on characterization results, not tested in production.
3.  $V_{PP}$  must be applied only during the programming or erasing operation and not permanently for reliability reasons.
4. Data based on simulation results, not tested in production.

**Warning:** Do not connect 12V to  $V_{PP}$  before  $V_{DD}$  is powered on, as this may damage the device.

## 12.8 I/O PORT PIN CHARACTERISTICS

### 12.8.1 General Characteristics

Subject to general operating conditions for  $V_{DD}$ ,  $f_{OSC}$ , and  $T_A$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL}$	Input low level voltage <sup>1)</sup>	CMOS ports			$0.3 \times V_{DD}$	V
$V_{IH}$	Input high level voltage <sup>1)</sup>		$0.7 \times V_{DD}$			
$V_{hys}$	Schmitt trigger voltage hysteresis <sup>2)</sup>			0.7		
$I_{INJ(PIN)}^{3)}$	Injected Current on PB0 (Flash devices only)	$V_{DD}=5V$	0		+4	mA
	Injected Current on an I/O pin				$\pm 4$	
$\Sigma I_{INJ(PIN)}^{3)}$	Total injected current (sum of all I/O and control pins)				$\pm 25$	
$I_L$	Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			$\pm 1$	$\mu A$
$I_S$	Static current consumption	Floating input mode <sup>4)</sup>		400		
$R_{PU}$	Weak pull-up equivalent resistor <sup>5)</sup>	$V_{IN}=V_{SS}$   $V_{DD}=5V$	50	120	250	k $\Omega$
$C_{IO}$	I/O pin capacitance			5		pF
$t_{f(I/O)out}$	Output high to low level fall time <sup>1)</sup>	$C_L=50pF$ Between 10% and 90%		25		ns
$t_{r(I/O)out}$	Output low to high level rise time <sup>1)</sup>			25		
$t_{w(I)in}$	External interrupt pulse time <sup>6)</sup>		1			$t_{CPU}$

Figure 79. Unused I/Os configured as input

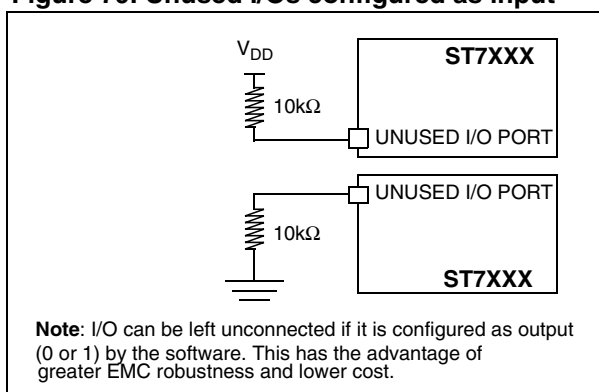
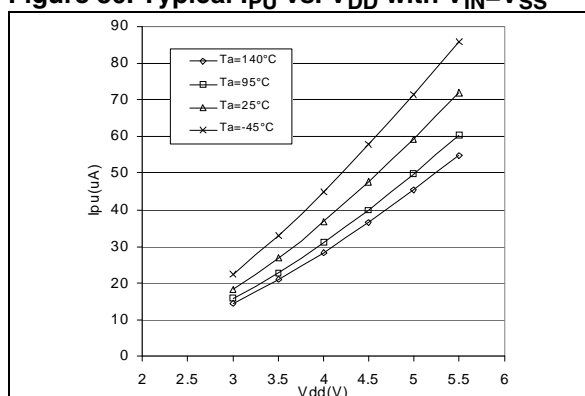


Figure 80. Typical  $I_{PU}$  vs.  $V_{DD}$  with  $V_{IN}=V_{SS}$



#### Notes:

- Data based on characterization results, not tested in production.
- Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
- When the current limitation is not possible, the  $V_{IN}$  maximum must be respected, otherwise refer to  $I_{INJ(PIN)}$  specification. A positive injection is induced by  $V_{IN} > V_{DD}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ . Refer to [section 12.2.2 on page 143](#) for more details.
- Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example and leaving the I/O unconnected on the board or an external pull-up or pull-down resistor (see [Figure 79](#)). Static peak current value taken at a fixed  $V_{IN}$  value, based on design simulation and technology characteristics, not tested in production. This value depends on  $V_{DD}$  and temperature values.
- The  $R_{PU}$  pull-up equivalent resistor is based on a resistive transistor (corresponding  $I_{PU}$  current characteristics described in [Figure 80](#)).
- To generate an external interrupt, a minimum pulse width has to be applied on an I/O port pin configured as an external interrupt source.

## 12.10 TIMER PERIPHERAL CHARACTERISTICS

Subject to general operating conditions for  $V_{DD}$ ,  $f_{OSC}$ , and  $T_A$  unless otherwise specified.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output...).

### 12.10.1 8-Bit PWM-ART Auto-Reload Timer

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{res(PWM)}$	PWM resolution time		1			$t_{CPU}$
		$f_{CPU}=8MHz$	125			ns
$f_{EXT}$	ART external clock frequency		0		$f_{CPU}/2$	MHz
$f_{PWM}$	PWM repetition rate		0		$f_{CPU}/2$	
$Res_{PWM}$	PWM resolution				8	bit
$V_{OS}$	PWM/DAC output step voltage	$V_{DD}=5V$ , Res=8-bits		20		mV

### 12.10.2 16-Bit Timer

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(ICAP)in}$	Input capture pulse time		1			$t_{CPU}$
$t_{res(PWM)}$	PWM resolution time		2			$t_{CPU}$
		$f_{CPU}=8MHz$	250			ns
$f_{EXT}$	Timer external clock frequency		0		$f_{CPU}/4$	MHz
$f_{PWM}$	PWM repetition rate		0		$f_{CPU}/4$	MHz
$Res_{PWM}$	PWM resolution				16	bit

COMMUNICATION INTERFACE CHARACTERISTICS (Cont'd)

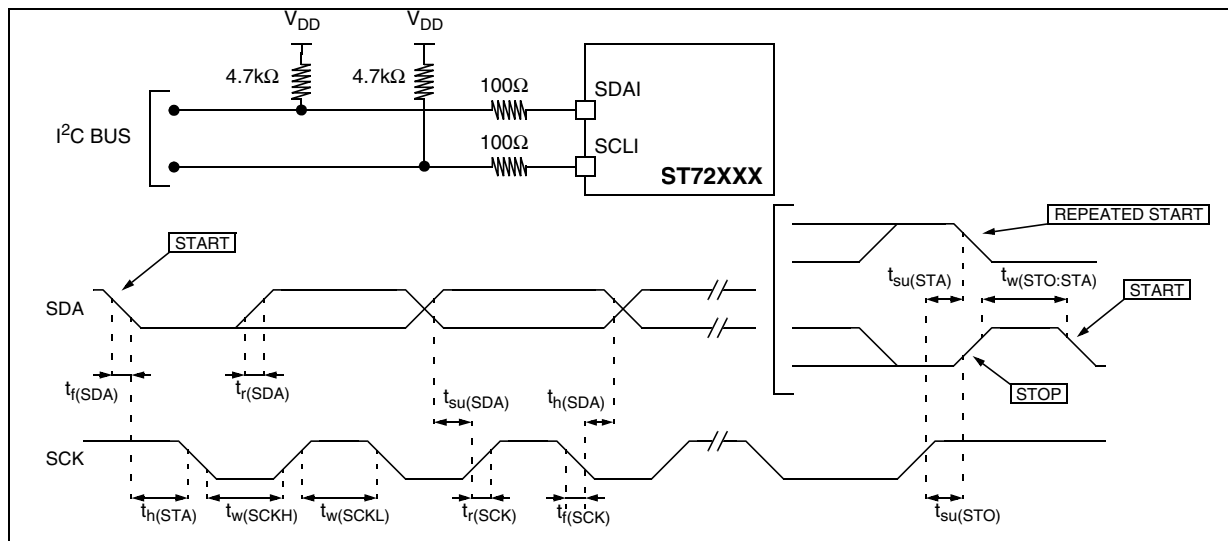
12.11.2 I<sup>2</sup>C - Inter IC Control Interface

Subject to general operating conditions for V<sub>DD</sub>, f<sub>CPU</sub>, and T<sub>A</sub> unless otherwise specified.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDAI and SCLI). The ST7 I<sup>2</sup>C interface meets the requirements of the Standard I<sup>2</sup>C communication protocol described in the following table.

Symbol	Parameter	Standard mode I <sup>2</sup> C		Fast mode I <sup>2</sup> C <sup>5)</sup>		Unit
		Min <sup>1)</sup>	Max <sup>1)</sup>	Min <sup>1)</sup>	Max <sup>1)</sup>	
t <sub>w(SCLL)</sub>	SCL clock low time	4.7		1.3		μs
t <sub>w(SCLH)</sub>	SCL clock high time	4.0		0.6		
t <sub>su(SDA)</sub>	SDA setup time	250		100		ns
t <sub>h(SDA)</sub>	SDA data hold time	0 <sup>3)</sup>		0 <sup>2)</sup>	900 <sup>3)</sup>	
t <sub>r(SDA)</sub> t <sub>r(SCL)</sub>	SDA and SCL rise time		1000	20+0.1C <sub>b</sub>	300	
t <sub>f(SDA)</sub> t <sub>f(SCL)</sub>	SDA and SCL fall time		300	20+0.1C <sub>b</sub>	300	
t <sub>h(STA)</sub>	START condition hold time	4.0		0.6		μs
t <sub>su(STA)</sub>	Repeated START condition setup time	4.7		0.6		
t <sub>su(STO)</sub>	STOP condition setup time	4.0		0.6		μs
t <sub>w(STO:STA)</sub>	STOP to START condition time (bus free)	4.7		1.3		μs
C <sub>b</sub>	Capacitive load for each bus line		400		400	pF

Figure 93. Typical Application with I<sup>2</sup>C Bus and Timing Diagram <sup>4)</sup>



Notes:

1. Data based on standard I<sup>2</sup>C protocol requirement, not tested in production.
2. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
3. The maximum hold time of the START condition has only to be met if the interface does not stretch the low period of SCL signal.
4. Measurement points are done at CMOS levels: 0.3xV<sub>DD</sub> and 0.7xV<sub>DD</sub>.
5. At 4MHz f<sub>CPU</sub>, max.I<sup>2</sup>C speed (400kHz) is not achievable. In this case, max. I<sup>2</sup>C speed will be approximately 260kHz.