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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	I <sup>2</sup> C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/st72f325k6tce">https://www.e-xfl.com/product-detail/stmicroelectronics/st72f325k6tce</a>

## 2 PIN DESCRIPTION

Figure 2. 64-Pin LQFP 14x14 and 10x10 Package Pinout

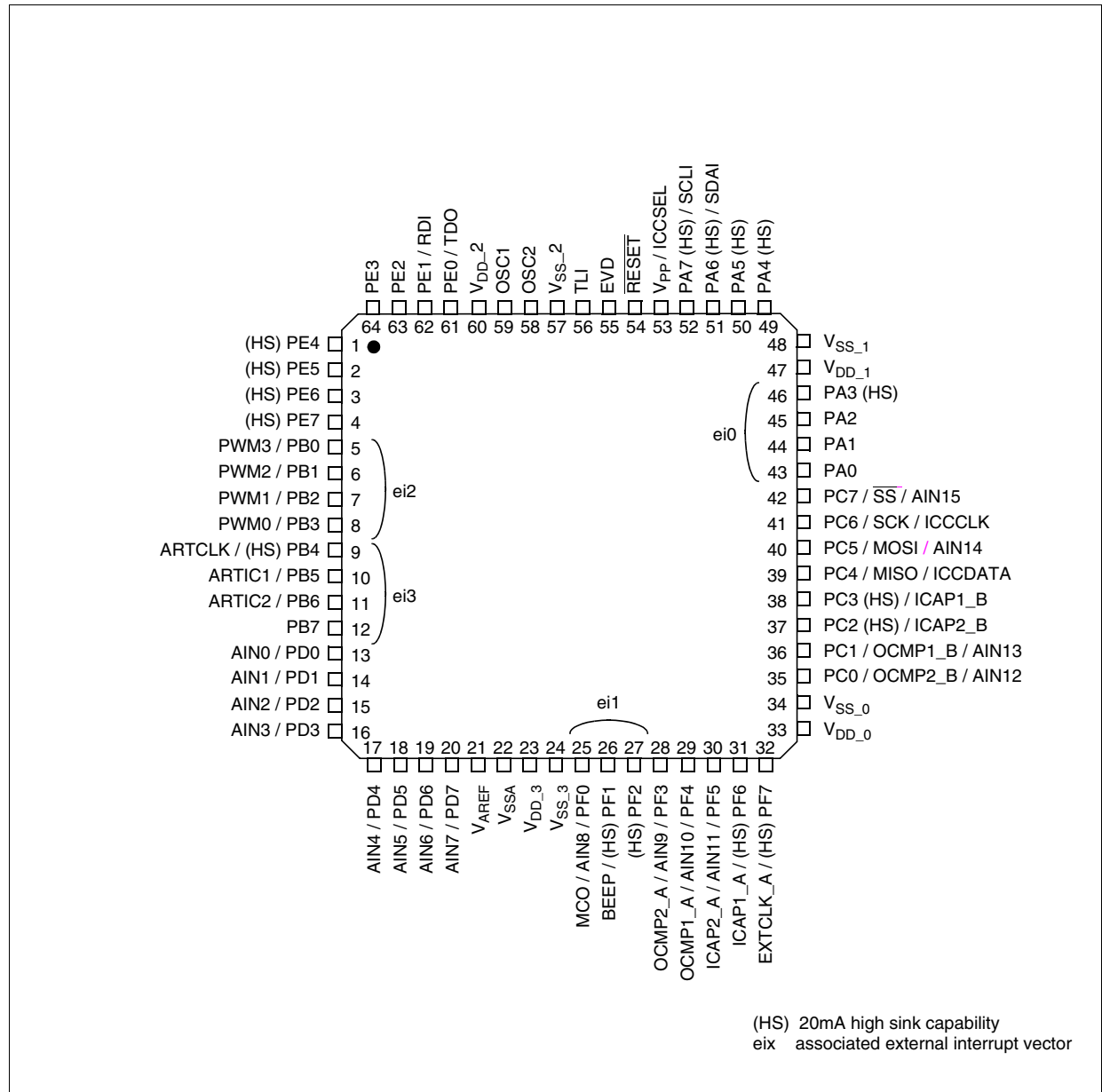
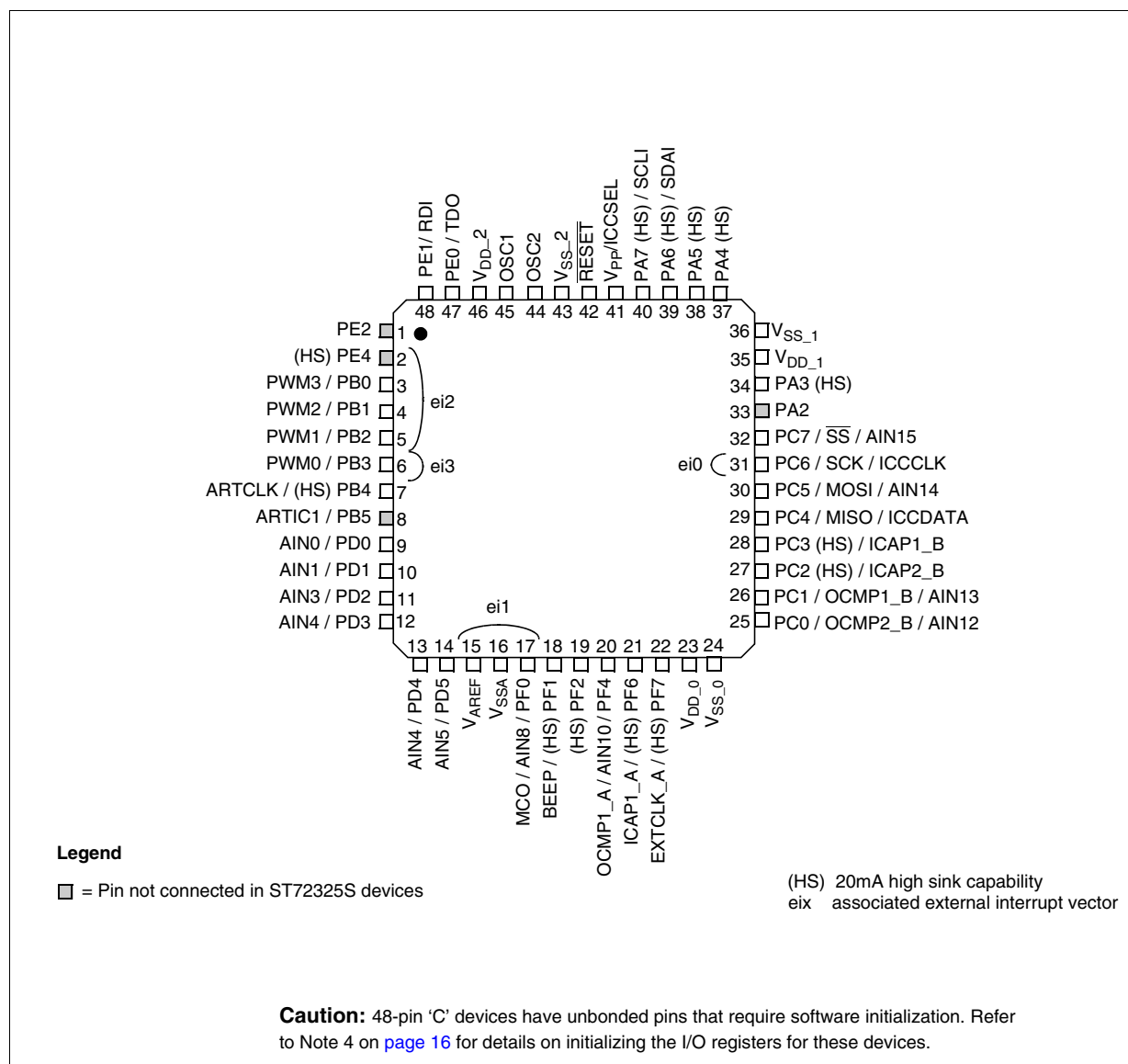


Figure 3. 48-Pin LQFP 7x7 Device Pinout



Address	Block	Register Label	Register Name	Reset Status	Remarks
002Ch 002Dh	MCC	MCCSR MCCBCR	Main Clock Control / Status Register Main Clock Controller: Beep Control Register	00h 00h	R/W R/W
002Eh to 0030h	Reserved Area (3 Bytes)				
0031h 0032h 0033h 0034h 0035h 0036h 0037h 0038h 0039h 003Ah 003Bh 003Ch 003Dh 003Eh 003Fh	TIMER A	TACR2 TACR1 TACSR TAIC1HR TAIC1LR TAOC1HR TAOC1LR TACHR TACLR TAACHR TAACLR TAIC2HR TAIC2LR TAOC2HR TAOC2LR	Timer A Control Register 2 Timer A Control Register 1 Timer A Control/Status Register Timer A Input Capture 1 High Register Timer A Input Capture 1 Low Register Timer A Output Compare 1 High Register Timer A Output Compare 1 Low Register Timer A Counter High Register Timer A Counter Low Register Timer A Alternate Counter High Register Timer A Alternate Counter Low Register Timer A Input Capture 2 High Register Timer A Input Capture 2 Low Register Timer A Output Compare 2 High Register Timer A Output Compare 2 Low Register	00h 00h xxxx x0xx b xxh xxh 80h 00h FFh FCh FFh FCh xxh xxh 80h 00h	R/W R/W R/W Read Only Read Only R/W R/W Read Only Read Only Read Only Read Only Read Only Read Only R/W R/W
0040h	Reserved Area (1 Byte)				
0041h 0042h 0043h 0044h 0045h 0046h 0047h 0048h 0049h 004Ah 004Bh 004Ch 004Dh 004Eh 004Fh	TIMER B	TBCR2 TBCR1 TBCSR TBIC1HR TBIC1LR TBOC1HR TBOC1LR TBCHR TBCLR TBACHR TBACLR TBIC2HR TBIC2LR TBOC2HR TBOC2LR	Timer B Control Register 2 Timer B Control Register 1 Timer B Control/Status Register Timer B Input Capture 1 High Register Timer B Input Capture 1 Low Register Timer B Output Compare 1 High Register Timer B Output Compare 1 Low Register Timer B Counter High Register Timer B Counter Low Register Timer B Alternate Counter High Register Timer B Alternate Counter Low Register Timer B Input Capture 2 High Register Timer B Input Capture 2 Low Register Timer B Output Compare 2 High Register Timer B Output Compare 2 Low Register	00h 00h xxxx x0xx b xxh xxh 80h 00h FFh FCh FFh FCh xxh xxh 80h 00h	R/W R/W R/W Read Only Read Only R/W R/W Read Only Read Only Read Only Read Only Read Only Read Only R/W R/W
0050h 0051h 0052h 0053h 0054h 0055h 0056h 0057h	SCI	SCISR SCIDR SCIBRR SCICR1 SCICR2 SCIERP SCIETPR	SCI Status Register SCI Data Register SCI Baud Rate Register SCI Control Register 1 SCI Control Register 2 SCI Extended Receive Prescaler Register Reserved area SCI Extended Transmit Prescaler Register	C0h xxh 00h x000 0000b 00h 00h ---	Read Only R/W R/W R/W R/W R/W R/W

## 6.3 RESET SEQUENCE MANAGER (RSM)

### 6.3.1 Introduction

The reset sequence manager includes three RESET sources as shown in [Figure 15](#):

- External  $\overline{\text{RESET}}$  source pulse
- Internal LVD RESET (Low Voltage Detection)
- Internal WATCHDOG RESET

These sources act on the  $\overline{\text{RESET}}$  pin and it is always kept low during the delay phase.

The RESET service routine vector is fixed at addresses FFFEh-FFFFh in the ST7 memory map.

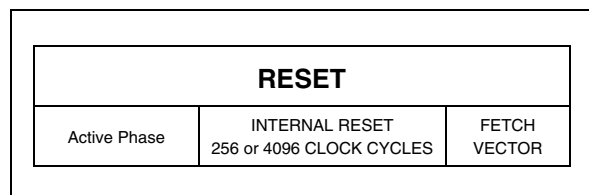
The basic RESET sequence consists of 3 phases as shown in [Figure 14](#):

- Active Phase depending on the RESET source
- 256 or 4096 CPU clock cycle delay (selected by option byte)
- RESET vector fetch

The 256 or 4096 CPU clock cycle delay allows the oscillator to stabilise and ensures that recovery has taken place from the Reset state. The shorter or longer clock cycle delay should be selected by option byte to correspond to the stabilization time of the external oscillator used in the application (see [section 14.1 on page 181](#)).

The RESET vector fetch phase duration is 2 clock cycles.

**Figure 14. RESET Sequence Phases**



**Caution:** When the ST7 is unprogrammed or fully erased, the Flash is blank and the RESET vector is not programmed.

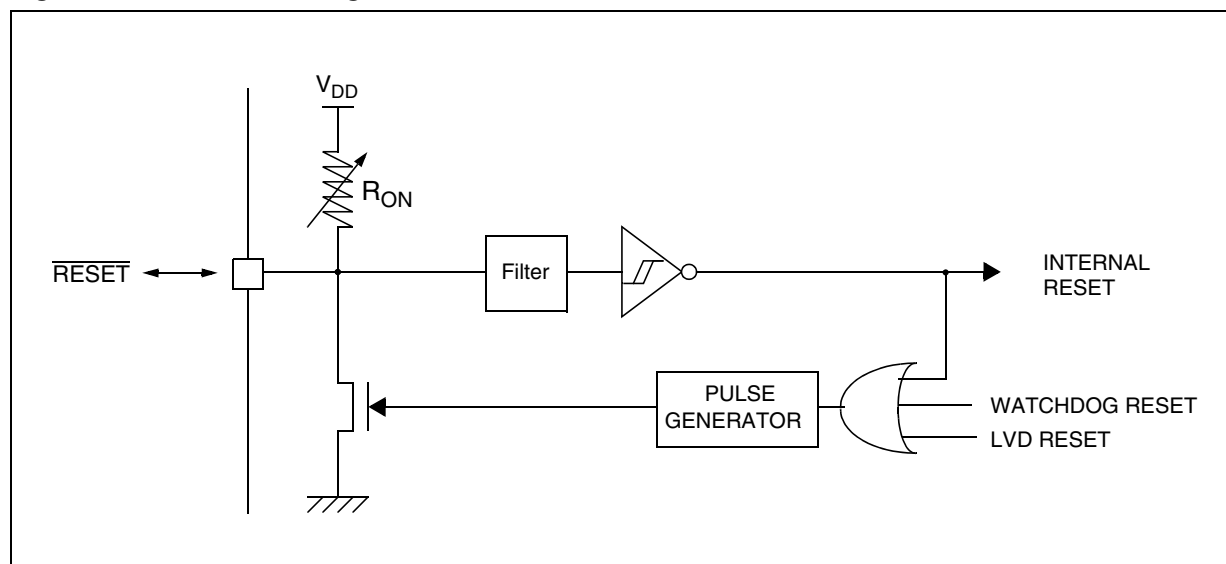
For this reason, it is recommended to keep the RESET pin in low state until programming mode is entered, in order to avoid unwanted behavior.

### 6.3.2 Asynchronous External $\overline{\text{RESET}}$ pin

The  $\overline{\text{RESET}}$  pin is both an input and an open-drain output with integrated  $R_{\text{ON}}$  weak pull-up resistor. This pull-up has no fixed value but varies in accordance with the input voltage. It can be pulled low by external circuitry to reset the device. See [“CONTROL PIN CHARACTERISTICS” on page 162](#) for more details.

A RESET signal originating from an external source must have a duration of at least  $t_{\text{h(RSTL)}}_{\text{in}}$  in order to be recognized (see [Figure 16](#)). This detection is asynchronous and therefore the MCU can enter reset state even in HALT mode.

**Figure 15. Reset Block Diagram**



## INTERRUPTS (Cont'd)

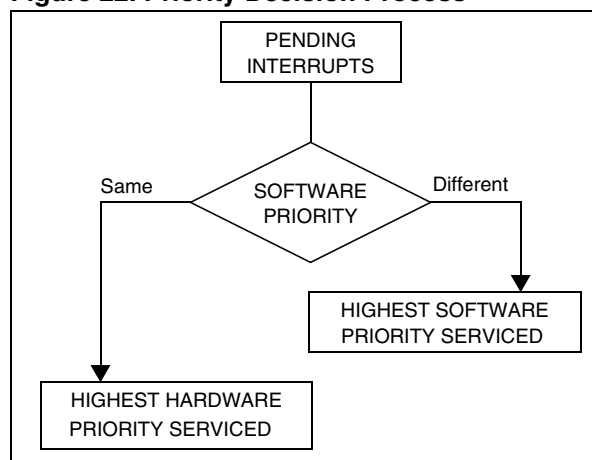
### Servicing Pending Interrupts

As several interrupts can be pending at the same time, the interrupt to be taken into account is determined by the following two-step process:

- the highest software priority interrupt is serviced,
- if several interrupts have the same software priority then the interrupt with the highest hardware priority is serviced first.

Figure 22 describes this decision process.

**Figure 22. Priority Decision Process**



When an interrupt request is not serviced immediately, it is latched and then processed when its software priority combined with the hardware priority becomes the highest one.

**Note 1:** The hardware priority is exclusive while the software one is not. This allows the previous process to succeed with only one interrupt.

**Note 2:** TLI, RESET and TRAP can be considered as having the highest software priority in the decision process.

### Different Interrupt Vector Sources

Two interrupt source types are managed by the ST7 interrupt controller: the non-maskable type (RESET, TRAP) and the maskable type (external or from internal peripherals).

### Non-Maskable Sources

These sources are processed regardless of the state of the I1 and I0 bits of the CC register (see Figure 21). After stacking the PC, X, A and CC registers (except for RESET), the corresponding vector is loaded in the PC register and the I1 and I0 bits of the CC are set to disable interrupts (level 3). These sources allow the processor to exit HALT mode.

#### ■ TRAP (Non Maskable Software Interrupt)

This software interrupt is serviced when the TRAP instruction is executed. It will be serviced according to the flowchart in Figure 21.

**Caution:** TRAP can be interrupted by a TLI.

#### ■ RESET

The RESET source has the highest priority in the ST7. This means that the first current routine has the highest software priority (level 3) and the highest hardware priority.

See the RESET chapter for more details.

### Maskable Sources

Maskable interrupt vector sources can be serviced if the corresponding interrupt is enabled and if its own interrupt software priority (in ISPRx registers) is higher than the one currently being serviced (I1 and I0 in CC register). If any of these two conditions is false, the interrupt is latched and thus remains pending.

#### ■ TLI (Top Level Hardware Interrupt)

This hardware interrupt occurs when a specific edge is detected on the dedicated TLI pin. It will be serviced according to the flowchart in Figure 21 as a trap.

**Caution:** A TRAP instruction must not be used in a TLI service routine.

#### ■ External Interrupts

External interrupts allow the processor to exit from HALT low power mode. External interrupt sensitivity is software selectable through the External Interrupt Control register (EICR).

External interrupt triggered on edge will be latched and the interrupt request automatically cleared upon entering the interrupt service routine.

If several input pins of a group connected to the same interrupt line are selected simultaneously, these will be logically ORed.

#### ■ Peripheral Interrupts

Usually the peripheral interrupts cause the MCU to exit from HALT mode except those mentioned in the "Interrupt Mapping" table. A peripheral interrupt occurs when a specific flag is set in the peripheral status registers and if the corresponding enable bit is set in the peripheral control register. The general sequence for clearing an interrupt is based on an access to the status register followed by a read or write to an associated register.

**Note:** The clearing sequence resets the internal latch. A pending interrupt (i.e. waiting for being serviced) will therefore be lost if the clear sequence is executed.

**Table 15. Watchdog Timer Register Map and Reset Values**

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
002Ah	<b>WDGCR</b> Reset Value	WDGA 0	T6 1	T5 1	T4 1	T3 1	T2 1	T1 1	T0 1

**MAIN CLOCK CONTROLLER WITH REAL TIME CLOCK (Cont'd)**

Bit 0 = **OIF** *Oscillator interrupt flag*

This bit is set by hardware and cleared by software reading the MCCR register. It indicates when set that the main oscillator has reached the selected elapsed time (TB1:0).

0: Timeout not reached

1: Timeout reached

**CAUTION:** The BRES and BSET instructions must not be used on the MCCR register to avoid unintentionally clearing the OIF bit.

**MCC BEEP CONTROL REGISTER (MCCBCR)**

Read/Write

Reset Value: 0000 0000 (00h)

7						0	
0	0	0	0	0	0	BC1	BC0

Bit 7:2 = Reserved, must be kept cleared.

Bit 1:0 = **BC[1:0]** *Beep control*

These 2 bits select the PF1 pin beep capability.

BC1	BC0	Beep mode with $f_{OSC2}=8\text{MHz}$	
0	0	Off	
0	1	~2-KHz	Output Beep signal ~50% duty cycle
1	0	~1-KHz	
1	1	~500-Hz	

The beep output signal is available in ACTIVE-HALT mode but has to be disabled to reduce the consumption.

**Table 16. Main Clock Controller Register Map and Reset Values**

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
002Bh	<b>SICSR</b> Reset Value	AVDS 0	AVDIE 0	AVDF 0	LVDRF x	0	CSSIE 0	CSSD 0	WDGRF x
002Ch	<b>MCCSR</b> Reset Value	MCO 0	CP1 0	CP0 0	SMS 0	TB1 0	TB0 0	OIE 0	OIF 0
002Dh	<b>MCCBCR</b> Reset Value	0	0	0	0	0	0	BC1 0	BC0 0



## 16-BIT TIMER (Cont'd)

### 10.4.3.3 Input Capture

In this section, the index,  $i$ , may be 1 or 2 because there are two input capture functions in the 16-bit timer.

The two 16-bit input capture registers (IC1R and IC2R) are used to latch the value of the free running counter after a transition is detected on the ICAP $i$  pin (see Figure 5).

	MS Byte	LS Byte
ICiR	ICiHR	ICiLR

ICiR register is a read-only register.

The active transition is software programmable through the IEDG $i$  bit of Control Registers (CR $i$ ).

Timing resolution is one count of the free running counter: ( $f_{CPU}/CC[1:0]$ ).

#### Procedure:

To use the input capture function select the following in the CR2 register:

- Select the timer clock (CC[1:0]) (see Table 1).
- Select the edge of the active transition on the ICAP2 pin with the IEDG2 bit (the ICAP2 pin must be configured as floating input or input with pull-up without interrupt if this configuration is available).

And select the following in the CR1 register:

- Set the ICIE bit to generate an interrupt after an input capture coming from either the ICAP1 pin or the ICAP2 pin
- Select the edge of the active transition on the ICAP1 pin with the IEDG1 bit (the ICAP1 pin must be configured as floating input or input with pull-up without interrupt if this configuration is available).

When an input capture occurs:

- ICF $i$  bit is set.
- The ICiR register contains the value of the free running counter on the active transition on the ICAP $i$  pin (see Figure 6).
- A timer interrupt is generated if the ICIE bit is set and the I bit is cleared in the CC register. Otherwise, the interrupt remains pending until both conditions become true.

Clearing the Input Capture interrupt request (that is, clearing the ICF $i$  bit) is done in two steps:

1. Reading the SR register while the ICF $i$  bit is set.
2. An access (read or write) to the ICiLR register.

#### Notes:

1. After reading the ICiHR register, transfer of input capture data is inhibited and ICF $i$  will never be set until the ICiLR register is also read.
2. The ICiR register contains the free running counter value which corresponds to the most recent input capture.
3. The two input capture functions can be used together even if the timer also uses the two output compare functions.
4. In One Pulse mode and PWM mode only Input Capture 2 can be used.
5. The alternate inputs (ICAP1 and ICAP2) are always directly connected to the timer. So any transitions on these pins activates the input capture function.  
Moreover if one of the ICAP $i$  pins is configured as an input and the second one as an output, an interrupt can be generated if the user toggles the output pin and if the ICIE bit is set. This can be avoided if the input capture function  $i$  is disabled by reading the ICiHR (see note 1).
6. The TOF bit can be used with interrupt generation in order to measure events that go beyond the timer range (FFFFh).

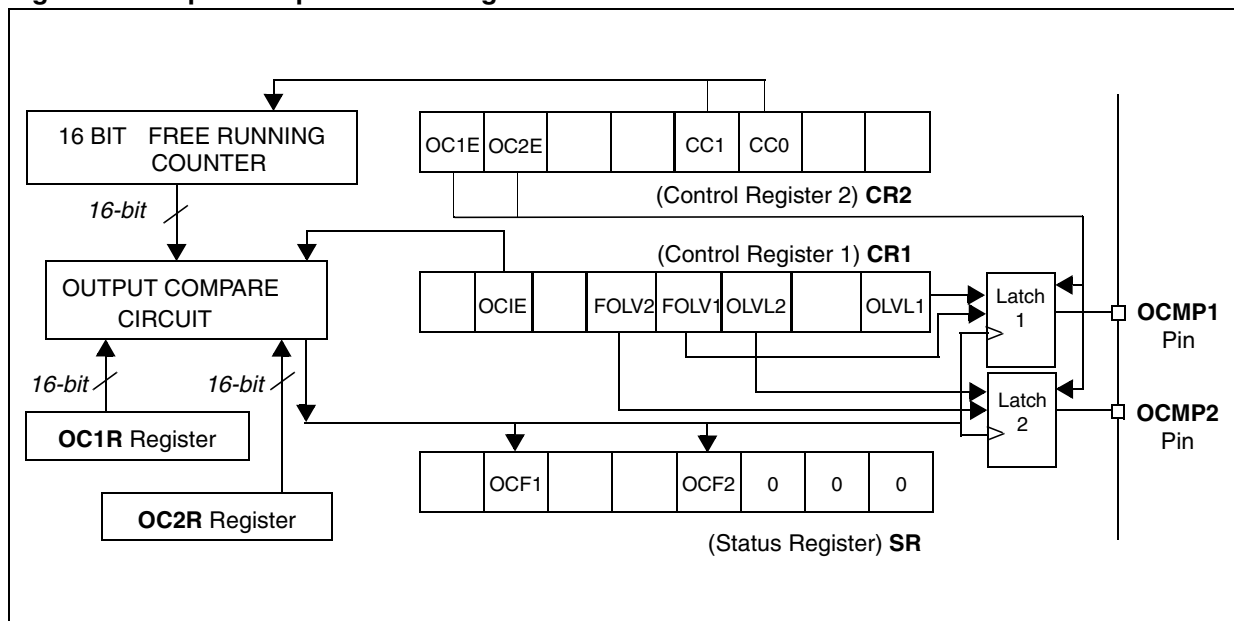
**16-BIT TIMER (Cont'd)****Notes:**

1. After a processor write cycle to the OCiHR register, the output compare function is inhibited until the OCiLR register is also written.
2. If the OCiE bit is not set, the OCMPi pin is a general I/O port and the OLVLi bit will not appear when a match is found but an interrupt could be generated if the OCiE bit is set.
3. In both internal and external clock modes, OCFi and OCMPi are set while the counter value equals the OCiR register value (see Figure 8 for an example with  $f_{CPU}/2$  and Figure 9 for an example with  $f_{CPU}/4$ ). This behavior is the same in OPM or PWM mode.
4. The output compare functions can be used both for generating external events on the OCMPi pins even if the input capture mode is also used.
5. The value in the 16-bit OCiR register and the OLVLi bit should be changed after each successful comparison in order to control an output waveform or establish a new elapsed timeout.

**Forced Compare Output capability**

When the FOLVi bit is set by software, the OLVLi bit is copied to the OCMPi pin. The OLVLi bit has to be toggled in order to toggle the OCMPi pin when it is enabled (OCiE bit = 1). The OCFi bit is then not set by hardware, and thus no interrupt request is generated.

The FOLVLi bits have no effect in both One Pulse mode and PWM mode.

**Figure 51. Output Compare Block Diagram**

**16-BIT TIMER (Cont'd)****10.4.4 Low Power Modes**

Mode	Description
WAIT	No effect on 16-bit Timer. Timer interrupts cause the device to exit from WAIT mode.
HALT	16-bit Timer registers are frozen. In HALT mode, the counter stops counting until Halt mode is exited. Counting resumes from the previous count when the MCU is woken up by an interrupt with “exit from HALT mode” capability or from the counter reset value when the MCU is woken up by a RESET. If an input capture event occurs on the ICAP <sub>i</sub> pin, the input capture detection circuitry is armed. Consequently, when the MCU is woken up by an interrupt with “exit from HALT mode” capability, the ICF <sub>i</sub> bit is set, and the counter value present when exiting from HALT mode is captured into the IC <sub>i</sub> R register.

**10.4.5 Interrupts**

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
Input Capture 1 event/Counter reset in PWM mode	ICF1	ICIE	Yes	No
Input Capture 2 event	ICF2			
Output Compare 1 event (not available in PWM mode)	OCF1	OCIE		
Output Compare 2 event (not available in PWM mode)	OCF2			
Timer Overflow event	TOF	TOIE		

**Note:** The 16-bit Timer interrupt events are connected to the same interrupt vector (see Interrupts chapter). These events generate an interrupt if the corresponding Enable Control Bit is set and the interrupt mask in the CC register is reset (RIM instruction).

**10.4.6 Summary of Timer Modes**

MODES	TIMER RESOURCES			
	Input Capture 1	Input Capture 2	Output Compare 1	Output Compare 2
Input Capture (1 and/or 2)	Yes	Yes	Yes	Yes
Output Compare (1 and/or 2)				
One Pulse Mode	No	Not Recommended <sup>1)</sup>	No	Partially <sup>2)</sup>
PWM Mode		Not Recommended <sup>3)</sup>		No

1) See note 4 in [Section 0.1.3.5 One Pulse Mode](#)

2) See note 5 in [Section 0.1.3.5 One Pulse Mode](#)

3) See note 4 in [Section 0.1.3.6 Pulse Width Modulation Mode](#)

**16-BIT TIMER (Cont'd)****CONTROL REGISTER 2 (CR2)**

Read/Write

Reset Value: 0000 0000 (00h)

7							0
OC1E	OC2E	OPM	PWM	CC1	CC0	IEDG2	EXEDG

Bit 7 = **OC1E** *Output Compare 1 Pin Enable*.

This bit is used only to output the signal from the timer on the OCMP1 pin (OLV1 in Output Compare mode, both OLV1 and OLV2 in PWM and one-pulse mode). Whatever the value of the OC1E bit, the Output Compare 1 function of the timer remains active.

0: OCMP1 pin alternate function disabled (I/O pin free for general-purpose I/O).

1: OCMP1 pin alternate function enabled.

Bit 6 = **OC2E** *Output Compare 2 Pin Enable*.

This bit is used only to output the signal from the timer on the OCMP2 pin (OLV2 in Output Compare mode). Whatever the value of the OC2E bit, the Output Compare 2 function of the timer remains active.

0: OCMP2 pin alternate function disabled (I/O pin free for general-purpose I/O).

1: OCMP2 pin alternate function enabled.

Bit 5 = **OPM** *One Pulse Mode*.

0: One Pulse mode is not active.

1: One Pulse mode is active, the ICAP1 pin can be used to trigger one pulse on the OCMP1 pin; the active transition is given by the IEDG1 bit. The length of the generated pulse depends on the contents of the OC1R register.

Bit 4 = **PWM** *Pulse Width Modulation*.

0: PWM mode is not active.

1: PWM mode is active, the OCMP1 pin outputs a programmable cyclic signal; the length of the pulse depends on the value of OC1R register; the period depends on the value of OC2R register.

Bit 3, 2 = **CC[1:0]** *Clock Control*.

The timer clock mode depends on these bits:

**Table 18. Clock Control Bits**

Timer Clock	CC1	CC0
$f_{CPU} / 4$	0	0
$f_{CPU} / 2$		1
$f_{CPU} / 8$	1	0
External Clock (where available)		1

**Note:** If the external clock pin is not available, programming the external clock configuration stops the counter.

Bit 1 = **IEDG2** *Input Edge 2*.

This bit determines which type of level transition on the ICAP2 pin will trigger the capture.

0: A falling edge triggers the capture.

1: A rising edge triggers the capture.

Bit 0 = **EXEDG** *External Clock Edge*.

This bit determines which type of level transition on the external clock pin EXTCLK will trigger the counter register.

0: A falling edge triggers the counter register.

1: A rising edge triggers the counter register.

**I<sup>2</sup>C BUS INTERFACE (Cont'd)**

Acknowledge may be enabled and disabled by software.

The I<sup>2</sup>C interface address and/or general call address can be selected by software.

The speed of the I<sup>2</sup>C interface may be selected between Standard (up to 100KHz) and Fast I<sup>2</sup>C (up to 400KHz).

**SDA/SCL Line Control**

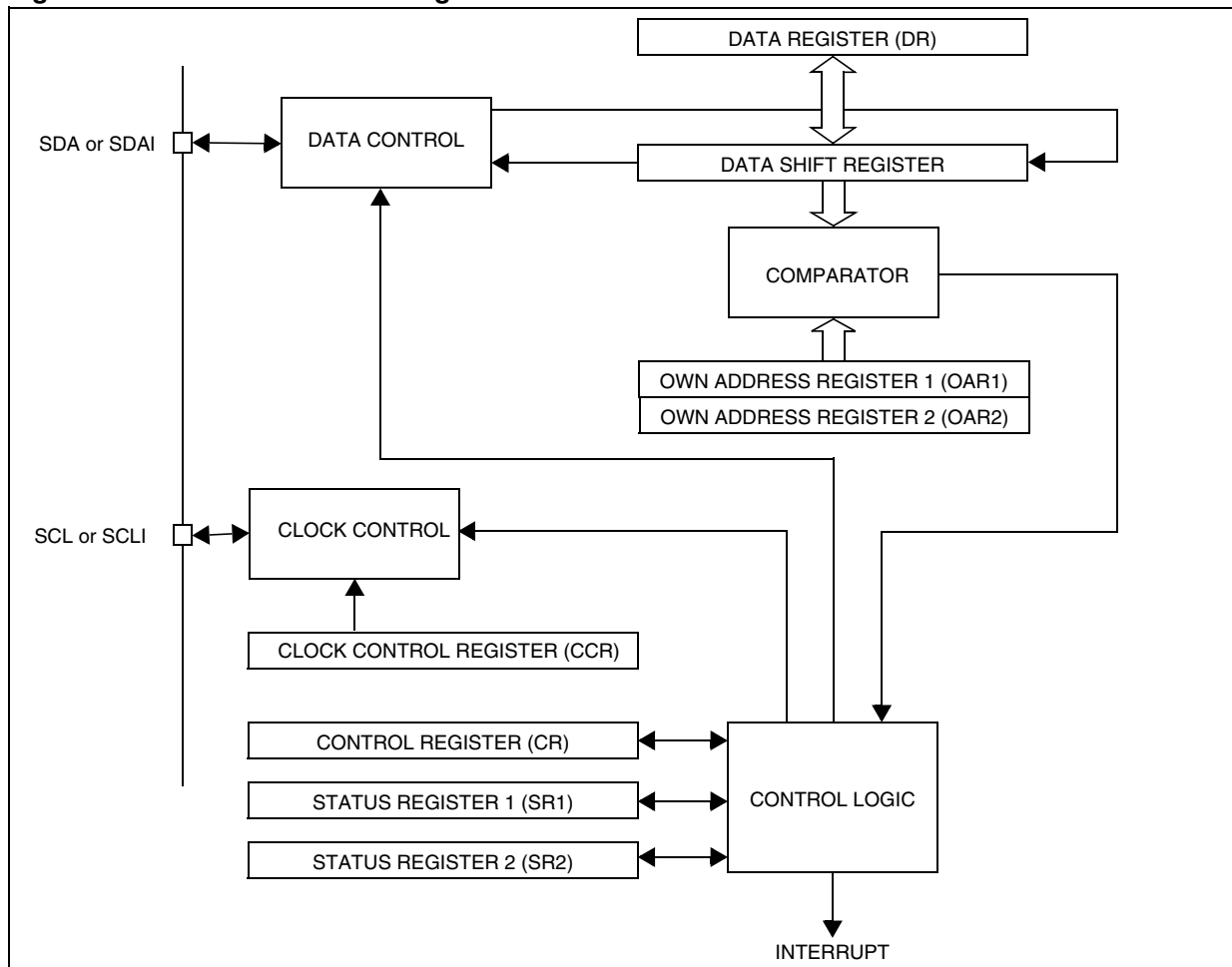
Transmitter mode: the interface holds the clock line low before transmission to wait for the microcontroller to write the byte in the Data Register.

Receiver mode: the interface holds the clock line low after reception to wait for the microcontroller to read the byte in the Data Register.

The SCL frequency ( $F_{SCL}$ ) is controlled by a programmable clock divider which depends on the I<sup>2</sup>C bus mode.

When the I<sup>2</sup>C cell is enabled, the SDA and SCL ports must be configured as floating inputs. In this case, the value of the external pull-up resistor used depends on the application.

When the I<sup>2</sup>C cell is disabled, the SDA and SCL ports revert to being standard I/O port pins.

**Figure 68. I<sup>2</sup>C Interface Block Diagram**

**I<sup>2</sup>C BUS INTERFACE** (Cont'd)

Bit 1 = **M/SL** Master/Slave.

This bit is set by hardware as soon as the interface is in Master mode (writing START=1). It is cleared by hardware after detecting a Stop condition on the bus or a loss of arbitration (ARLO=1). It is also cleared when the interface is disabled (PE=0).

0: Slave mode

1: Master mode

Bit 0 = **SB** Start bit (Master mode).

This bit is set by hardware as soon as the Start condition is generated (following a write START=1). An interrupt is generated if ITE=1. It is cleared by software reading SR1 register followed by writing the address byte in DR register. It is also cleared by hardware when the interface is disabled (PE=0).

0: No Start condition

1: Start condition generated

**I<sup>2</sup>C STATUS REGISTER 2 (SR2)**

Read Only

Reset Value: 0000 0000 (00h)

7			0				
0	0	0	AF	STOPF	ARLO	BERR	GCAL

Bit 7:5 = Reserved. Forced to 0 by hardware.

Bit 4 = **AF** Acknowledge failure.

This bit is set by hardware when no acknowledge is returned. An interrupt is generated if ITE=1. It is cleared by software reading SR2 register or by hardware when the interface is disabled (PE=0).

The SCL line is not held low while AF=1 but by other flags (SB or BTF) that are set at the same time.

0: No acknowledge failure

1: Acknowledge failure

Note:

- When an AF event occurs, the SCL line is not held low; however, the SDA line can remain low if the last bits transmitted are all 0. It is then necessary to release both lines by software.

Bit 3 = **STOPF** Stop detection (Slave mode).

This bit is set by hardware when a Stop condition is detected on the bus after an acknowledge (if ACK=1). An interrupt is generated if ITE=1. It is cleared by software reading SR2 register or by hardware when the interface is disabled (PE=0).

The SCL line is not held low while STOPF=1.

0: No Stop condition detected

1: Stop condition detected

Bit 2 = **ARLO** Arbitration lost.

This bit is set by hardware when the interface loses the arbitration of the bus to another master. An interrupt is generated if ITE=1. It is cleared by software reading SR2 register or by hardware when the interface is disabled (PE=0).

After an ARLO event the interface switches back automatically to Slave mode (M/SL=0).

The SCL line is not held low while ARLO=1.

0: No arbitration lost detected

1: Arbitration lost detected

Note:

- In a Multimaster environment, when the interface is configured in Master Receive mode it does not perform arbitration during the reception of the Acknowledge Bit. Mishandling of the ARLO bit from the I2CSR2 register may occur when a second master simultaneously requests the same data from the same slave and the I<sup>2</sup>C master does not acknowledge the data. The ARLO bit is then left at 0 instead of being set.

Bit 1 = **BERR** Bus error.

This bit is set by hardware when the interface detects a misplaced Start or Stop condition. An interrupt is generated if ITE=1. It is cleared by software reading SR2 register or by hardware when the interface is disabled (PE=0).

The SCL line is not held low while BERR=1.

0: No misplaced Start or Stop condition

1: Misplaced Start or Stop condition

Note:

- If a Bus Error occurs, a Stop or a repeated Start condition should be generated by the Master to re-synchronize communication, get the transmission acknowledged and the bus released for further communication

Bit 0 = **GCAL** General Call (Slave mode).

This bit is set by hardware when a general call address is detected on the bus while ENGC=1. It is cleared by hardware detecting a Stop condition (STOPF=1) or when the interface is disabled (PE=0).

0: No general call address detected on bus

1: general call address detected on bus

## 10.8 10-BIT A/D CONVERTER (ADC)

### 10.8.1 Introduction

The on-chip Analog to Digital Converter (ADC) peripheral is a 10-bit, successive approximation converter with internal sample and hold circuitry. This peripheral has up to 16 multiplexed analog input channels (refer to device pin out description) that allow the peripheral to convert the analog voltage levels from up to 16 different sources.

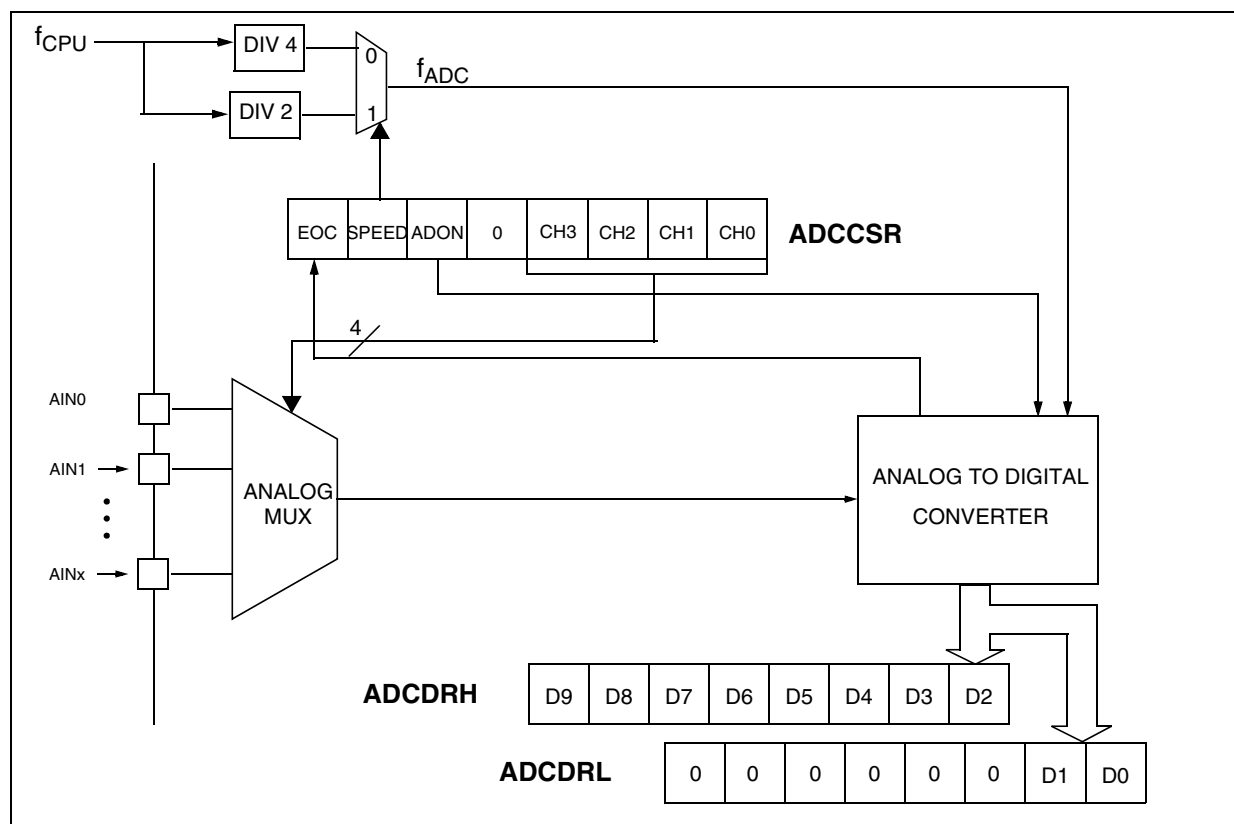
The result of the conversion is stored in a 10-bit Data Register. The A/D converter is controlled through a Control/Status Register.

### 10.8.2 Main Features

- 10-bit conversion
- Up to 16 channels with multiplexed input
- Linear successive approximation
- Data register (DR) which contains the results
- Conversion complete status flag
- On/off bit (to reduce consumption)

The block diagram is shown in [Figure 71](#).

**Figure 71. ADC Block Diagram**



**SUPPLY CURRENT CHARACTERISTICS (Cont'd)****12.4.3 On-Chip Peripherals**

Measured on LQFP64 generic board  $T_A = 25^\circ\text{C}$   $f_{\text{CPU}}=4\text{MHz}$ .

Symbol	Parameter	Conditions	Typ	Unit
$I_{\text{DD(TIM)}}$	16-bit Timer supply current <sup>1)</sup>	$V_{\text{DD}}=5.0\text{V}$	50	$\mu\text{A}$
$I_{\text{DD(ART)}}$	ART PWM supply current <sup>2)</sup>	$V_{\text{DD}}=5.0\text{V}$	75	$\mu\text{A}$
$I_{\text{DD(SPI)}}$	SPI supply current <sup>3)</sup>	$V_{\text{DD}}=5.0\text{V}$	400	$\mu\text{A}$
$I_{\text{DD(SCI)}}$	SCI supply current <sup>4)</sup>	$V_{\text{DD}}=5.0\text{V}$	400	$\mu\text{A}$
$I_{\text{DD(I2C)}}$	I2C supply current <sup>5)</sup>	$V_{\text{DD}}=5.0\text{V}$	175	$\mu\text{A}$
$I_{\text{DD(ADC)}}$	ADC supply current when converting <sup>6)</sup>	$V_{\text{DD}}=5.0\text{V}$	400	$\mu\text{A}$

**Notes:**

1. Data based on a differential  $I_{\text{DD}}$  measurement between reset configuration (timer counter running at  $f_{\text{CPU}}/4$ ) and timer counter stopped (only TIMD bit set). Data valid for one timer.
2. Data based on a differential  $I_{\text{DD}}$  measurement between reset configuration (timer stopped) and timer counter enabled (only TCE bit set).
3. Data based on a differential  $I_{\text{DD}}$  measurement between reset configuration (SPI disabled) and a permanent SPI master communication at maximum speed (data sent equal to 55h). This measurement includes the pad toggling consumption.
4. Data based on a differential  $I_{\text{DD}}$  measurement between SCI low power state (SCID=1) and a permanent SCI data transmit sequence.
5. Data based on a differential  $I_{\text{DD}}$  measurement between reset configuration (I2C disabled) and a permanent I2C master communication at 100kHz (data sent equal to 55h). This measurement include the pad toggling consumption (27kOhm external pull-up on clock and data lines).
6. Data based on a differential  $I_{\text{DD}}$  measurement between reset configuration and continuous A/D conversions.



## 12.9 CONTROL PIN CHARACTERISTICS

### 12.9.1 Asynchronous $\overline{\text{RESET}}$ Pin

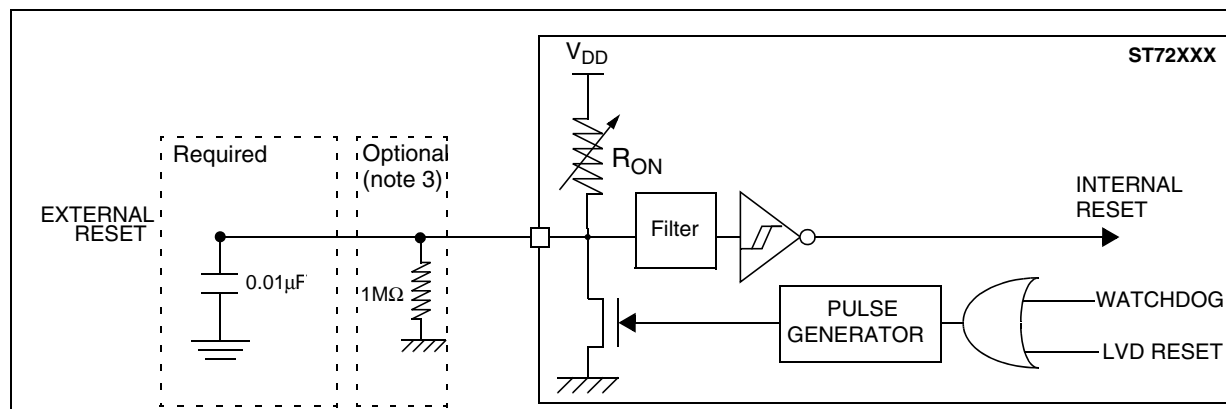
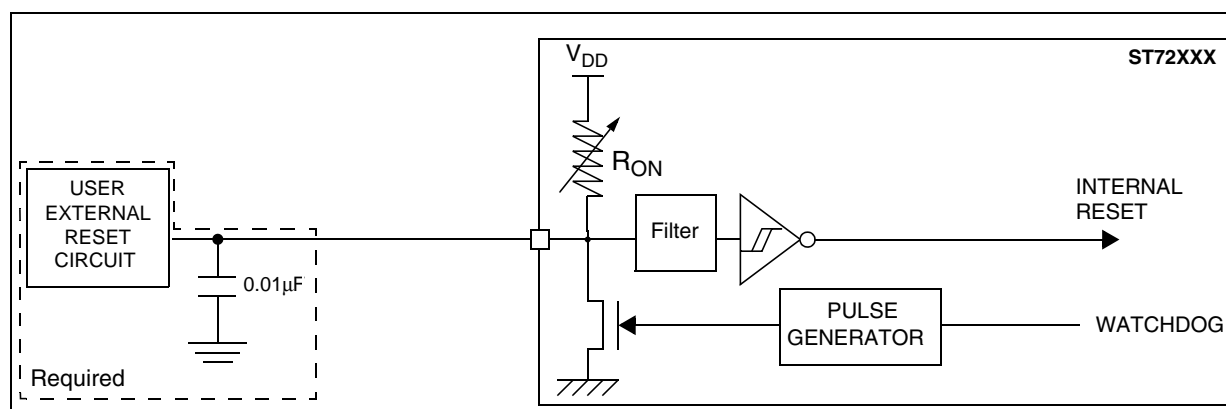
Subject to general operating conditions for  $V_{DD}$ ,  $f_{CPU}$ , and  $T_A$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL}$	Input low level voltage <sup>1)</sup>				$0.3 \times V_{DD}$	V
$V_{IH}$	Input high level voltage <sup>1)</sup>		$0.7 \times V_{DD}$			
$V_{hys}$	Schmitt trigger voltage hysteresis <sup>2)</sup>			2.5		V
$V_{OL}$	Output low level voltage <sup>3)</sup>	$V_{DD}=5V$   $I_{IO}=+2mA$		0.2	0.5	
$I_{IO}$	Input current on $\overline{\text{RESET}}$ pin			2		mA
$R_{ON}$	Weak pull-up equivalent resistor		20	30	120	k $\Omega$
$t_{w(RSTL)out}$	Generated reset pulse duration	Stretch applied on external pulse	0		$42^{6)}$	$\mu s$
		Internal reset sources	20	30	$42^{6)}$	$\mu s$
$t_{h(RSTL)in}$	External reset pulse hold time <sup>4)</sup>		2.5			$\mu s$
$t_{g(RSTL)in}$	Filtered glitch duration <sup>5)</sup>			200		ns

#### Notes:

1. Data based on characterization results, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels.
3. The  $I_{IO}$  current sunk must always respect the absolute maximum rating specified in [Section 12.2.2](#) and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $I_{VSS}$ .
4. To guarantee the reset of the device, a minimum pulse has to be applied to the  $\overline{\text{RESET}}$  pin. All short pulses applied on the  $\overline{\text{RESET}}$  pin with a duration below  $t_{h(RSTL)in}$  can be ignored.
5. The reset network (the resistor and two capacitors) protects the device against parasitic resets, especially in noisy environments.
6. Data guaranteed by design, not tested in production.

## CONTROL PIN CHARACTERISTICS (Cont'd)

Figure 87. RESET pin protection when LVD is enabled.<sup>1)2)3)4)</sup>Figure 88. RESET pin protection when LVD is disabled.<sup>1)</sup>**Note 1:**

- The reset network protects the device against parasitic resets.
- The output of the external reset circuit must have an open-drain output to drive the ST7 reset pad. Otherwise the device can be damaged when the ST7 generates an internal reset (LVD or watchdog).
- Whatever the reset source is (internal or external), the user must ensure that the level on the  $\overline{\text{RESET}}$  pin can go below the  $V_{IL}$  max. level specified in [section 12.9.1 on page 162](#). Otherwise the reset will not be taken into account internally.
- Because the reset circuit is designed to allow the internal RESET to be output in the  $\overline{\text{RESET}}$  pin, the user must ensure that the current sunk on the RESET pin is less than the absolute maximum value specified for  $I_{INJ}(\text{RESET})$  in [section 12.2.2 on page 143](#).

**Note 2:** When the LVD is enabled, it is recommended not to connect a pull-up resistor or capacitor. A 10nF pull-down capacitor is required to filter noise on the reset line.

**Note 3:** In case a capacitive power supply is used, it is recommended to connect a 1MΩ pull-down resistor to the  $\overline{\text{RESET}}$  pin to discharge any residual voltage induced by the capacitive effect of the power supply (this will add 5µA to the power consumption of the MCU).

**Note 4:** Tips when using the LVD:

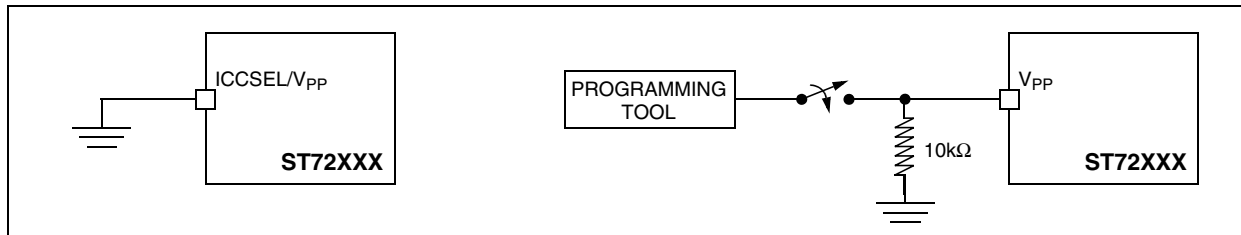
1. Check that all recommendations related to reset circuit have been applied (see notes above).
2. Check that the power supply is properly decoupled (100nF + 10µF close to the MCU). Refer to AN1709 and AN2017. If this cannot be done, it is recommended to put a 100nF + 1MΩ pull-down on the RESET pin.
3. The capacitors connected on the RESET pin and also the power supply are key to avoid any start-up marginality. In most cases, steps 1 and 2 above are sufficient for a robust solution. Otherwise: replace 10nF pull-down on the RESET pin with a 5µF to 20µF capacitor.

**CONTROL PIN CHARACTERISTICS (Cont'd)****12.9.2 ICCSEL/V<sub>PP</sub> Pin**

Subject to general operating conditions for  $V_{DD}$ ,  $f_{CPU}$ , and  $T_A$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max <sup>1</sup>	Unit
$I_L$	Input leakage current	$V_{IN}=V_{SS}$		$\pm 1$	$\mu A$

**Figure 89. Two typical Applications with ICCSEL/V<sub>PP</sub> Pin <sup>2)</sup>**

**Notes:**

1. Data based on design simulation and/or technology characteristics, not tested in production.
2. When ICC mode is not required by the application ICCSEL/V<sub>PP</sub> pin must be tied to  $V_{SS}$ .

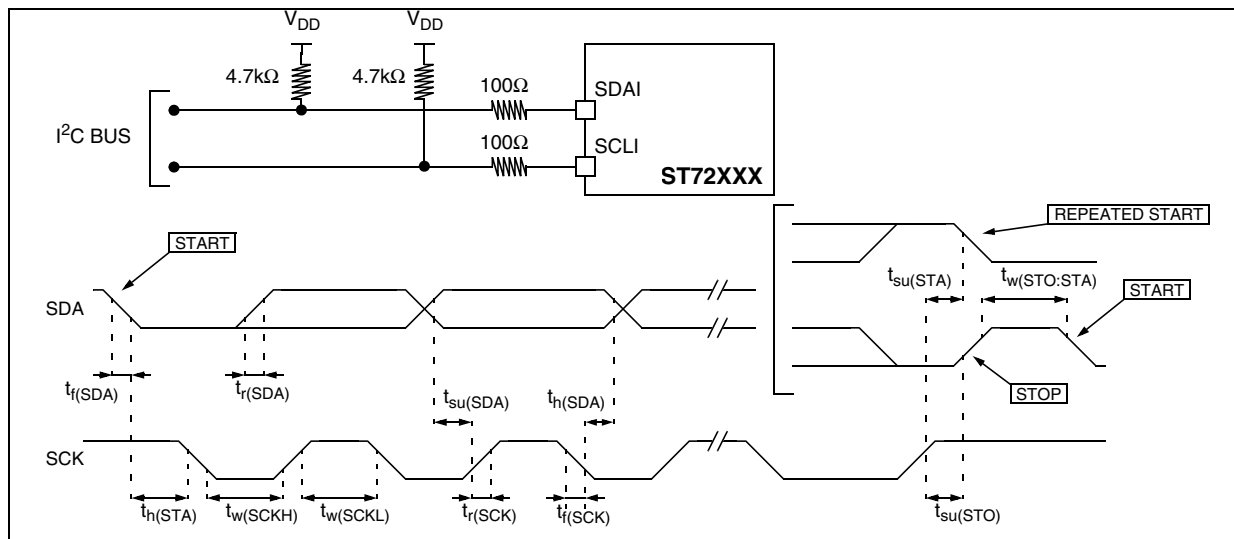
## COMMUNICATION INTERFACE CHARACTERISTICS (Cont'd)

12.11.2 I<sup>2</sup>C - Inter IC Control Interface

Subject to general operating conditions for  $V_{DD}$ ,  $f_{CPU}$ , and  $T_A$  unless otherwise specified.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDAI and SCLI). The ST7 I<sup>2</sup>C interface meets the requirements of the Standard I<sup>2</sup>C communication protocol described in the following table.

Symbol	Parameter	Standard mode I <sup>2</sup> C		Fast mode I <sup>2</sup> C <sup>5)</sup>		Unit
		Min <sup>1)</sup>	Max <sup>1)</sup>	Min <sup>1)</sup>	Max <sup>1)</sup>	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		$\mu s$
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_h(SDA)$	SDA data hold time	0 <sup>3)</sup>		0 <sup>2)</sup>	900 <sup>3)</sup>	
$t_r(SDA)$ $t_r(SCL)$	SDA and SCL rise time		1000	$20+0.1C_b$	300	
$t_f(SDA)$ $t_f(SCL)$	SDA and SCL fall time		300	$20+0.1C_b$	300	
$t_h(STA)$	START condition hold time	4.0		0.6		$\mu s$
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		$\mu s$
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		$\mu s$
$C_b$	Capacitive load for each bus line		400		400	pF

Figure 93. Typical Application with I<sup>2</sup>C Bus and Timing Diagram <sup>4)</sup>

## Notes:

1. Data based on standard I<sup>2</sup>C protocol requirement, not tested in production.
2. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
3. The maximum hold time of the START condition has only to be met if the interface does not stretch the low period of SCL signal.
4. Measurement points are done at CMOS levels:  $0.3 \times V_{DD}$  and  $0.7 \times V_{DD}$ .
5. At 4MHz  $f_{CPU}$ , max. I<sup>2</sup>C speed (400kHz) is not achievable. In this case, max. I<sup>2</sup>C speed will be approximately 260kHz.

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