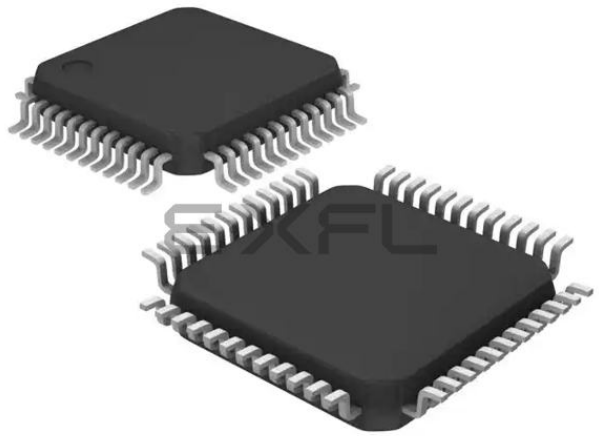


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f325s6t6

Pin n°					Pin Name	Type	Level		Port						Main function (after reset)	Alternate function	
									Input				Output				
LQFP64	LQFP48C	LQFP48S	LQFP44	SDIP42			Input	Output	float	wpu	int	ana	OD	PP			
17	13	13	11	6	PD4/AIN4	I/O	C_T		X	X		X	X	X	Port D4	ADC Analog Input 4	
18	14	14	12	7	PD5/AIN5	I/O	C_T		X	X		X	X	X	Port D5	ADC Analog Input 5	
19	-[4]	-	-	-	PD6/AIN6	I/O	C_T		X	X		X	X	X	Port D6	ADC Analog Input 6	
20	-[4]	-	-	-	PD7/AIN7	I/O	C_T		X	X		X	X	X	Port D7	ADC Analog Input 7	
21	15	15	13	8	V_{AREF}[6]	I									Analog Reference Voltage for ADC		
22	16	16	14	9	V_{SSA}[6]	S									Analog Ground Voltage		
23	-	-	-	-	V_{DD_3}[6]	S									Digital Main Supply Voltage		
24	-	-	-	-	V_{SS_3}[6]	S									Digital Ground Voltage		
25	17	17	15	10	PF0/MCO/AIN8	I/O	C_T		X	ei1		X	X	X	Port F0	Main clock out (f_{OSC}/2)	ADC Analog Input 8
26	18	18	16	11	PF1 (HS)/BEEP	I/O	C_T	HS	X	ei1			X	X	Port F1	Beep signal output	
27	19	19	17	12	PF2 (HS)	I/O	C_T	HS	X		ei1		X	X	Port F2		
28	-[4]	-	-	-	PF3/OCMP2_A/ AIN9	I/O	C_T		X	X		X	X	X	Port F3	Timer A Output Compare 2	ADC Analog Input 9
29	20	20	18	13	PF4/OCMP1_A/ AIN10	I/O	C_T		X	X		X	X	X	Port F4	Timer A Output Compare 1	ADC Analog Input 10
30	-[4]	-	-	-	PF5/ICAP2_A/ AIN11	I/O	C_T		X	X		X	X	X	Port F5	Timer A Input Capture 2	ADC Analog Input 11
31	21	21	19	14	PF6 (HS)/ICAP1_A	I/O	C_T	HS	X	X			X	X	Port F6	Timer A Input Capture 1	
32	22	22	20	15	PF7 (HS)/ EXTCLK_A	I/O	C_T	HS	X	X			X	X	Port F7	Timer A External Clock Source	
33	23	23	21	-	V_{DD_0}[6]	S									Digital Main Supply Voltage		
34	24	24	22	-	V_{SS_0}[6]	S									Digital Ground Voltage		
35	25	25	23	16	PC0/OCMP2_B/ AIN12	I/O	C_T		X	X		X	X	X	Port C0	Timer B Output Compare 2	ADC Analog Input 12
36	26	26	24	17	PC1/OCMP1_B/ AIN13	I/O	C_T		X	X		X	X	X	Port C1	Timer B Output Compare 1	ADC Analog Input 13
37	27	27	25	18	PC2 (HS)/ICAP2_B	I/O	C_T	HS	X	X			X	X	Port C2	Timer B Input Capture 2	
38	28	28	26	19	PC3 (HS)/ICAP1_B	I/O	C_T	HS	X	X			X	X	Port C3	Timer B Input Capture 1	
39	29	29	27	20	PC4/MISO/ICCDATA	I/O	C_T		X	X			X	X	Port C4	SPI Master In / Slave Out Data	ICC Data Input
40	30	30	28	21	PC5/MOSI/AIN14	I/O	C_T		X	X		X	X	X	Port C5	SPI Master Out / Slave In Data	ADC Analog Input 14
41	31	31	29	22	PC6/SCK/ICCCLK	I/O	C_T		X	X			X	X	Port C6	SPI Serial Clock	ICC Clock Output

POWER SAVING MODES (Cont'd)

8.4.2 HALT MODE

The HALT mode is the lowest power consumption mode of the MCU. It is entered by executing the 'HALT' instruction when the OIE bit of the Main Clock Controller Status register (MCCSR) is cleared (see section 10.2 on page 61 for more details on the MCCSR register).

The MCU can exit HALT mode on reception of either a specific interrupt (see Table 9, "Interrupt Mapping," on page 41) or a RESET. When exiting HALT mode by means of a RESET or an interrupt, the oscillator is immediately turned on and the 256 or 4096 CPU cycle delay is used to stabilize the oscillator. After the start up delay, the CPU resumes operation by servicing the interrupt or by fetching the reset vector which woke it up (see Figure 32).

When entering HALT mode, the I[1:0] bits in the CC register are forced to '10b'to enable interrupts. Therefore, if an interrupt is pending, the MCU wakes up immediately.

In HALT mode, the main oscillator is turned off causing all internal processing to be stopped, including the operation of the on-chip peripherals. All peripherals are not clocked except the ones which get their clock supply from another clock generator (such as an external or auxiliary oscillator).

The compatibility of Watchdog operation with HALT mode is configured by the "WDGHALT" option bit of the option byte. The HALT instruction when executed while the Watchdog system is enabled, can generate a Watchdog RESET (see section 14.1 on page 181 for more details).

Figure 31. HALT Timing Overview

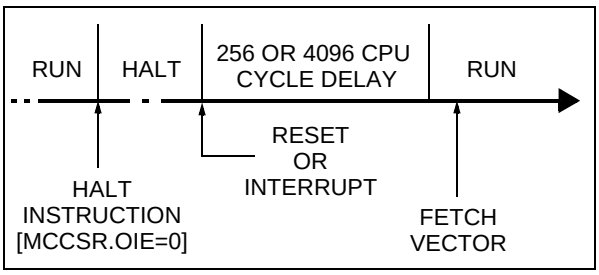
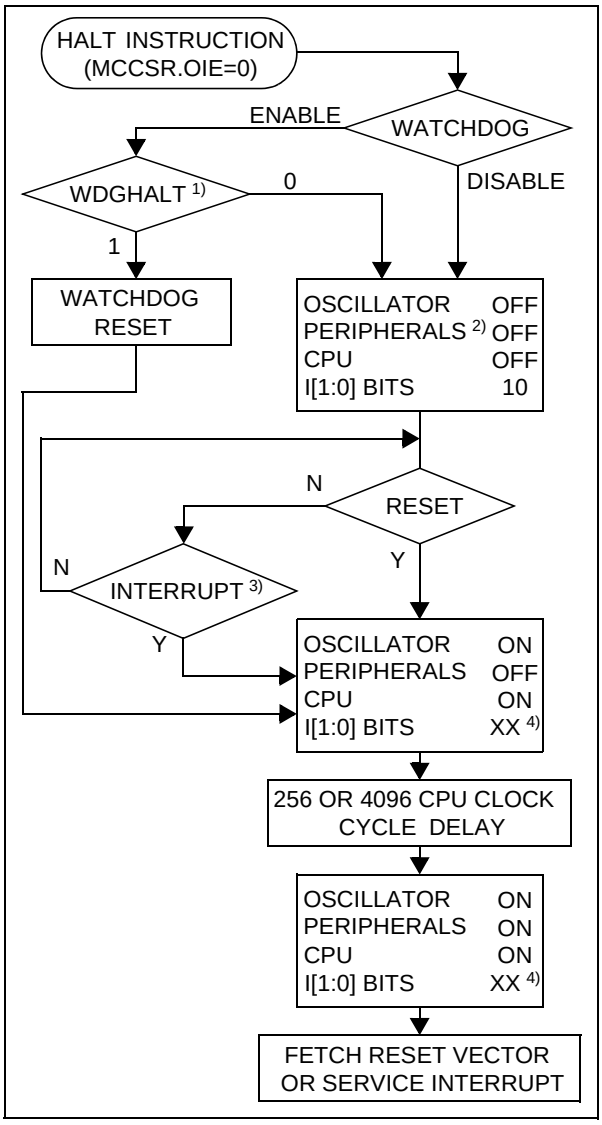


Figure 32. HALT Mode Flow-chart



Notes:

1. WDGHALT is an option bit. See option byte section for more details.
2. Peripheral clocked with an external clock source can still be active.
3. Only some specific interrupts can exit the MCU from HALT mode (such as external interrupt). Refer to Table 9, "Interrupt Mapping," on page 41 for more details.
4. Before servicing an interrupt, the CC register is pushed on the stack. The I[1:0] bits of the CC register are set to the current software priority level of the interrupt routine and recovered when the CC register is popped.

ON-CHIP PERIPHERALS (Cont'd)

10.3.2 Functional Description

Counter

The free running 8-bit counter is fed by the output of the prescaler, and is incremented on every rising edge of the clock signal.

It is possible to read or write the contents of the counter on the fly by reading or writing the Counter Access register (ARTCAR).

When a counter overflow occurs, the counter is automatically reloaded with the contents of the ARTARR register (the prescaler is not affected).

Counter clock and prescaler

The counter clock frequency is given by:

$$f_{COUNTER} = f_{INPUT} / 2^{CC[2:0]}$$

The timer counter's input clock (f_{INPUT}) feeds the 7-bit programmable prescaler, which selects one of the 8 available taps of the prescaler, as defined by CC[2:0] bits in the Control/Status Register (ARTCSR). Thus the division factor of the prescaler can be set to 2^n (where n = 0, 1,..7).

This f_{INPUT} frequency source is selected through the EXCL bit of the ARTCSR register and can be either the f_{CPU} or an external input frequency f_{EXT}.

The clock input to the counter is enabled by the TCE (Timer Counter Enable) bit in the ARTCSR register. When TCE is reset, the counter is stopped and the prescaler and counter contents are frozen. When TCE is set, the counter runs at the rate of the selected clock source.

Counter and Prescaler Initialization

After RESET, the counter and the prescaler are cleared and $f_{INPUT} = f_{CPU}$.

The counter can be initialized by:

– Writing to the ARTARR register and then setting the FCRL (Force Counter Re-Load) and the TCE (Timer Counter Enable) bits in the ARTCSR register.

– Writing to the ARTCAR counter access register,

In both cases the 7-bit prescaler is also cleared, whereupon counting will start from a known value.

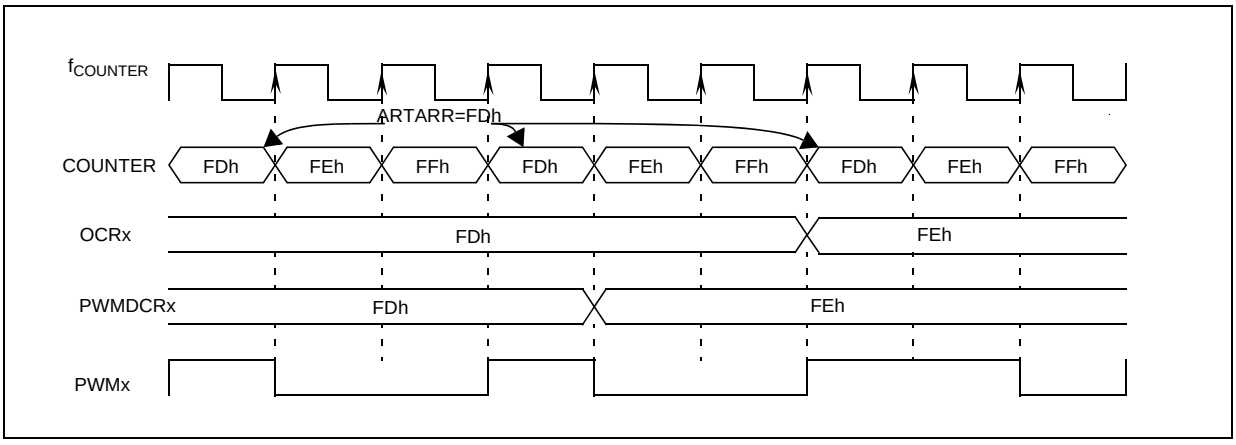
Direct access to the prescaler is not possible.

Output compare control

The timer compare function is based on four different comparisons with the counter (one for each PWMx output). Each comparison is made between the counter value and an output compare register (OCRx) value. This OCRx register can not be accessed directly, it is loaded from the duty cycle register (PWMDCRx) at each overflow of the counter.

This double buffering method avoids glitch generation when changing the duty cycle on the fly.

Figure 40. Output compare control



ON-CHIP PERIPHERALS (Cont'd)

INPUT CAPTURE
CONTROL / STATUS REGISTER (ARTICCSR)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
0	0	CS2	CS1	CIE2	CIE1	CF2	CF1

Bit 7:6 = Reserved, always read as 0.

Bit 5:4 = CS[2:1] *Capture Sensitivity*
These bits are set and cleared by software. They determine the trigger event polarity on the corresponding input capture channel.
0: Falling edge triggers capture on channel x.
1: Rising edge triggers capture on channel x.

Bit 3:2 = CIE[2:1] *Capture Interrupt Enable*
These bits are set and cleared by software. They enable or disable the Input capture channel interrupts independently.
0: Input capture channel x interrupt disabled.
1: Input capture channel x interrupt enabled.

Bit 1:0 = CF[2:1] *Capture Flag*
These bits are set by hardware and cleared by software reading the corresponding ARTICRx register. Each CFx bit indicates that an input capture x has occurred.
0: No input capture on channel x.
1: An input capture has occurred on channel x.

INPUT CAPTURE REGISTERS (ARTICRx)

Read only

Reset Value: 0000 0000 (00h)

7							0
IC7	IC6	IC5	IC4	IC3	IC2	IC1	IC0

Bit 7:0 = IC[7:0] *Input Capture Data*

These read only bits are set and cleared by hardware. An ARTICRx register contains the 8-bit auto-reload counter value transferred by the input capture channel x event.

16-BIT TIMER (Cont'd)

Figure 49. Input Capture Block Diagram

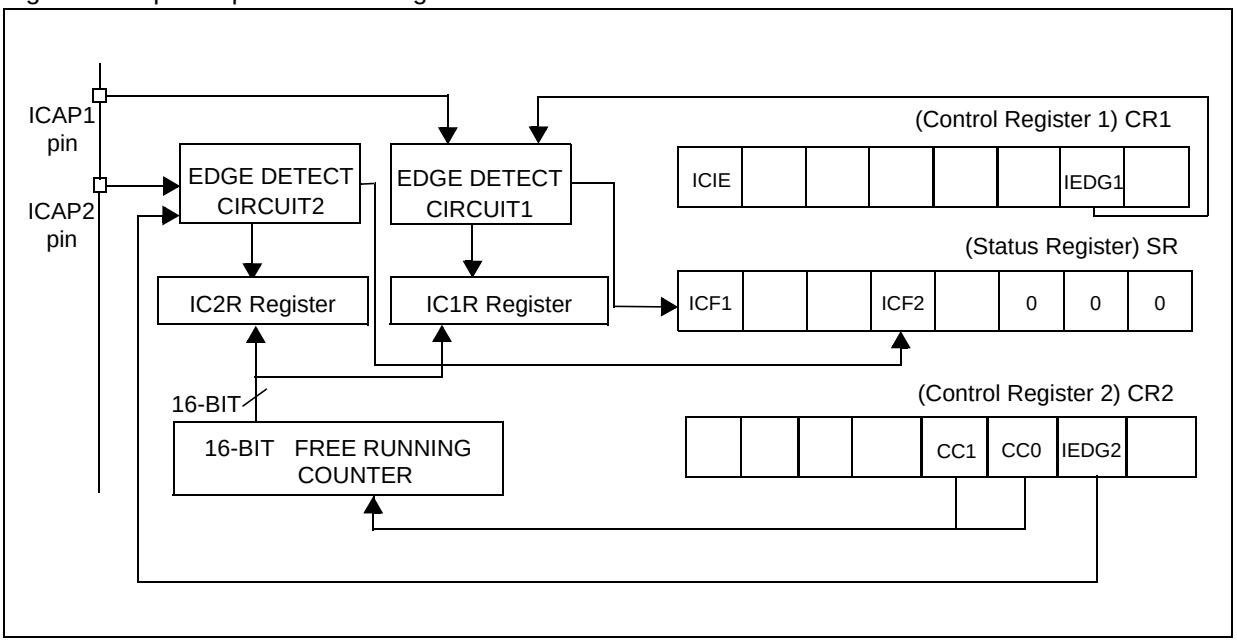
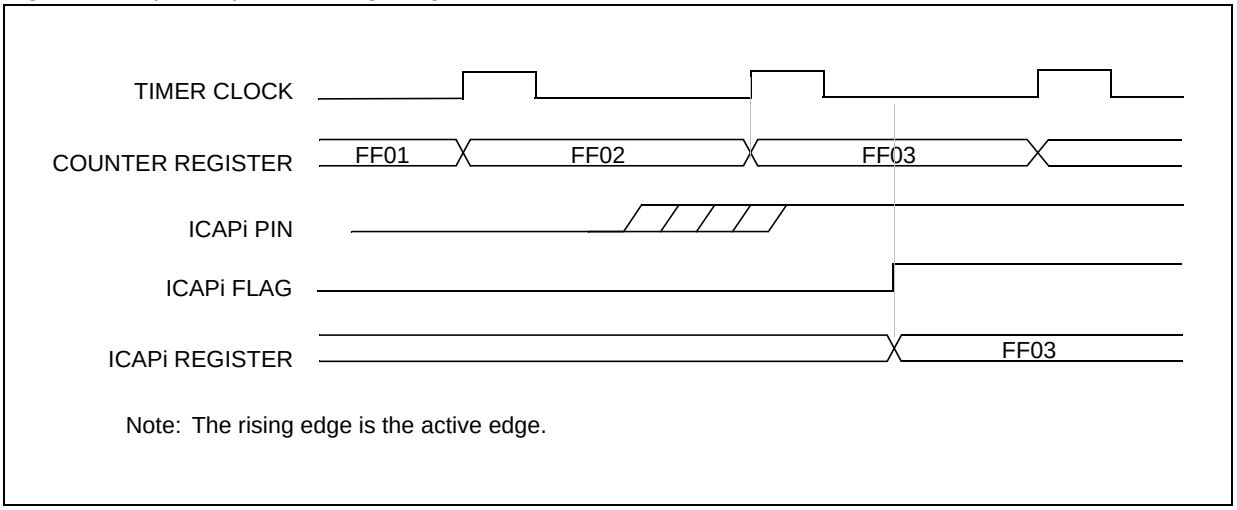


Figure 50. Input Capture Timing Diagram



Note: The rising edge is the active edge.

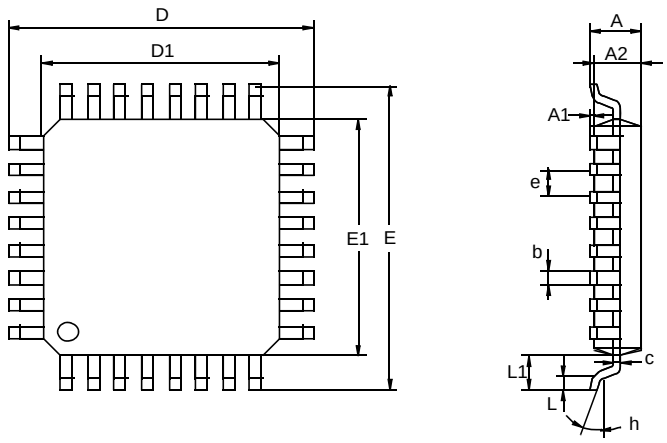
16-BIT TIMER (Cont'd)

Notes:

1. After a processor write cycle to the OC*i*HR register, the output compare function is inhibited until the OC*i*LR register is also written.
2. If the OC*i*E bit is not set, the OCMP*i* pin is a general I/O port and the OLVL*i* bit will not appear when a match is found but an interrupt could be generated if the OCIE bit is set.
3. In both internal and external clock modes, OCFi and OCMPi are set while the counter value equals the OCiR register value (see Figure 8 for an example with $f_{CPU}/2$ and Figure 9 for an example with $f_{CPU}/4$). This behavior is the same in OPM or PWM mode.
4. The output compare functions can be used both for generating external events on the OCMP*i* pins even if the input capture mode is also used.
5. The value in the 16-bit OC*i*R register and the OLV*i* bit should be changed after each successful comparison in order to control an o 0 Tw 5.4]TJ23 TD .003n or.7(h4.8(is(r) -.0018 Te)]TJ -13.8.1(i(te)OF1 1 T

PACKAGE MECHANICAL DATA (Cont'd)

Figure 105. 32-Pin Low Profile Quad Flat Package



Dim.	mm			inches [1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.30	0.37	0.45	0.0118	0.0146	0.0177
C	0.09		0.20	0.0035		0.0079
D		9.00			0.3543	
D1		7.00			0.2756	
E		9.00			0.3543	
E1		7.00			0.2756	
e		0.80			0.0315	
	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
	Number of Pins					
N	32					

Note 1. Values in inches are converted from mm and rounded to 4 decimal digits.