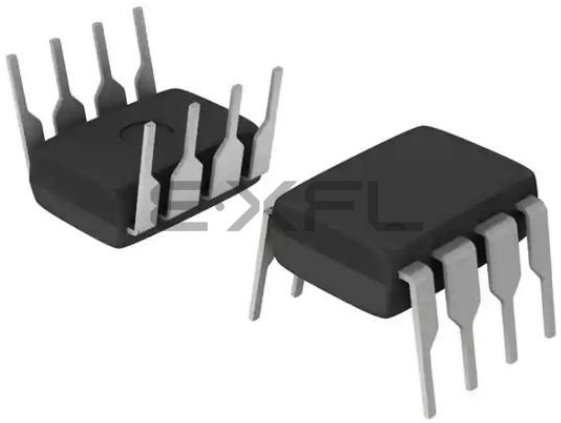

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ACE1502
Core Size	8-Bit
Speed	25MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	6
Program Memory Size	1KB (1K x 8)
Program Memory Type	EEPROM
EEPROM Size	64 x 8
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.400", 10.16mm)
Supplier Device Package	8-DIP
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/ace1501en

2. Electrical Characteristics

Absolute Maximum Ratings

Ambient Storage Temperature	-65 °C to +150 °C
Input Voltage	-0.3V to V_{CC} + 0.3V
Lead Temperature (10s max)	+300°C
Electrostatic Discharge on all pins	2000V min

Operating Conditions

Relative Humidity (non-condensing)	95%
EEPROM write limits	See DC Electrical Characteristics

Part Number	Operating Voltage	Ambient Operating Temperature
ACE1501E	1.8 to 3.6V	-40°C to +85°C
ACE1501V	1.8 to 3.6V	-40°C to +125°C

ACE1501 DC Electrical Characteristics, V_{CC} = 1.8 to 3.6V

All measurements are valid for ambient operating temperature unless otherwise stated.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
Icc[3]	Suppy Current - no data EEPROM write in progress	1.8V 2.2V 2.7V 3.6V		0.4 0.4 0.5 0.6	0.6 0.6 0.7 1.0	mA mA mA mA
Icc_H	HALT Mode current	2.7V @ 25°C 2.7V @ -40°C to +85°C		 100	400 5000	nA nA
		3.6V @ 25°C 3.6V @ -40°C to +85°C		 0.25	1000 10	nA µA
Icc_L[4]	IDLE Mode current	1.8V 3.6V		210 250	 400	µA µA
Vcc_W	EEPROM write voltage	Code EEPROM in Programming Mode Data EEPROM in Operating Mode	3.0 1.8	3.3	3.6 3.6	V V
S_{Vcc}	Power Supply Slope		1µs/V		10ms/V	
V_{IL}	Input Low with Schmitt Trigger buffer	Vcc = 2.2 - 3.6V			0.2Vcc	V
		Vcc < 2.2V			0.15Vcc	V
V_{IH}	Input High with Schmitt Trigger buffer	Vcc = 1.8 - 3.6V	0.8Vcc			V
I_{IP}	Input Pull-up Current	Vcc = 3.6V, V_{IN} = 0V	30	65	350	µA
I_{TL}	Tri-State Leakage	Vcc = 3.6V		2	200	nA
V_{OL}	Output Low Voltage: G0, G1, G2, G3, G4, G5, G6, G7	Vcc = 1.8 - 2.7V 2 mA sink			0.2Vcc	V
	Output Low Voltage: G0, G1, G2, G3, G4, G5, G6, G7	Vcc = 3.3 - 3.6V 7.0 mA sink			0.2Vcc	V
V_{OH}	Output High Voltage: G0, G1, G2, G3, G4, G5, G6, G7	Vcc = 2.2 - 2.7V 2 mA source	0.8Vcc			V
	Output High Voltage: G0, G1, G2, G3, G4, G5, G6, G7	Vcc = 3.3 - 3.6V 7 mA source	0.8Vcc			V

3. Icc active current is dependant on the program code.
4. Based on a continuous IDLE looping program.

Figure 8. Icc Active

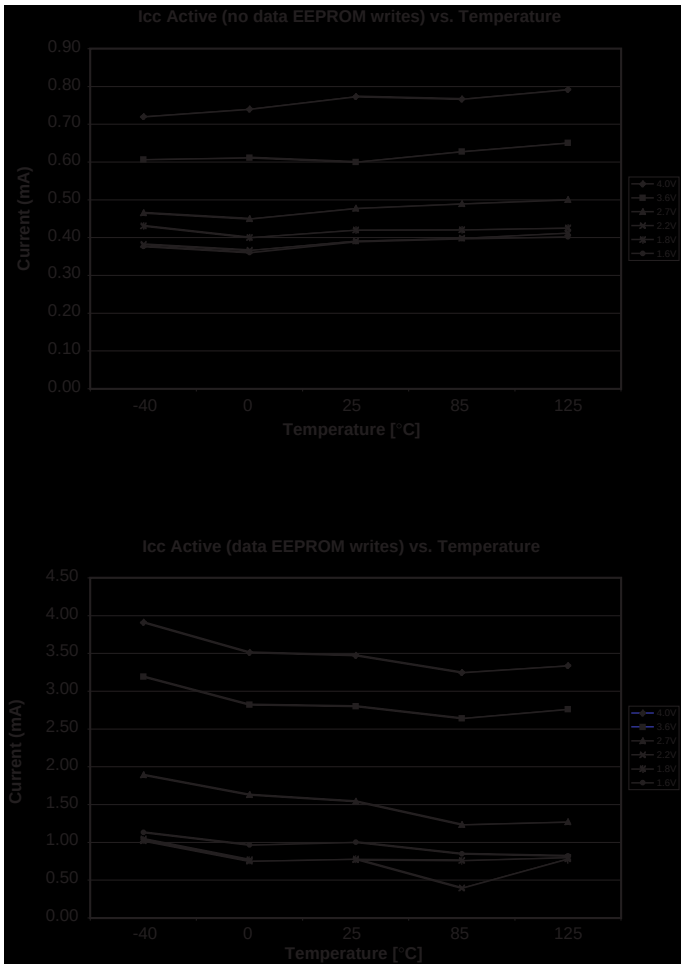


Figure 9. HALT Mode Currents

Figure 10. IDLE Mode Currents

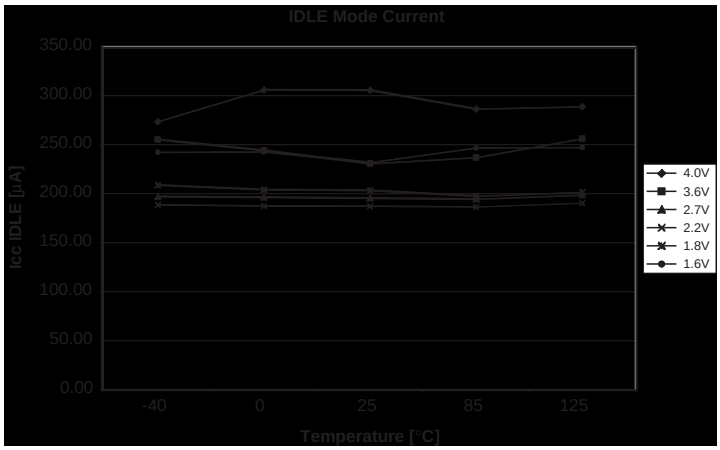


Figure 11. V_{OL}/V_{OH} vs. Current

3.4 Memory Map

All I/O ports, peripheral registers, and core registers (except the accumulator and the program counter) are mapped into the memory space.

Table 10. Memory Mapped Registers

Address	Memory Space	Block	Contents
0x00 - 0x3F	Data	SRAM	Data RAM
0x40 - 0x7F	Data	EEPROM	Data EEPROM
0x80-0x9F	Data	Reserved	
0xA0	Data	HBC	HBCNTRL register
0xA1	Data	HBC	PSCALE register
0xA2	Data	HBC	HPATTERN register
0xA3	Data	HBC	LPATTERN register
0xA4	Data	HBC	BPSEL register
0xA7	Data	Timer1	T1RBLO register
0xA8	Data	Timer1	T1RBHI register
0xA9	Data	HBC	DAT0 register
0xAA	Data	Timer1	T1RALO register
0xAB	Data	Timer1	T1RAHI register
0xAC	Data	Timer1	TMR1LO register
0xAD	Data	Timer1	TMR1HI register
0xAE	Data	Timer1	T1CNTRL register
0xAF	Data	MIW	WKEDG register
0xB0	Data	MIW	WKPND register
0xB1	Data	MIW	WKEN register
0xB2	Data	I/O	PORTGD register
0xB3	Data	I/O	PORTGC register
0xB4	Data	I/O	PORTGP register
0xB5	Data	Timer0	WDSVR register
0xB6	Data	Timer0	T0CNTRL register
0xB7	Data	Clock	HALT mode register
0xB8-0xBA	Data	Reserved	
0xBB	Data	Init. Register	Initialization Register 1
0xBC	Data	Init. Register	Initialization Register 2
0xBD	Data	LBD	LBD register
0xBE	Data	Core	XHI register
0xBF	Data	Core	XLO register
0xC0	Data	Clock	Power Mode Clear (PMC) Register
0xCE	Data	Core	SP register
0xCF	Data	Core	Status register (SR)
0xD0 - 0xFF	Data	Reserved	
0x800 - 0xBF5	Program	EEPROM	Code EEPROM
0xFF6 - 0xFF7	Program	Core	Timer0 Interrupt vector
0xFF8 - 0xFF9	Program	Core	Timer1 Interrupt vector
0xFFA - 0xFFB	Program	Core	MIW Interrupt vector
0xFFC - 0xFFD	Program	Core	Soft Interrupt vector
0xFFE - 0xFFF	Program	Reserved	

Table 11. Timer 1 Control Register (T1CNTRL)

T1CNTRL Register	Bit Name	Function
Bit 7	T1C3	Timer TIMER1 control bit 3 (see Table 12)
Bit 6	T1C2	Timer TIMER1 control bit 2 (see Table 12)
Bit 5	T1C1	Timer TIMER1 control bit 1 (see Table 12)
Bit 4	T1C0	Timer TIMER1 run: 1= Start timer, 0 = Stop timer; or Timer TIMER1 underflow interrrupt pending flag in input capture mode
Bit 3	T1PND	Timer1 interrupt pending flag: 1 = Timer1 interrupt Pending, 0 = Timer1 interrupt not pending
Bit 2	T1EN	Timer1 interrupt enable bit: 1 = Timer1 interrupt enabled, 0 = Timer1 interrupt disabled
Bit 1	M1S1	Capture type: 0 = Pulse capture, 1 = Cycle capture (see Table 12)
Bit 0	T1RBEN	PWM Mode: 0 = Timer1 reload on T1RA, 1 = TIMER1 reload on T1RA and T1RB (always starting with T1RA)

Table 12. Timer 1 Operating Modes

T1 C3	T1 C2	T1 C1	M4 S1	T1 RB	Timer Mode Source	Interrupt	Timer Counts-on
0	0	0	X	X	MODE 2	TIMER1 Underflow	T1 Pos. Edge
0	0	1	X	X	MODE 2	TIMER1 Underflow	T1 Neg. Edge
1	0	1	X	0	MODE 1 T1 Toggle	Autoreload T1RA	Instruction Clock
1	0	0	X	0	MODE 1 No T1 Toggle	Autoreload T1RA	Instruction Clock
1	0	1	X	1	MODE 1 T1 Toggle	Autoreload T1RA/T1RB	Instruction Clock
1	0	0	X	1	MODE 1 No T1 Toggle	Autoreload T1RA/T1RB	Instruction Clock
0	1	0	X	X	MODE 3 Captures: T1 Pos Edge	Pos. T1 Edge	Instruction Clock
0	1	1	X	X	MODE 3 Captures: T1 Neg Edge	Neg. T1 Edge	Instruction Clock
1	1	0	0	X	MODE 4	Pos. to Neg.	Instruction Clock
1	1	0	1	X	MODE 4	Pos. to Pos.	Instruction Clock
1	1	1	0	X	MODE 4	Neg. to Pos.	Instruction Clock
1	1	1	1	X	MODE 4	Neg. to Neg.	Instruction Clock

4.2 Mode 1: Pulse Width Modulation (PWM) Mode

In the PWM mode, the timer counts down at the instruction clock rate. When an underflow occurs, the timer register is reloaded from T1RA/T1RB and the count down proceeds from the loaded value. At every underflow, a pending flag (T1PND) located in the T1CNTRL register is set. Software must then clear the T1PND flag and load the T1RA/T1RB register with an alternate PWM value (if desired.) In addition, the timer can be configured to toggle the T1 output bit upon underflow. Configuring the timer to toggle T1 results in the generation of a signal outputted from port G2 with the width and duty cycle controlled by the values stored in the T1RA/T1RB. A block diagram of the timer's PWM mode of operation is shown in Figure 15.

The PWM timer can be configured to use the T1RA register only for auto-reloading the timer registers or can be configured to use both T1RA and T1RB alternately. If the T1RBEN bit of the T1CNTRL register is 0, the PWM timer will reload using only T1RA ignoring any value store in the T1RB register. However, if the T1RBEN bit is 1 the PWM timer will be reloaded using both the T1RA and T1RB registers. A hardware select logic is implemented to select between T1RA and T1RB alternately, always starting with T1RA, every timer underflows to auto-reload the timer registers. This feature is useful when a signal with variable duty cycle needs to be generated without software intervention.

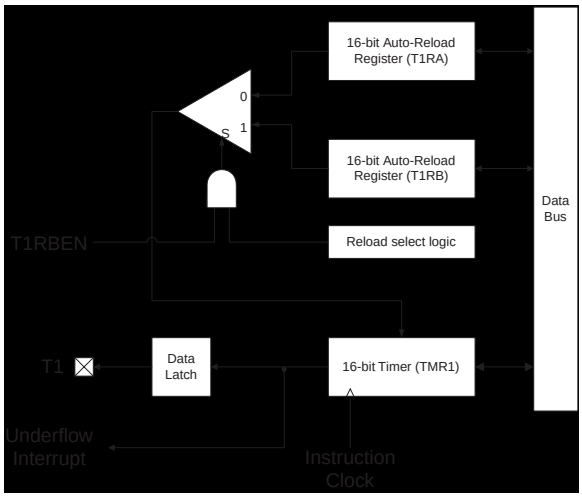
The timer has one interrupt (TMRI1) that is maskable through the T1EN bit of the T1CNTRL register. However, the core is only interrupted if the T1EN bit and the G (Global Interrupt enable) bit of the SR is set. If interrupts are enabled, the timer will generate an interrupt each time T1PND flags is set (whenever the timer underflows provided that the pending flag was cleared.) The interrupt service routine is responsible for proper handling of the T1PND flag and the T1EN bit.

The interrupt will be synchronous with every rising and falling edge of the T1 output signal. Generating interrupts only on rising or falling edges of T1 is achievable through appropriate handling of the T1EN bit or T1PND flag through software.

The following steps show how to properly configure Timer 1 to operate in the PWM mode. For this example, the T1 output signal is toggled with every timer underflow and the “high” and “low” times for the T1 output can be set to different values. The T1 output signal can start out either high or low depending on the configuration of G2; the instructions below are for starting with the T1 output high. Follow the instructions in parentheses to start the T1 output low.

1. Configure T1 as an output by setting bit 2 of PORTGC.
   - SBIT 2, PORTGC ; Configure G2 as an output
2. Initialize T1 to 1 (or 0) by setting (or clearing) bit 2 of PORTGD.
   - SBIT 2, PORTGD ; Set G2 high
3. Load the initial PWM high (low) time into the timer register.
   - LD TMR1LO, #6FH ; High (Low) for 1.391ms (1MHz clock)
   - LD TMR1HI, #05H
4. Load the PWM low (high) time into the T1RA register.
   - LD T1RALO, #2FH ; Low (High) for .303ms (1MHz clock)
   - LD T1RAHI, #01H
5. Write the appropriate control value to the T1CNTRL register to select PWM mode with T1 toggle, to clear the enable bit and pending flag, and to start the timer. (See Table 11 and Table 12.)
   - LD T1CNTRL, #0B0H ; Setting the T1C0 bit starts the timer
6. After every underflow, load T1RA with alternate values. If the user wishes to generate an interrupt on a T1 output transition, reset the pending flags and then enable the interrupt using T1EN. The G bit must also be set. The interrupt service routine must reset the pending flag and perform whatever processing is desired.
   - RBIT T1PND, T1CNTRL ; T1PND equals 3
   - LD T1RALO, #6FH ; High (Low) for 1.391ms (1MHz clock)
   - LD T1RAHI, #05H

Figure 15. Pulse Width Modulation Mode



4.3 Mode 2: External Event Counter Mode

The External Event Counter mode operates similarly to the PWM mode; however, the timer is not clocked by the instruction clock but by transitions of the T1 input signal. The edge is selectable through the T1C1 bit of the T1CNTRL register. A block diagram of the timer’s External Event Counter mode of operation is shown in Figure 16.

The T1 input should be connected to an external device that generates a positive/negative-going pulse for each event. By clocking the timer through T1, the number of positive/negative transitions can be counted therefore allowing software to capture the number of events that occur. The input signal on T1 must have a pulse width equal to or greater than one instruction clock cycle.

The counter can be configured to sense either positive-going or negative-going transitions on the T1 pin. The maximum frequency at which transitions can be sensed is one-half the frequency of the instruction clock.

As with the PWM mode, when the counter underflows the counter is reloaded from the T1RA register and the count down proceeds from the loaded value. At every underflow, a pending flag (T1PND) located in the T1CNTRL register is set. Software must then clear the T1PND flag and can then load the T1RA register with an alternate value.

The counter has one interrupt (TMRI1) that is maskable through the T1EN bit of the T1CNTRL register. However, the core is only interrupted if the T1EN bit and the G (Global Interrupt enable) bit of the SR is set. If interrupts are enabled, the counter will generate an interrupt each time the T1PND flag is set (whenever timer underflows provided that the pending flag was cleared.) The interrupt service routine is responsible for proper handling of the T1PND flag and the T1EN bit.

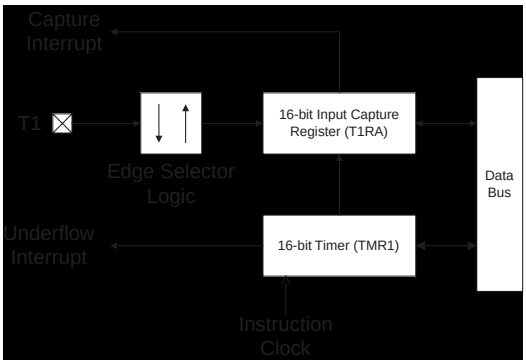
The following steps show how to properly configure Timer 1 to operate in the External Event Counter mode. For this example, the counter is clocked every falling edge of the T1 input signal. Follow the instructions in parentheses to clock the counter every rising edge.

1. Configure T1 as an input by clearing bit 2 of PORTGC.
   - RBIT 2, PORTGC ; Configure G2 as an input
2. Initialize T1 to input with pull-up by setting bit 2 of PORTGD.
   - SBIT 2, PORTGD ; Set G2 high
3. Enable the global interrupt enable bit.
   - SBIT 4, STATUS
4. Load the initial count into the TMR1 and T1RA registers. When the number of external events is detected, the counter will reach zero; however, it will not underflow until the next event is detected. To count N pulses, load the value N-1 into the registers. If it is only necessary to count the number of occurrences and no action needs to be taken at a particular count, load the value 0xFFFF into the registers.
   - LD TMR1LO, #0FFH
   - LD TMR1HI, #0FFH
   - LD T1RALO, #0FFH
   - LD T1RAHI, #0FFH

(See Table 11 and Table 12)
- LD T1CNTRL, #64H ; T1C1 is the edge select bit

6. As soon as the input capture mode is enabled, the timer starts counting. When the selected edge is sensed on T1, the T1RA register is loaded and a Timer 1 interrupt is triggered.

Figure 17. Input Capture Mode



4.5 Mode 4: Difference Input Capture Mode

The Difference Input Capture mode works similarly to the standard Input Capture mode. However, for the Difference Input Capture the timer automatically captures the elapsed time between the selected edges without the core needing to perform the calculation.

For example, the standard Input Capture mode requires that the timer be configured to capture a particular edge (rising or falling) at which time the timer's value is copied into the capture register. If the elapsed time is required, software must move the captured data into RAM and reconfigure the Input Capture mode to capture on the next edge (rising or falling). Software must then subtract the difference between the two edges to yield useful information.

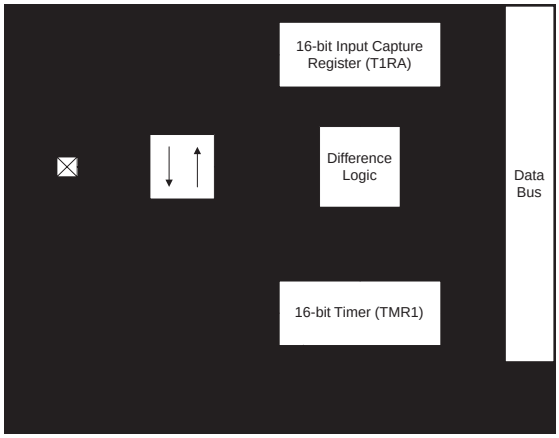
The Difference Capture mode eliminates the need for software intervention and allows for capturing very short pulse or cycle widths. It can be configured to capture the elapsed time between:

1. rising edge to falling edge
2. rising edge to rising edge
3. falling edge to rising edge
4. falling edge to falling edge

Once configured, the Difference Capture timer waits for the first selected edge. When the edge transition has occurred, the 16-bit timer starts counting up based every instruction clock cycle. It will continue to count until the second selected edge transition occurs at which time the timer stops and stores the elapse time into the T1RA register.

Software can now read the difference between transitions directly without using any processor resources. However, like the standard Input Capture mode both the capture (T1PND) and the underflow (T1C0) flags must be monitored and handled appropriately. This feature allows the ACEx microcontroller to capture very small pulses where standard microcontrollers might have missed cycles due to the limited bandwidth.

Figure 18. Difference Capture Mode



5. Timer 0

Timer 0 is a 12-bit free running idle timer. Upon power-up or any reset, the timer is reset to 0x000 and then counts up continuously based on the instruction clock of 1MHz (1 µs). Software cannot read from or write to this timer. However, software can monitor the timer's pending (T0PND) bit that is set every 8192 cycles (initially 4096 cycles after a reset). The T0PND flag is set every other time the timer overflows (transitions from 0xFFF to 0x000) through a divide-by-2 circuit. After an overflow, the timer will reset and restart its counting sequence.

Software can either poll the T0PND bit or vector to an interrupt subroutine. In order to interrupt on a T0PND, software must be sure to enable the Timer 0 interrupt enable (T0INTEN) bit in the Timer 0 control (T0CNTRL) register and also make sure the G bit is set in SR. Once the timer interrupt is serviced, software should reset the T0PND bit before exiting the routine. Timer 0 supports the following functions:

1. Exiting from IDLE mode (See Section 16 for details.)
2. Start up delay from HALT mode
3. Watchdog pre-scalar (See Section 6 for details.)

The T0INTEN bit is a read/write bit. If set to 0, interrupt requests from the Timer 0 are ignored. If set to 1, interrupt requests are accepted. Upon reset, the T0INTEN bit is reset to 0.

The T0PND bit is a read/write bit. If set to 1, it indicates that a Timer 0 interrupt is pending. This bit is set by a Timer 0 overflow and is reset by software or system reset.

The WKINTEN bit is used in the Multi-input Wakeup/Interrupt block. See Section 8 for details.

Figure 19. Timer 0 Control Register Definition (T0CNTRL)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WKINTEN	x	x	x	x	x	T0PND	T0INTEN

6. Watchdog

The Watchdog timer is used to reset the device and safely recover in the rare event of a processor "runaway condition." The 12-bit Timer 0 is used as a pre-scalar for Watchdog timer. The Watchdog timer must be serviced before every 61,440 cycles but no sooner than 4096 cycles since the last Watchdog reset. The Watchdog is serviced through software by writing the value 0x1B to the Watchdog Service (WDSVR) register (see Figure 20). The part resets automatically if the Watchdog is serviced too frequent, or not frequent enough.

The Watchdog timer must be enabled through the Watchdog enable bit (WDEN) in the initialization register. The WDEN bit can only be set while the device is in programming mode. Once set, the Watchdog will always be powered-up enabled. Software cannot disable the Watchdog. The Watchdog timer can only be disabled in programming mode by resetting the WDEN bit as long as the memory write protect (WDIS) feature is not enabled.

WARNING

Ensure that the Watchdog timer has been serviced before entering IDLE mode because it remains operational during this time.

Figure 20. Watchdog Service Register (WDSVR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	1	1	0	1	1

7. Hardware Bit-Coder (Not Available on ACE1501)

The Hardware Bit-Coder is a dedicated hardware bit-encoding peripheral block, Hardware Bit-Coder (HBC), for IR/RF data transmission (see Figure 21.) The HBC is completely software programmable and can be configured to emulate various bit-encoding formats. The software developer has the freedom to encode each bit of data into a desired pattern and output the encoded data at the desired frequency through either the G2 or G5 output (TX) ports.

The HBC contains six 8-bit memory-mapped configuration registers PSCALE, HPATTERN, LPATTERN, BPSEL, HBCNTRL, and DAT0. The registers are used to select the transmission frequency, store the data bit-encoding patterns, configure the data bit-pattern/frame lengths, and control the data transmission flow.

To select the IR/RF transmission frequency, an 8-bit divide constant must be written into the IR/RF Pre-scalar (PSCALE) register. The IR/RF transmission frequency generator divides the 1MHz instruction clock down by 4 and the PSCALE register is used to select the desired IR/RF frequency shift. Together, the transmission frequency range can be configured between 976Hz (PSCALE = 0xFF) and 125kHz (PSCALE = 0x01). Upon a reset, the PSCALE register is initialized to zero disabling the IR/RF transmission frequency generator. However, once the PSCALE register is programmed, the desired IR/RF frequency is maintained as long as the device is powered.

Once the transmission frequency is selected, the data bit-encoding patterns must be stored in the appropriate registers. The HBC contains two 8-bit bit-encoding pattern registers, High-pattern (HPATTERN) and Low-pattern (LPATTERN). The encoding pattern stored in the HPATTERN register is transmitted when the data bit value to be encoded is a 1. Similarly, the pattern stored in the LPATTERN register is transmitted when the data bit value to be encoded is a 0. The HBC transmits each encoded pattern MSB first.

The number of bits transmitted from the HPATTERN and LPATTERN registers is software programmable through the Bit Period Configuration (BPSEL) register (see Figure 22). During the transmission of HPATTERN, the number of bits transmitted is configured by BPH[2:0] (BPSEL[2:0]) while BPL[2:0] (BPSEL[5:3]) configures the number of transmitted bits for the LPATTERN. The HBC allows from 2 (0x1) to 8 (0x7) encoding pattern bits to be transmitted from each register. Upon a reset, BPSEL is initially 0 disabling the HBC from transmitting pattern bits from either register.

The Data (DAT0) register is used to store up to 8 bits of data to be encoded and transmitted by the HBC. This data is shifted, bit by bit, MSB to LSB into a 1-bit decision register. If the active bit shifted into the decision register is 1, the pattern in the HPATTERN register is shifted out of the output port. Similarly, if the active bit is 0 the pattern in the LPATTERN register is shifted out.

The HBC control (HBCNTRL) register is used to configure and control the data transmission. HBCNTRL is divided in 5 different controlling signal FRAME[2:0], IOSEL, TXBUSY, START / STOP, and OCFLAG (see Figure 23.)

FRAME[2:0] selects the number of bits of DAT0 to encode and transmit. The HBC allows from 2 (0x1) to 8 (0x7) DAT0 bits to be encoded and transmitted. Upon a reset, FRAME is initialized to zero disabling the DAT0's decision register transmitting no data.

The IOSEL signal selects the transmission to output (TX) through either port G2 or G5. If IOSEL is 1, G5 is selected as the output port otherwise G2 is selected.

The TXBUSY signal is read only and is used to inform software that a transmission is in progress. TXBUSY goes high when the encoded data begins to shift out of the output port and will remains high during each consecutive DAT0 frame bit transmission (see Figure 25). The HBC will clear the TXBUSY signal when the last DAT0 encoded bit of the frame is transmitted and the STOP signal is 0.

The START / STOP signal controls the encoding and transmission process for each data frame. When software sets the START / STOP bit the DAT0 frame transmission process begins. The START signal will remain high until the beginning of the last encoded DAT0 frame bit transmission. The HBC then clears the START / STOP bit allowing software to elect to either continue with a new DAT0 frame transmission or stop the transmission all together (see Figure 25). If TXBUSY is 0 when the START signal is enabled, a synchronization period occurs before any data is transmitted lasting the amount of time to transmit a 0 encoded bit (see Figure 24).

The OCFLAG signal is read only and goes high when the last encoded bit of the DAT0 frame is transmitting. The OCFLAG signal is used to inform software that the DAT0 frame transmission operation is completing (see Figure 25). If multiple DAT0 frames are to be transmitted consecutively, software should poll the OCFLAG signal for a 1. Once OCFLAG is 1, DAT0 must be reload and the START / STOP bit must be restored to 1 in order to begin the new frame transmission without interruptions (the synchronization period). Since OCFLAG remains high during the entire last encoded DAT0 frame bit transmission, software should wait for the HBC to clear the OCFLAG signal before polling for the new OCFLAG high pulse. If new data is not reloaded into DAT0 and the START signal (STOP is active) is not set before the OCFLAG is 0, the transmission process will end (TXBUSY is cleared) and a new process will begin starting with the synchronization period.

Figure 24 and Figure 25 shows how the HBC performs its data encoding. In the example, two frames are encoded and transmitted consecutively with the following bit encoding format specification:

1. Transmission frequency = 62.5KHz
2. Data to be encoded = 0x52, 0x92 (all 8-bits)
3. Each bit should be encoded as a 3-bit binary value, ‘1’ = 110b and ‘0’ = 100b
4. Transmission output port : G2

To perform the data transmission, software must first initialize the PSCALE, BPSEL, HPATTERN, LPATTERN, and DAT0 registers with the appropriate values.

```
LD    PSCALE, #03H        ; (1MHz ?? 4) ?? 4 = 62.5KHz
LD    BPSEL, #012H        ; BPH = 2, BPL = 2 (3 bits each)
LD    HPATTERN, #0C0H     ; HPATTERN = 0xC0
LD    LPATTERN, #090H     ; LPATTERN = 0x90
LD    DAT0, #052H         ; DAT0 = 0x52
```

Once the basic registers are initialized, the HBC can be started. (At the same time, software must set the number of data bits per data frame and select the desired output port.)

```
LD    HBCNTRL, #27H       ; START / STOP = 1,
                          FRAME = 7, IOSEL = 0
```

After the HBC has started, software must then poll the OCFLAG for a high pulse and restore the DAT0 register and the START signal to continue with the next data transmission.

```
LOOP_HI:
  IFBIT  OCFLAG, HBCNTRL      ; Wait for OCFLAG = 1
  JP     NXT_FRAME
  JP     LOOP_HI

NXT_FRAME:
  LD     DAT0, #092H          ; DAT0 = 0x92
  SBIT   START, HBCNTRL       ; START / STOP = 1
```

If software is to proceed with another data transmission, the OCFLAG must be zero before polling for the next OCFLAG high pulse. However, since the specification in the example requires no other data transmission software can proceed as desired.

```
LOOP_LO:
  IFBIT  OCFLAG, HBCNTRL      ; Wait for OCFLAG = 0
  JP     LOOP_LO
  Etc.                        ; Program proceeds
                              as desired
```

Figure 21. Hardware Bit-coder (HBC) Block Diagram

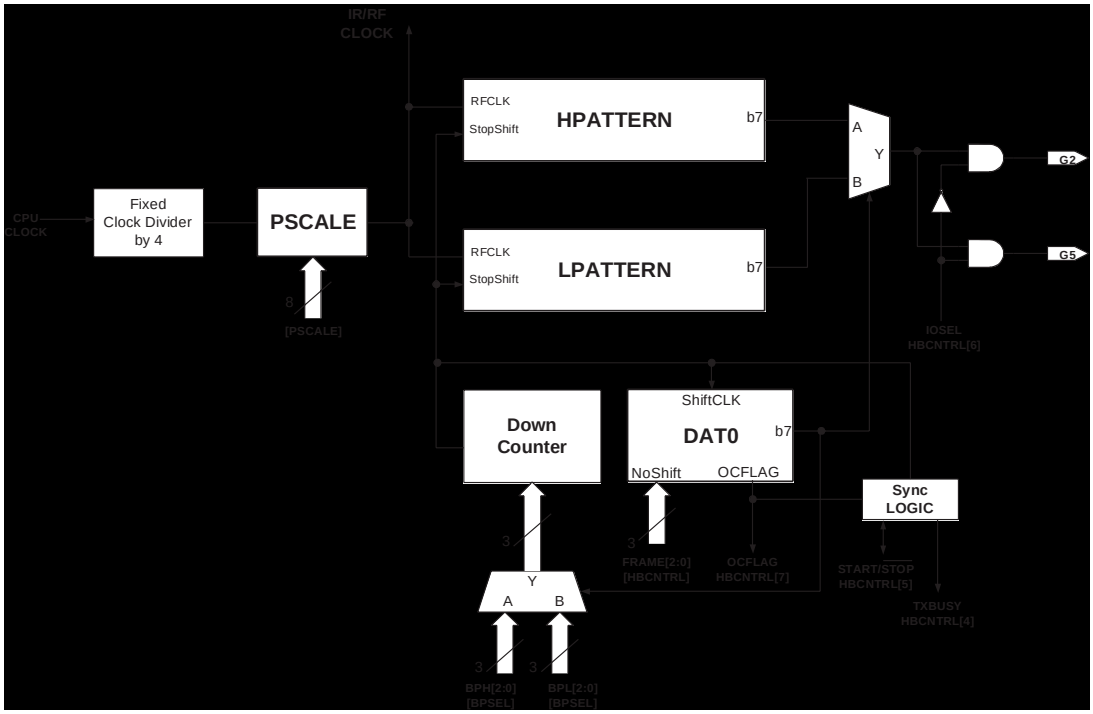
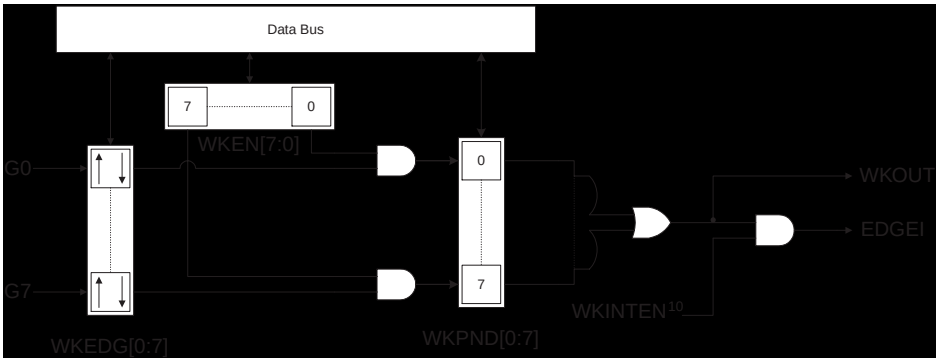


Figure 27. Multi-input Wakeup (MIW) Block Diagram



10. WKINTEN: Bit 7 of T0CNTRL

9. I/O Port

The eight I/O pins (six on 8-pin package option) are bi-directional (see Figure 28). The bi-directional I/O pins can be individually configured by software to operate as high-impedance inputs, as inputs with weak pull-up, or as push-pull outputs. The operating state is determined by the contents of the corresponding bits in the data and configuration registers. Each bi-directional I/O pin can be used for general purpose I/O, or in some cases, for a specific alternate function determined by the on-chip hardware.

Figure 28. PORTGD Logic Diagram

9.1 I/O registers

The I/O pins (G0-G7) have three memory-mapped port registers associated with the I/O circuitry: a port configuration register (PORTGC), a port data register (PORTGD), and a port input register (PORTGP). PORTGC is used to configure the pins as inputs or outputs. A pin may be configured as an input by writing a 0 or as an output by writing a 1 to its corresponding PORTGC bit. If a pin is configured as an output, its PORTGD bit represents the state of the pin (1 = logic high, 0 = logic low). If the pin is configured as an input, its PORTGD bit selects whether the pin is a weak pull-up or a high-impedance input. Table 13 provides details of the port configuration options. The port configuration and data registers can both be read from or written to. Reading PORTGP returns the value of the port pins regardless of how the pins are configured. Since this device supports MIW, PORTG inputs have Schmitt triggers.

Figure 29. I/O Register bit assignments

PORTGC, PORTGD, PORTGD							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
[11]G7	[11]G6	G5	G4	[12]G3	G2	G1	G0

11. Available only on the 14-pin package option

12. G3 after reset is an input with weak pull-up

Table 13. I/O configuration options

Configuration Bit	Data Bit	Port Pin Configuration
0	0	High-impedence input (TRI-STATE input)
0	1	Input with pull-up (weak one input)
1	0	Push-pull zero output
1	1	Push-pull one output

10. In-circuit Programming Specification

The ACEx microcontroller supports in-circuit programming of the internal data EEPROM, code EEPROM, and the initialization registers.

In order to enter into program mode a 10-bit opcode (0x34B) must be shifted into the ACE1501 while the device is executing the internal power on reset (T_{RESET}). The shifting protocol follows the same timing rules as the programming protocol defined in Figure 30.

The opcode is shifted into the ACE1501 serially, MSB first, with the data being valid by the rising edge of the clock. Once the pattern is shifted into the device, the current 10-bit pattern is matched to protocol entrance opcode of 0x34B. If the 10-bit pattern is a match, the device will enable the internal program mode flag so that the device will enter into program mode once reset has completed (see Figure 30.)

The opcode must be shifted in after Vcc settles to the nominal level and should end before the power on reset sequence (T_{reset}) completes; otherwise, the device will start normal execution of the program code. If the external reset is applied by bringing the reset pin low, once the reset pin is release the opcode may now be shifted in and again should end before the reset sequence completes.

10.3 Programming Protocol

After placing the device in program, the programming protocol and commands may be issued.

An externally controlled four-wire interface consisting of a LOAD control pin (G3), a serial data SHIFT-IN input pin (G4), a serial data SHIFT-OUT output pin (G2), and a CLOCK pin (G1) is used to access the on-chip memory locations. Communication between the ACEx microcontroller and the external programmer is made through a 32-bit command and response word described in Table 14. Be sure to either float or tie G5 to Vcc for proper programming functionality.

The serial data timing for the four-wire interface is shown in Figure 31 and the programming protocol is shown in Figure 30.

10.3.1 Write Sequence

The external programmer brings the ACEx microcontroller into programming then needs to set the LOAD pin to Vcc before shifting in the 32-bit serial command word using the SHIFT_IN and CLOCK signals. By definition, bit 31 of the command word is shifted in first. At the same time, the ACEx microcontroller shifts out the 32-bit serial response to the last command on the SHIFT_OUT pin. It is recommended that the external programmer samples this signal t_{ACCESS} (500 ns) after the rising edge of the CLOCK signal. The serial response word, sent immediately after entering programming mode, contains indeterminate data.

After 32 bits have been shifted into the device, the external programmer must set the LOAD signal to 0V, and then apply two clock pulses as shown in Figure 30 to complete program cycle.

The SHIFT_OUT pin acts as the handshaking signal between the device and programming hardware once the LOAD signal is brought low. The device sets SHIFT_OUT low by the time the programmer has sent the second rising edge during the LOAD = 0V phase (if the timing specifications in Figure 30 are obeyed).

The device will set the R bit of the Status register when the write operation has completed. The external programmer must wait for the SHIFT_OUT pin to go high before bringing the LOAD signal to Vcc to initiate a normal command cycle.

10.3.2 Read Sequence

When reading the device after a write, the external programmer must set the LOAD signal to Vcc before it sends the new command word. Next, the 32-bit serial command word (for during a READ) should be shifted into the device using the SHIFT_IN and the CLOCK signals while the data from the previous command is serially shifted out on the SHIFT_OUT pin. After the Read command has been shifted into the device, the external programmer must, once again, set the LOAD signal to 0V and apply two clock pulses as shown in Figure 30 to complete READ cycle. Data from the selected memory location, will be latched into the lower 8 bits of the command word shortly after the second rising edge of the CLOCK signal.

Writing a series of bytes to the device is achieved by sending a series of Write command words while observing the devices handshaking requirements.

Reading a series of bytes from the device is achieved by sending a series of Read command words with the desired addresses in sequence and reading the following response words to verify the correct address and data contents.

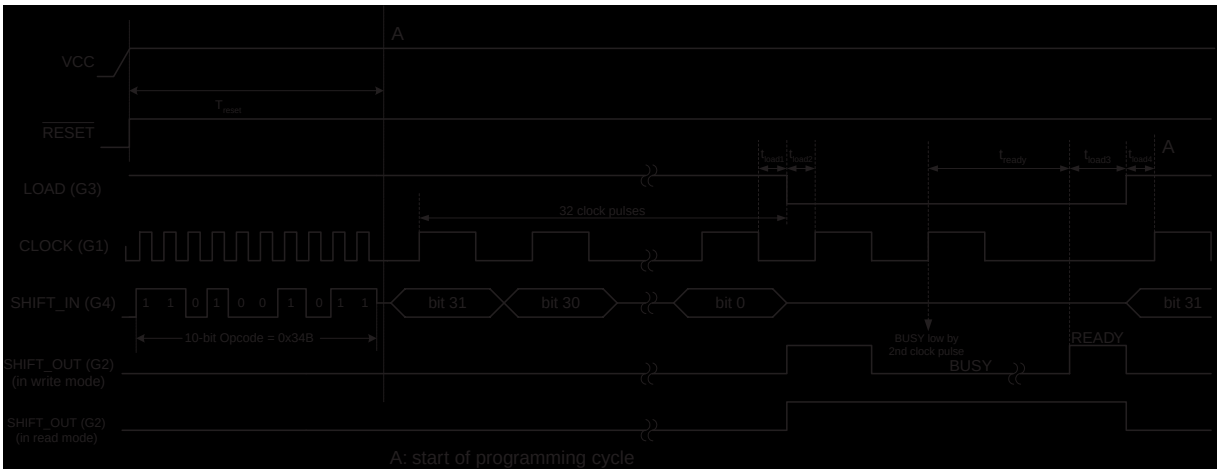
The addresses of the data EEPROM and code EEPROM locations are the same as those used in normal operation.

Powering down the device will cause the part to exit programming mode.

Table 14 32-Bit Command and Response Word

Bit Number	Input Command Word	Output Response Word
bits 31-30	Must be set to 0	X
bit 29	Set to 1 to read/write data EEPROM, or the initialization registers, otherwise 0	X
bit 28	Set to 1 to read/write code EEPROM, otherwise 0	X
bits 27-25	Must be set to 0	X
bit 24	Set to 1 to read, 0 to write	X
bits 23-19	Must be set to 0	X
bits 18 -8	Address of the byte to be read or written	Same as Input command word
bits 7-0	Data to be programmed or zero if data is to be read	Programmed data or data read at specified address

Figure 30. Programming Protocol[13]



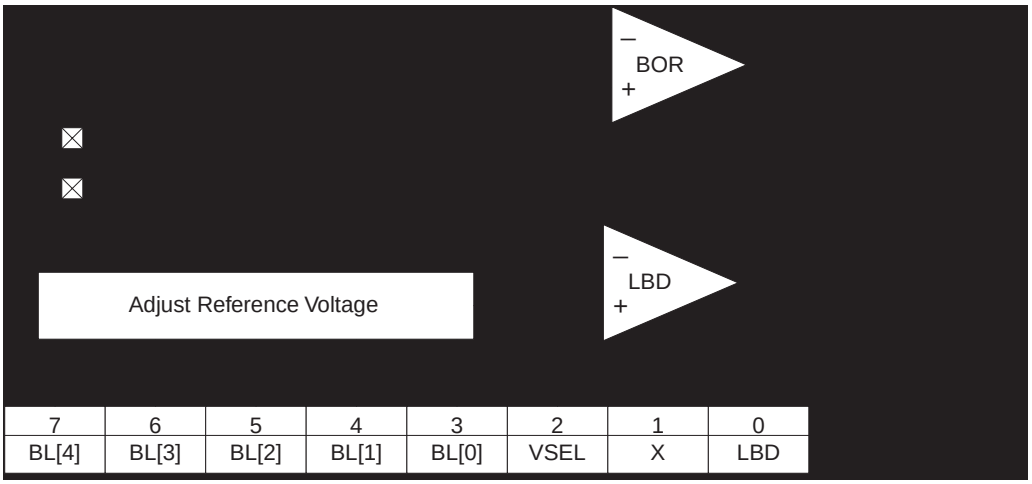
13. During in-circuit programming, G5 must be either not connected or driven high.

Figure 31. Serial Data Timing

11. Brown-out/Low Battery Detect Circuit

The Brown-out Reset (BOR) and Low Battery Detect (LBD) circuits on the ACEx microcontroller have been designed to offer two types of voltage reference comparators. The sections below will describe the functionality of both circuits.

Figure 32. BOR/LBD Block Diagram



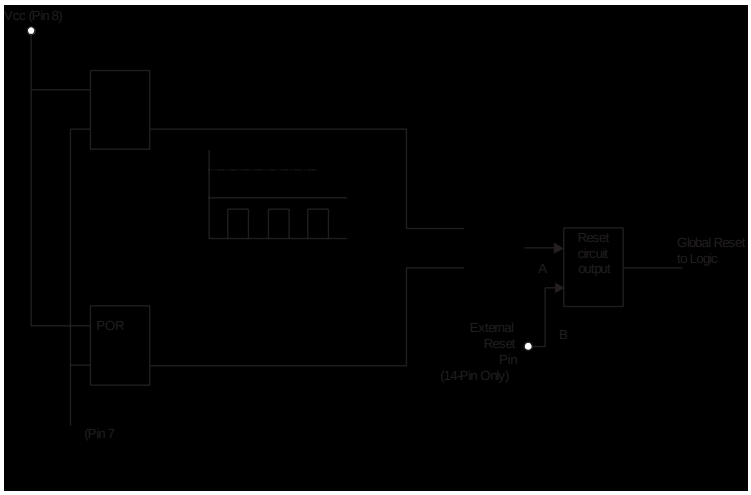
11.1 Brown-out Reset

The Brown-out Reset (BOR) function is used to hold the device in reset when Vcc drops below a fixed threshold (1.83V.) While in reset, the device is held in its initial condition until Vcc rises above the threshold value. Shortly after Vcc rises above the threshold value, an internal reset sequence is started. After the reset sequence, the core fetches the first instruction and starts normal operation.

The BOR should be used in situations when Vcc rises and falls slowly and in situations when Vcc does not fall to zero before rising back to operating range. The Brown-out Reset can be thought of as a supplement function to the Power-on Reset if Vcc does not fall below ~1.5V. The Power-on Reset circuit works best when Vcc starts from zero and rises sharply. In applications where Vcc is not constant, the BOR will give added device stability.

The BOR circuit must be enabled through the BOR enable bit (BOREN) in the initialization register. The BOREN bit can only be set while the device is in programming mode. Once set, the BOR will always be powered-up enabled. Software cannot disable the BOR. The BOR can only be disabled in programming mode by resetting the BOREN bit as long as the global write protect (WDIS) feature is not enabled.

Figure 33. BOR and POR Circuit Relationship Diagram



11.2 Low Battery Detect

The Low Battery Detect (LBD) circuit allows software to monitor the Vcc level at the lower voltage ranges. LBD has a 32-level software programmable voltage reference threshold that can be changed on the fly. Once Vcc falls below the selected threshold, the LBD flag in the LBD control register is set. The LBD flag will hold its value until Vcc rises above the threshold. (See Table 15)

The LBD bit is read only. If LBD is 0, it indicates that the Vcc level is higher than the selected threshold. If LBD is 1, it indicates that the Vcc level is below the selected threshold. The threshold level can be adjusted up to eight levels using the three trim bits (BL[4:0]) of the LBD control register. The LBD flag does not cause any hardware actions or an interruption of the processor. It is for software monitoring only.

The VSEL bit of the LBD control register can be used to select an external voltage source rather than Vcc. If VSEL is 1, the voltage source for the LBD comparator will be an input voltage provided through G4. If VSEL is 0, the voltage source will be Vcc.

The LBD circuit must be enabled through the LBD enable bit (LBDEN) in the initialization register. The LBDEN bit can only be set while the device is in programming mode. Once set, the LBD will always be powered-up enabled. Software cannot disable the LBD. The LBD can only be disabled in programming mode by resetting the LBDEN bit as long as the global write protect (WDIS) feature is not enabled.

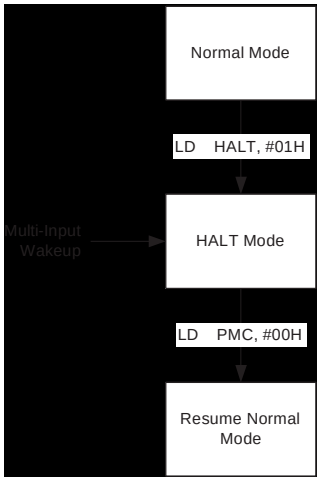
The LBD circuit is disabled during HALT/IDLE mode. After exiting HALT/IDLE, software must wait at lease 10 µs before reading the LBD bit to ensure that the internal circuit has stabilized.

Table 15. LBD Control Register Definition

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BL[4:0]					VSEL	X	LBD

Level	BL[4]	BL[3]	BL[2]	BL[1]	BL[0]	Voltage Reference Range (Typical)
1	0	0	0	0	0	1.81V
2	0	0	0	0	1	1.87V
3	0	0	0	1	0	1.93V
4	0	0	0	1	1	1.99V
5	0	0	1	0	0	2.05V
6	0	0	1	0	1	2.11V
7	0	0	1	1	0	2.17V
8	0	0	1	1	1	2.23V
9	0	1	0	0	0	2.29V
10	0	1	0	0	1	2.36V
11	0	1	0	1	0	2.42V
12	0	1	0	1	1	2.48V
13	0	1	1	0	0	2.54V
14	0	1	1	0	1	2.60V
15	0	1	1	1	0	2.66V
16	0	1	1	1	1	2.72V
17	1	0	0	0	0	2.77V
18	1	0	0	0	1	2.84V
19	1	0	0	1	0	2.91V
20	1	0	0	1	1	2.97V
21	1	0	1	0	0	3.03V
22	1	0	1	0	1	3.09V
23	1	0	1	1	0	3.16V
24	1	0	1	1	1	3.22V
25	1	1	0	0	0	3.28V
26	1	1	0	0	1	3.34V
27	1	1	0	1	0	3.41V
28	1	1	0	1	1	3.47V
29	1	1	1	0	0	3.54V
30	1	1	1	0	1	3.60V
31	1	1	1	1	0	3.67V
32	1	1	1	1	1	3.73V

Figure 36. Recommended HALT Flow

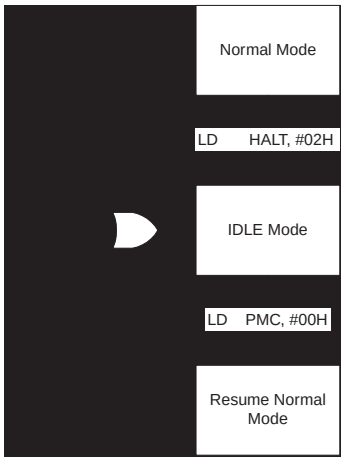


16. IDLE Mode

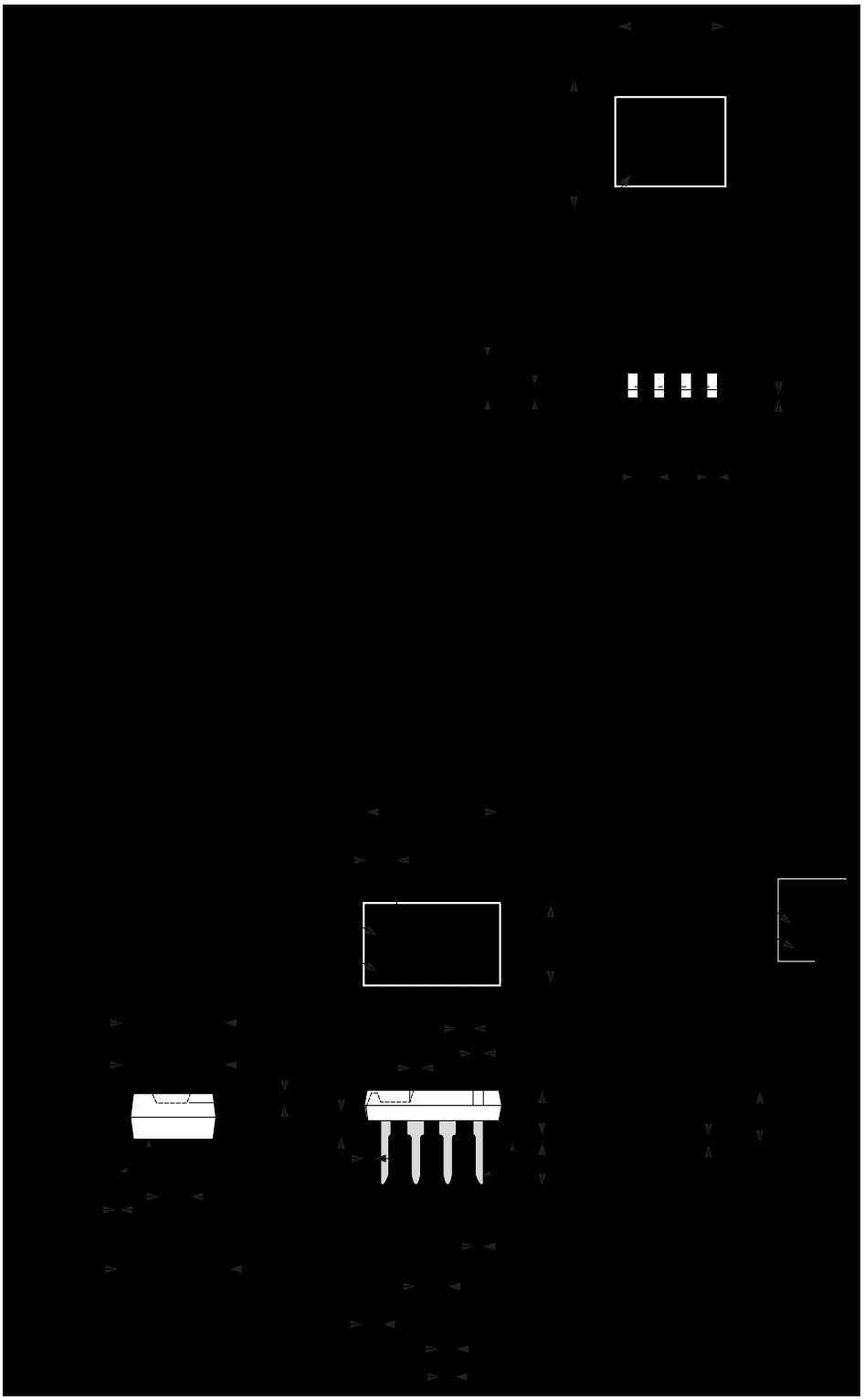
In addition to the HALT mode power saving feature, the device also supports an IDLE mode operation. The device is placed into IDLE mode by setting the IDLE enable bit (EIDLE) of the HALT register through software using only the “LD M, #” instruction. EIDLE is a write only bit and is automatically cleared upon exiting IDLE. The IDLE mode operation is similar to HALT except the internal oscillator, the Watchdog, and the Timer 0 remain active while the other on-chip systems including the LBD and the BOR circuits are shut down.

The device automatically wakes from IDLE mode by the Timer 0 overflow every 8192 cycles (see Section 5). Before entering IDLE mode, software must clear the WKEN register to disable the MIW block. Once a wake from IDLE mode is triggered, the core will begin normal operation by the next clock cycle. Immediately after exiting IDLE mode, software must clear the Power Mode Clear (PMC) register by using only the “LD M, #” instruction. (See Figure 37.)

Figure 37. Recommended IDLE Flow



Physical Dimensions inches (millimeters) unless otherwise noted)

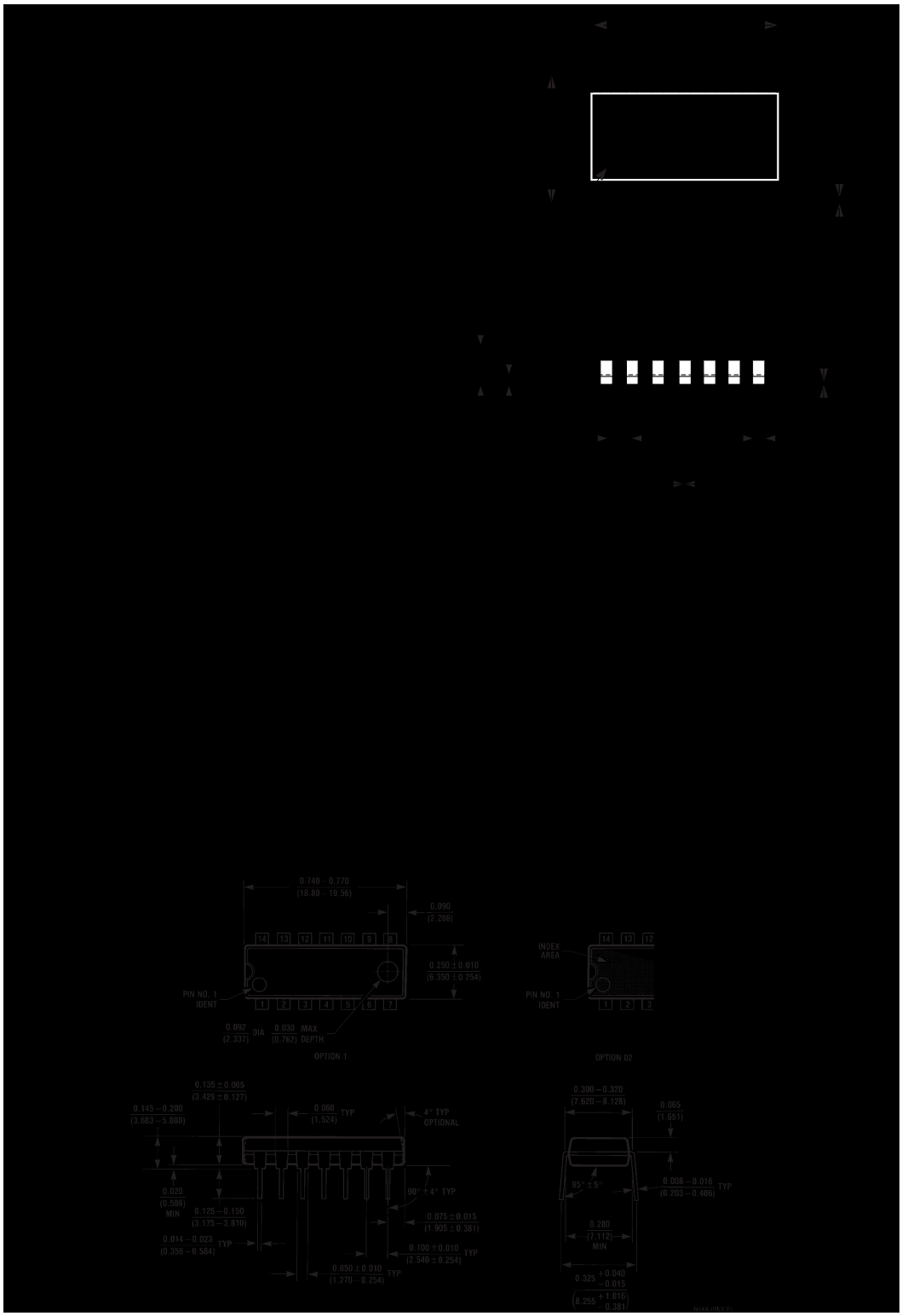


8-Pin DIP (N)
Order Number ACE1501EN/ACE1501VN
Package Number N08A

Physical Dimensions inches (millimeters) unless otherwise noted)

14-Pin TSSOP
Order Number ACE1501EMT/ACE1501VMT
Package Number MT14A

Physical Dimensions inches (millimeters) unless otherwise noted)



14-Pin DIP (N14)
Order Number ACE1501EN14/ACE1501VN14
Package Number N14A