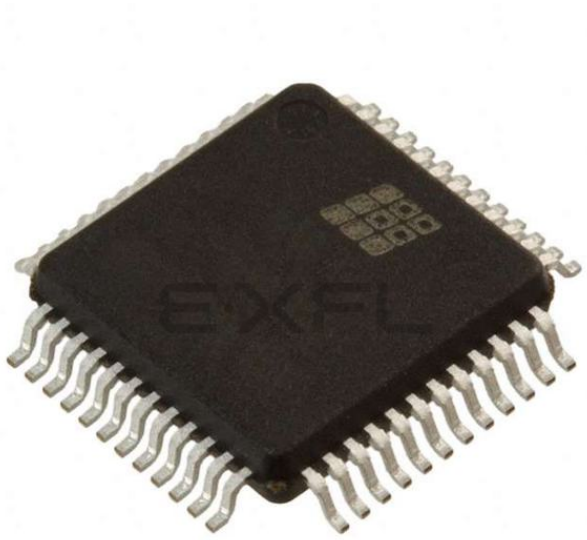
Lattice Semiconductor Corporation - ISPLSI 2032E-180LT48 Datasheet



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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	8
Number of Macrocells	32
Number of Gates	1000
Number of I/O	32
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/isplsi-2032e-180lt48

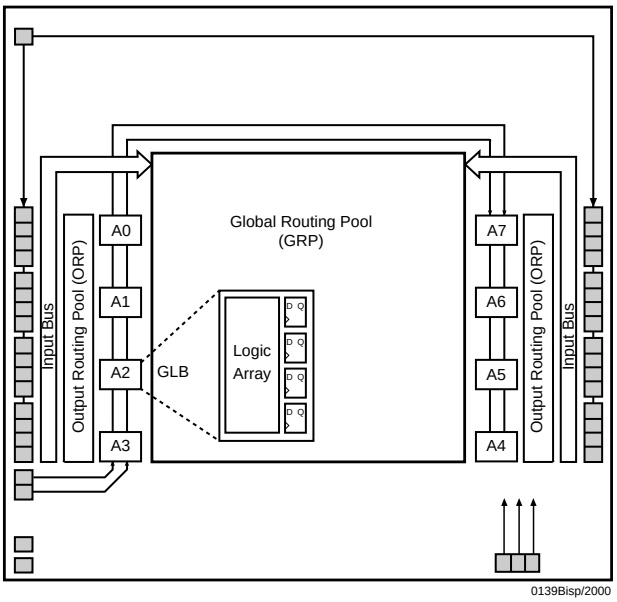
ispLSI® 2032E

In-System Programmable
SuperFAST™ High Density PLD

Features

- **SuperFAST HIGH DENSITY IN-SYSTEM PROGRAMMABLE LOGIC**
  - **— 1000 PLD Gates**
  - **— 32 I/O Pins, Two Dedicated Inputs**
  - **— 32 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
  - **— 100% Functionally and JEDEC Upward Compatible with ispLSI 2032 Devices**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 225 MHz Maximum Operating Frequency**
  - **— t_{pd} = 3.5 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— 5V Programmable Logic Core**
  - **— ispJTAG™ In-System Programmable via IEEE 1149.1 (JTAG) Test Access Port**
  - **— User-Selectable 3.3V or 5V I/O (48-Pin Package Only) Supports Mixed Voltage Systems**
  - **— PCI Compatible Outputs (48-Pin Package Only)**
  - **— Open-Drain Output Option**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— Unused Product Term Shutdown Saves Power**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Prototyping**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Enhanced Pin Locking Capability**
  - **— Three Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**

Functional Block Diagram



Description

The ispLSI 2032E is a High Density Programmable Logic Device. The device contains 32 Registers, 32 Universal I/O pins, two Dedicated Input Pins, three Dedicated Clock Input Pins, one dedicated Global OE input pin and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2032E features 5V in-system programmability and in-system diagnostic capabilities. The ispLSI 2032E offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 2032E device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. A7 (see Figure 1). There are a total of eight GLBs in the ispLSI 2032E device. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

The device also has 32 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually

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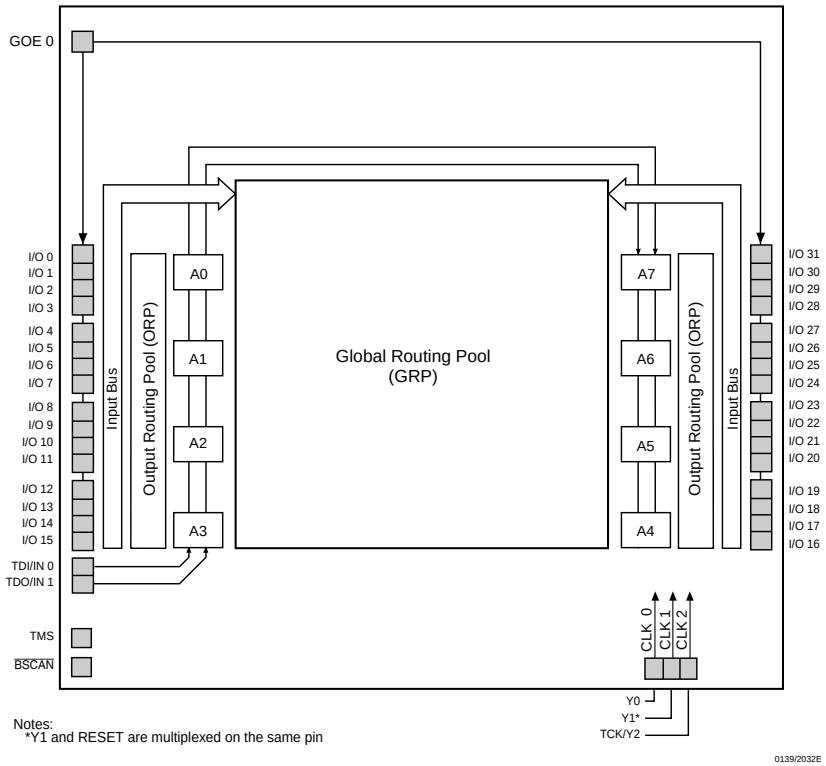
November 2003

Functional Block Diagram

Figure 1. ispLSI 2032E Functional Block Diagram



programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise. By connecting the VCCIO pins to a common 5V or 3.3V power supply, I/O output levels can be matched to 5V or 3.3V compatible voltages. When connected to a 5V supply, the I/O pins provide PCI-compatible output drive (48-pin device only).

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (see Figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by the ORP. Each ispLSI 2032E device contains one Megablock.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 2032E device are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Programmable Open-Drain Outputs

In addition to the standard output configuration, the outputs of the ispLSI 2032E are individually programmable, either as a standard totem-pole output or an open-drain output. The totem-pole output drives the specified Voh and Vol levels, whereas the open-drain output drives only the specified Vol. The Voh level on the open-drain output depends on the external loading and pull-up. This output configuration is controlled by a programmable fuse. The default configuration when the device is in bulk erased state is totem-pole configuration. The open-drain/totem-pole option is selectable through the Lattice software tools.

Absolute Maximum Ratings [1]

Supply Voltage V_{cc} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
V_{CC}	Supply Voltage: Logic Core, Input Buffers T_A = 0°C to +70°C		4.75	5.25	V
V_{CCIO}[1]	Supply Voltage: Output Drivers	5V	4.75	5.25	V
		3.3V	3.0	3.6	V
V_{IL}	Input Low Voltage		0	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+1	V

Table 2-0005/2032E

1. 3.3V I/O operation not available for 44-pin packages.

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYP	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	6	pf	V_{CC} = 5.0V, V_{IN} = 2.0V
C_2	I/O Capacitance	7	pf	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V
C_3	Clock Capacitance	10	pf	V_{CC} = 5.0V, V_Y = 2.0V

Table 2-0006/2032E

Erase/Reprogram Specification

PARAMETER	MINIMUM	MAXIMUM	UNITS
Erase/Reprogram Cycles	10,000	–	Cycles

Table 2-0008/2032E

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time 10% to 90%	1.5 ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

Table 2-0003/2032E

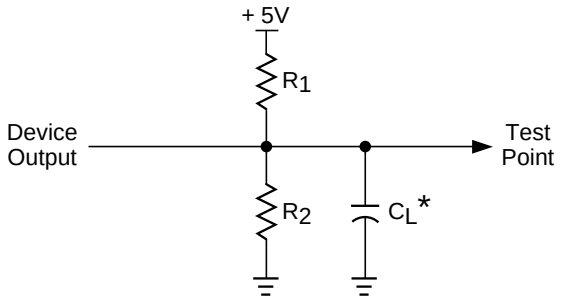
3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see Figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH}-0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL}+0.5V	470Ω	390Ω	5pF

Table 2 - 0004A

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A

DC Electrical Characteristics

Over Recommended Operating Conditions[1]

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	(V_{CCIO} - 0.2)V ≤ V_{IN} ≤ V_{CCIO}		–	–	10	µA
		V_{CCIO} ≤ V_{IN} ≤ 5.25V		–	–	10	µA
I_{IL-PU}	I/O Active Pull-Up Current, non-PCI	0V ≤ V_{IN} ≤ 2.0V		-10	–	-150	µA
	I/O Active Pull-Up Current, PCI[5]	0V ≤ V_{IN} ≤ 2.0V		-10	–	-250	µA
I_{OS}[1]	Output Short Circuit Current, non-PCI	V_{CCIO} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
	Output Short Circuit Current, PCI[5]	V_{CCIO} = 5.0V or 3.3V, V_{OUT} = 0.5V		–	–	-240	mA
I_{CC}[2,4,6]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V, f_{TOGGLE} = 1 MHz	-225/-200	–	85	–	mA
			Others	–	65	–	mA

Table 2-0007/2032E

1. One output at a time for a maximum duration of one second (V_{OUT} = 0.5V). Characterized, but not 100% tested.
2. Meaured using two 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Unused inputs held at 0.0V.
5. Available in 48-pin package only.
6. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-225		-200		-180		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Prop. Delay, 4PT Bypass, ORP Bypass	–	3.5	–	3.5	–	5.0	ns
t_{pd2}	A	2	Data Prop. Delay	–	5.5	–	5.5	–	7.5	ns
f_{max}	A	3	Clk Frequency with Int. Feedback[3]	225	–	200	–	180	–	MHz
f_{max} (Ext.)	–	4	Clk Frequency with Ext. Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	167	–	167	–	125	–	MHz
f_{max} (Tog.)	–	5	Clk Frequency, Max. Toggle	250	–	250	–	200	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clk, 4 PT Bypass	2.5	–	2.5	–	3.0	–	ns
t_{co1}	A	7	GLB Reg. Clk to Output Delay, ORP Bypass	–	2.5	–	2.5	–	4.0	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clk, 4 PT Bypass	0.0	–	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clk	3.5	–	3.5	–	4.0	–	ns
t_{co2}	–	10	GLB Reg. Clk to Output Delay	–	3.5	–	3.5	–	4.5	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clk	0.0	–	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay, ORP Bypass	–	5.0	–	5.0	–	6.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	3.5	–	3.5	–	4.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	7.0	–	7.0	–	10.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	7.0	–	7.0	–	10.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	3.5	–	3.5	–	5.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	3.5	–	3.5	–	5.0	ns
t_{wh}	–	18	Ext. Synch. Clk Pulse Duration, High	2.0	–	2.0	–	2.5	–	ns
t_{wl}	–	19	Ext. Synch. Clk Pulse Duration, Low	2.0	–	2.0	–	2.5	–	ns

Table 2-0030A/2032E

1. Unless noted otherwise, all parameters use a GRP load of four GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-135		-110		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	7.5	–	10.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	10.0	–	13.0	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	137	–	111	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	100	–	77.0	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle	167	–	125	–	MHz
t_{su1}	–	6	GLB Register Setup Time before Clock, 4 PT Bypass	4.0	–	5.5	–	ns
t_{co1}	A	7	GLB Register Clock to Output Delay, ORP Bypass	–	4.5	–	5.5	ns
t_{h1}	–	8	GLB Register Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Register Setup Time before Clock	5.5	–	7.5	–	ns
t_{co2}	–	10	GLB Register Clock to Output Delay	–	5.5	–	6.5	ns
t_{h2}	–	11	GLB Register Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	External Reset Pin to Output Delay, ORP Bypass	–	9.0	–	12.5	ns
t_{rw1}	–	13	External Reset Pulse Duration	5.0	–	6.5	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	12.0	–	14.5	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	12.0	–	14.5	ns
t_{goeen}	B	16	Global OE Output Enable	–	6.0	–	7.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	6.0	–	7.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	3.0	–	4.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	3.0	–	4.0	–	ns

Table 2-0030B/2032E

1. Unless noted otherwise, all parameters use a GRP load of four GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-225		-200		-180		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t_{io}	20	Input Buffer Delay	–	0.6	–	0.4	–	0.6	ns
t_{din}	21	Dedicated Input Delay	–	1.3	–	1.3	–	1.3	ns
GRP									
t_{grp}	22	GRP Delay	–	0.7	–	0.7	–	0.7	ns
GLB									
t_{4ptbpc}	23	4 Product Term Bypass Path Delay (Combinatorial)	–	1.2	–	1.8	–	1.8	ns
t_{4ptbpr}	24	4 Product Term Bypass Path Delay (Registered)	–	1.2	–	1.8	–	2.8	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	–	2.2	–	2.8	–	3.8	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	–	2.2	–	2.8	–	3.8	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	–	2.2	–	2.8	–	3.8	ns
t_{gbp}	28	GLB Register Bypass Delay	–	0.0	–	0.0	–	0.0	ns
t_{gsu}	29	GLB Register Setup Time before Clock	0.8	–	0.8	–	0.3	–	ns
t_{gh}	30	GLB Register Hold Time after Clock	1.7	–	1.7	–	2.7	–	ns
t_{gco}	31	GLB Register Clock to Output Delay	–	0.7	–	0.7	–	0.7	ns
t_{gro}	32	GLB Register Reset to Output Delay	–	1.3	–	2.9	–	1.1	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	–	2.5	–	2.5	–	2.9	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	–	4.2	–	4.4	–	5.9	ns
t_{ptck}	35	GLB Product Term Clock Delay	0.3	2.8	0.7	3.2	1.5	3.7	ns
ORP									
t_{orp}	36	ORP Delay	–	1.0	–	1.0	–	1.1	ns
t_{orpbp}	37	ORP Bypass Delay	–	0.0	–	0.0	–	0.6	ns
Outputs									
t_{ob}	38	Output Buffer Delay	–	1.0	–	0.6	–	1.3	ns
t_{sl}	39	Output Slew Limited Delay Adder	–	1.5	–	1.5	–	1.5	ns
t_{oen}	40	I/O Cell OE to Output Enabled	–	1.5	–	1.5	–	2.8	ns
t_{odis}	41	I/O Cell OE to Output Disabled	–	1.5	–	1.5	–	2.8	ns
t_{goe}	42	Global Output Enable	–	2.0	–	2.0	–	2.2	ns
Clocks									
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	0.8	0.8	1.2	1.2	1.4	1.4	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	1.0	1.0	1.4	1.4	1.6	1.6	ns
Global Reset									
t_{gr}	45	Global Reset to GLB	–	2.7	–	2.7	–	3.5	ns

Table 2-0036A/2032E

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

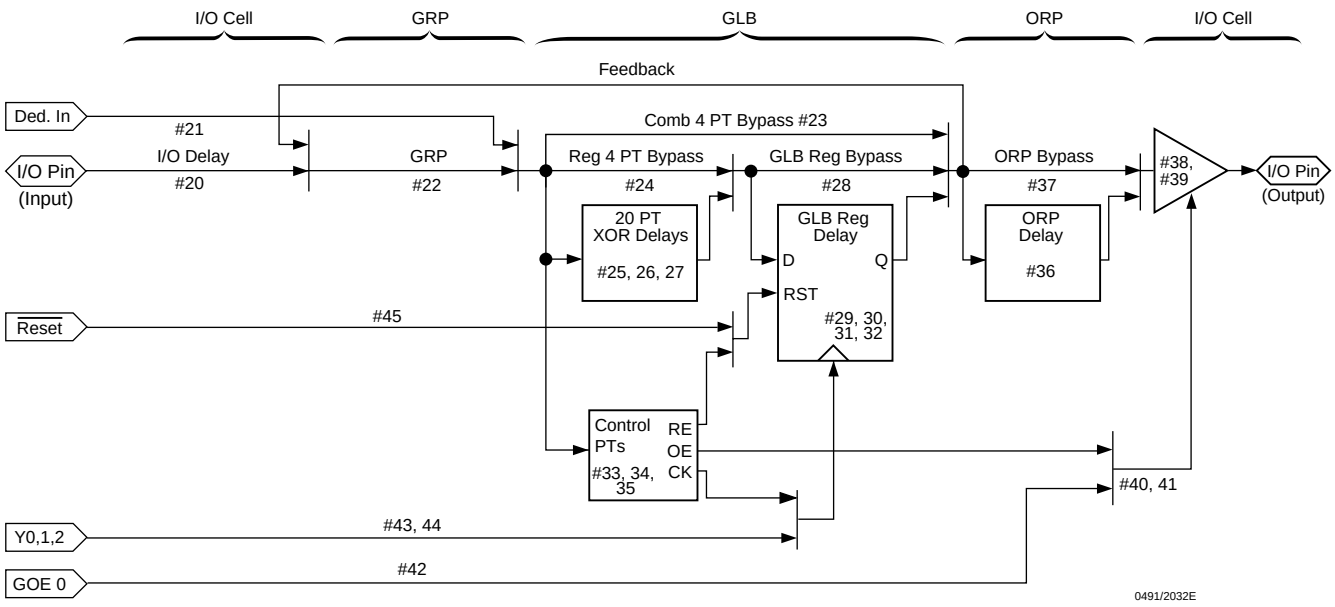
Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-135		-110		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{io}	20	Input Buffer Delay	–	1.1	–	1.7	ns
t_{din}	21	Dedicated Input Delay	–	2.4	–	3.4	ns
GRP							
t_{grp}	22	GRP Delay	–	1.3	–	1.7	ns
GLB							
t_{4ptbpc}	23	4 Product Term Bypass Path Delay (Combinatorial)	–	3.6	–	4.9	ns
t_{4ptbpr}	24	4 Product Term Bypass Path Delay (Registered)	–	3.6	–	4.8	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	–	5.0	–	6.2	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	–	5.1	–	6.8	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	–	5.6	–	7.5	ns
t_{gbp}	28	GLB Register Bypass Delay	–	0.0	–	0.1	ns
t_{gsu}	29	GLB Register Setup Time before Clock	0.3	–	0.5	–	ns
t_{gh}	30	GLB Register Hold Time after Clock	3.0	–	4.0	–	ns
t_{gco}	31	GLB Register Clock to Output Delay	–	0.7	–	0.6	ns
t_{gro}	32	GLB Register Reset to Output Delay	–	1.1	–	1.8	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	–	4.4	–	5.9	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	–	6.4	–	7.1	ns
t_{ptck}	35	GLB Product Term Clock Delay	2.9	5.2	4.0	7.0	ns
ORP							
t_{orp}	36	ORP Delay	–	1.3	–	1.5	ns
t_{orpbp}	37	ORP Bypass Delay	–	0.3	–	0.5	ns
Outputs							
t_{ob}	38	Output Buffer Delay	–	1.2	–	1.2	ns
t_{sl}	39	Output Slew Limited Delay Adder	–	10.0	–	10.0	ns
t_{oen}	40	I/O Cell OE to Output Enabled	–	3.2	–	4.0	ns
t_{odis}	41	I/O Cell OE to Output Disabled	–	3.2	–	4.0	ns
t_{goe}	42	Global Output Enable	–	2.8	–	3.0	ns
Clocks							
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	2.3	2.3	3.2	3.2	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.3	2.3	3.2	3.2	ns
Global Reset							
t_{gr}	45	Global Reset to GLB	–	6.4	–	9.0	ns

Table 2-0036B/2032E

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

ispLSI 2032E Timing Model



Derivations of tsu, th and tco from the Product Term Clock

tsu = Logic + Reg su - Clock (min)
= (**t**io + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**io + **t**grp + **t**ptck(min))
= (#20 + #22 + #26) + (#29) - (#20 + #22 + #35)
2.7 = (0.6 + 0.7 + 2.2) + (0.8) - (0.6 + 0.7 + 0.3)

th = Clock (max) + Reg h - Logic
= (**t**io + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**io + **t**grp + **t**20ptxor)
= (#20 + #22 + #35) + (#30) - (#20 + #22 + #26)
2.3 = (0.6 + 0.7 + 2.8) + (1.7) - (0.6 + 0.7 + 2.2)

tco = Clock (max) + Reg co + Output
= (**t**io + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#20 + #22 + #35) + (#31) + (#36 + #38)
6.8 = (0.6 + 0.7 + 2.8) + (0.7) + (1.0 + 1.0)

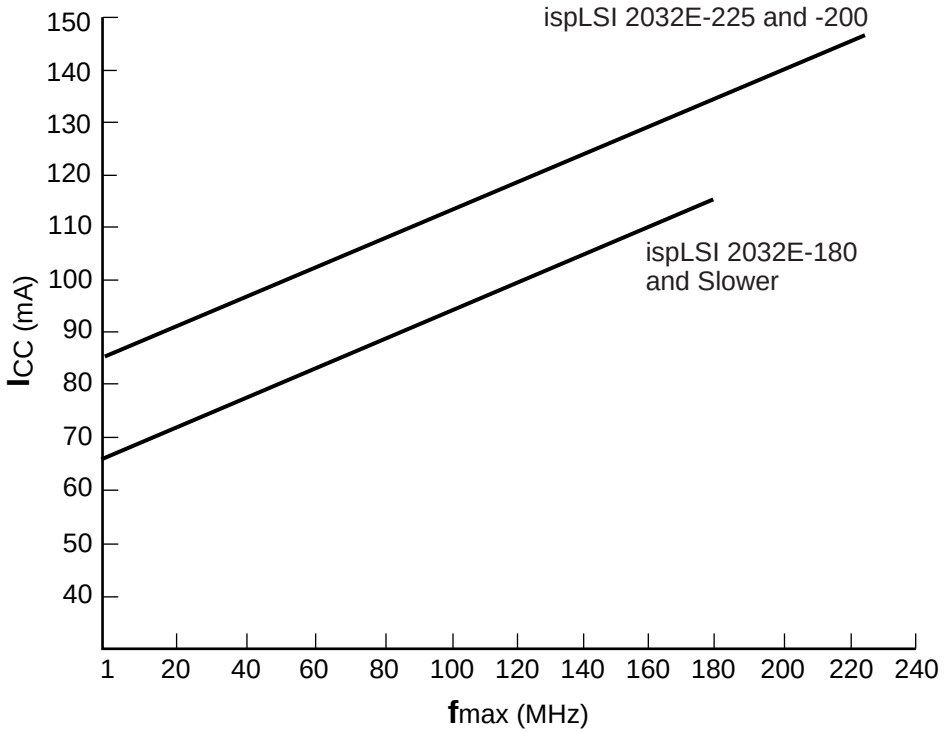
Note: Calculations are based upon timing specifications for the ispLSI 2032E-225L

Table 2-0042/2032E

Power Consumption

Power consumption in the ispLSI 2032E device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of two 16-bit counters
Typical current at 5V, 25°C

I_{CC} can be estimated for the ispLSI 2032E using the following equation:

For 2032E-225 and -200: I_{CC} = 4.5 + (# of PTs * 1.3) + (# of nets * Max freq * 0.0035)
For 2032E-180 and Slower: I_{CC} = 4.5 + (# of PTs * 1.02) + (# of nets * Max freq * 0.0035)

Where:

# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max freq = Highest Clock Frequency to the device (in MHz)

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127A/2032E

Pin Description

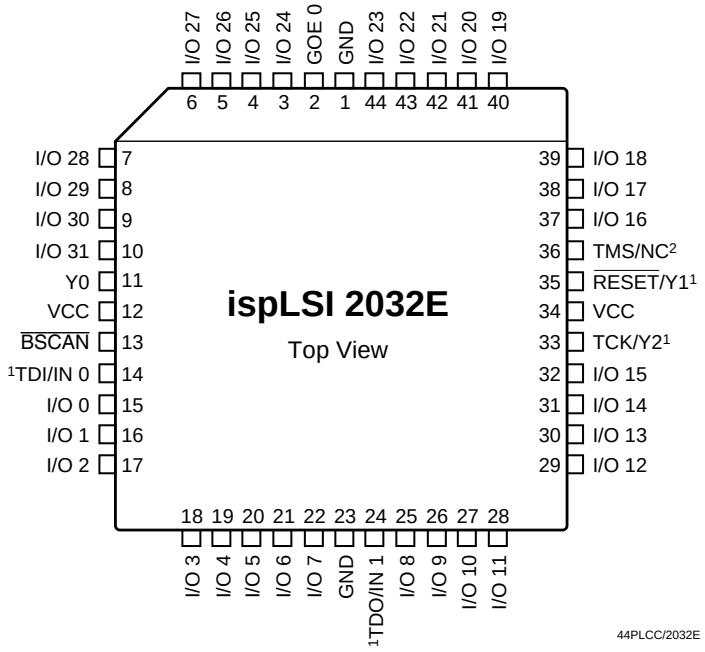
NAME	44-PIN PLCC PIN NUMBERS	44-PIN TQFP PIN NUMBERS	48-PIN TQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10	9, 10, 11, 12, 13, 14, 15, 16, 19, 20, 21, 22, 23, 24, 25, 26, 31 32, 33, 34, 35, 36, 37, 38, 41, 42, 43, 44, 1, 2, 3, 4	9, 10, 11, 13, 14, 15, 16, 17, 20, 21, 22, 23, 25, 26, 27, 28, 33, 34, 35, 37, 38, 39, 40, 41, 44, 45, 46, 47, 1, 2, 3, 4	Input/Output Pins — These are the general purpose I/O pins used by the logic array.
GOE 0	2	40	43	Global Output Enable input pin.
Y0	11	5	5	Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs on the device.
$\overline{\text{RESET}}$/Y1	35	29	31	This pin performs two functions: - Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. - Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
$\overline{\text{BSCAN}}$	13	7	7	Input — Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The TMS, TDI, TDO and TCK controls become active.
TDI/IN 0[1]	14	8	8	Input — This pin performs two functions. When $\overline{\text{BSCAN}}$ is logic low, it functions as an input pin to load programming data into the device. TDI/IN0 also is used as one of the two control pins for the ISP state machine. When $\overline{\text{BSCAN}}$ is high, it functions as a dedicated input pin.
TMS/NC[2]	36	30	32	Input — When in ISP mode, controls operation of ISP state machine.
TDO/IN 1[1]	24	18	19	Output/Input — This pin performs two functions. When $\overline{\text{BSCAN}}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{\text{BSCAN}}$ is high, it functions as a dedicated input pin.
TCK/Y2[1]	33	27	29	Input — This pin performs two functions. When $\overline{\text{BSCAN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. When $\overline{\text{BSCAN}}$ is high, it functions as a dedicated clock input. This clock input is brought into the Clock Distribution Network and can be routed to any GLB and/or I/O cell on the device.
GND	1, 23	17, 39	12, 18, 36, 42	Ground (GND)
VCC	12, 34	6, 28	6, 30	V_{CC}
VCCIO			24, 48	Supply voltage for output drivers, 5V or 3.3V. All VCCIO pins must be connected to the same voltage level.

Table 2-0002/2032E

1. Pins have dual function capability.
2. NC pins are not to be connected to any active signals, V_{CC} or GND.

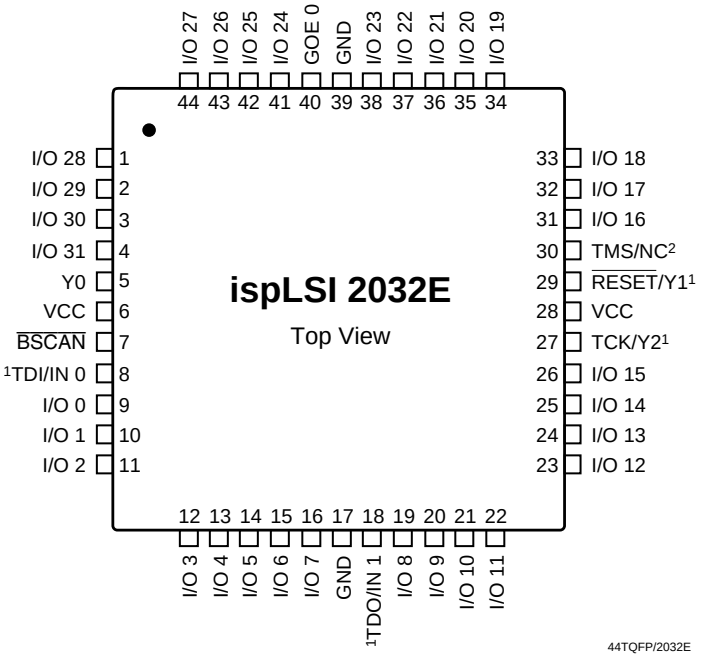
Pin Configuration

ispLSI 2032E 44-Pin PLCC Pinout Diagram



1. Pins have dual function capability.
2. NC pins are not to be connected to any active signals, V_{CC} or GND.

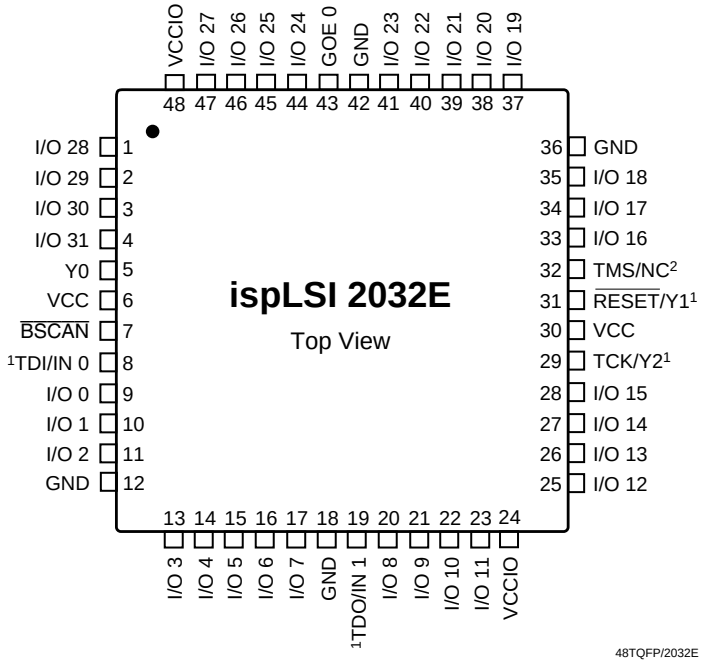
ispLSI 2032E 44-Pin TQFP Pinout Diagram



1. Pins have dual function capability.
2. NC pins are not to be connected to any active signals, V_{CC} or GND.

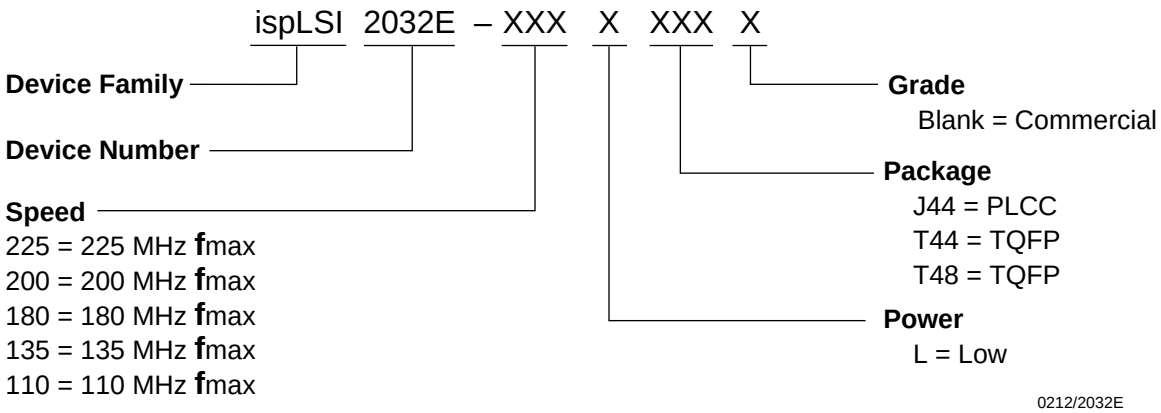
Pin Configuration

ispLSI 2032E 48-Pin TQFP Pinout Diagram



1. Pins have dual function capability.
2. NC pins are not to be connected to any active signals, V_{CC} or GND.

Part Number Description



0212/2032E

ispLSI 2032E Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	225	3.5	ispLSI 2032E-225LJ44	44-Pin PLCC
	225	3.5	ispLSI 2032E-225LT44	44-Pin TQFP
	225	3.5	ispLSI 2032E-225LT48	48-Pin TQFP
	200	3.5	ispLSI 2032E-200LT48*	48-Pin TQFP
	180	5.0	ispLSI 2032E-180LJ44	44-Pin PLCC
	180	5.0	ispLSI 2032E-180LT44	44-Pin TQFP
	180	5.0	ispLSI 2032E-180LT48	48-Pin TQFP
	135	7.5	ispLSI 2032E-135LJ44	44-Pin PLCC
	135	7.5	ispLSI 2032E-135LT44	44-Pin TQFP
	135	7.5	ispLSI 2032E-135LT48	48-Pin TQFP
	110	10.0	ispLSI 2032E-110LJ44	44-Pin PLCC
	110	10.0	ispLSI 2032E-110LT44	44-Pin TQFP
	110	10.0	ispLSI 2032E-110LT48	48-Pin TQFP

*2032E-225 recommended for new designs.

Table 2-0041/2032E