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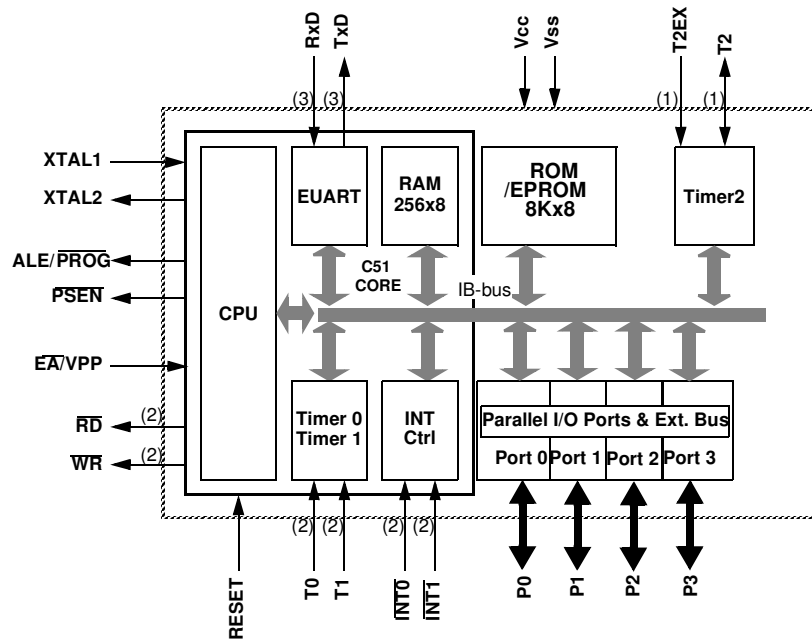
Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/20MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at87c52x2-slsun

Table 1. Memory Size

	ROM (bytes)	EPROM (bytes)	TOTAL RAM (bytes)
TS80C32X2	0	0	256
TS80C52X2	8k	0	256
TS87C52X2	0	8k	256

Block Diagram



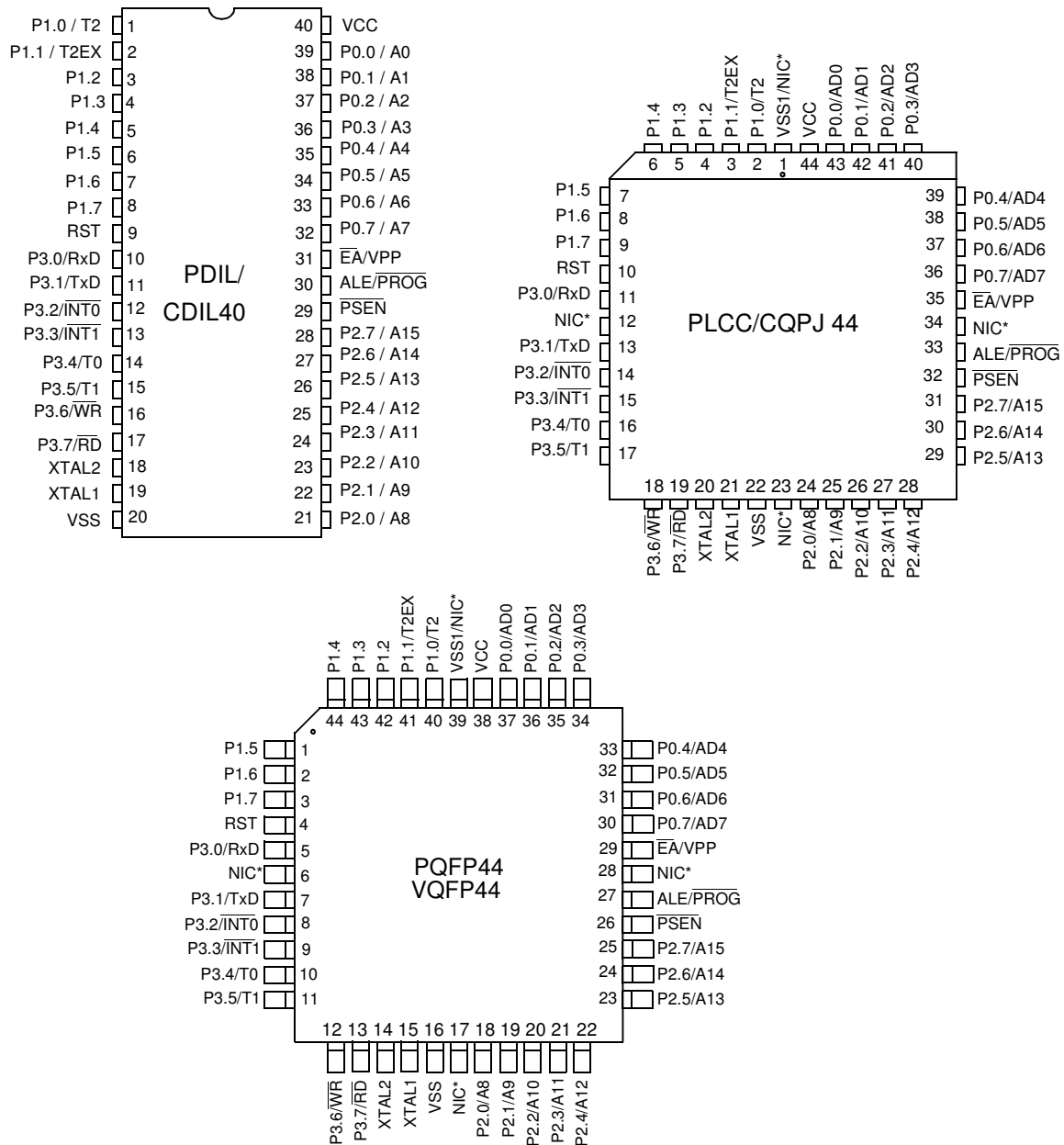
- Notes:
1. Alternate function of Port 1
 2. Alternate function of Port 3

Table 2. All SFRs with their address and their reset value

	Bit Addressable	Non Bit Addressable							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h									FFh
F0h	B 0000 0000								F7h
E8h									EFh
E0h	ACC 0000 0000								E7h
D8 h									DFh
D0 h	PSW 0000 0000								D7h
C8 h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0 h									C7h
B8h	IP XX00 0000	SADEN 0000 0000							BFh
B0h	P3 1111 1111							IPH XX00 0000	B7h
A8h	IE 0X00 0000	SADDR 0000 0000							AFh
A0h	P2 1111 1111		AUXR1 XXXX XXX0						A7h
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXXXXXX0	CKCON XXXX XXX0	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Reserved 

Pin Configuration



*NIC: No Internal Connection

Mnemonic	Pin Number			Type	Name and Function
	DIL	LCC	VQFP 1.4		
	13	15	9	I	INT1 (P3.3): External interrupt 1
	14	16	10	I	T0 (P3.4): Timer 0 external input
	15	17	11	I	T1 (P3.5): Timer 1 external input
	16	18	12	O	WR (P3.6): External data memory write strobe
	17	19	13	O	RD (P3.7): External data memory read strobe
Reset	9	10	4	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC} .
ALE/PROG	30	33	27	O (I)	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
PSEN	29	32	26	O	Program Store ENable: The read strobe to external program memory. When executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.
\overline{EA}/V_{PP}	31	35	29	I	External Access Enable/Programming Supply Voltage: \overline{EA} must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH (RB) or 7FFFH (RC), or FFFFH (RD). If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (RB) or 7FFFH (RC). \overline{EA} must be held low for ROMless devices. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming. If security level 1 is programmed, \overline{EA} will be internally latched on Reset.
XTAL1	19	21	15	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	Crystal 2: Output from the inverting oscillator amplifier

TS80C52X2 Enhanced Features

In comparison to the original 80C52, the TS80C52X2 implements some new features, which are:

- The X2 option
- The Dual Data Pointer
- The 4 level interrupt priority system
- The power-off flag
- The ONCE mode
- The ALE disabling
- Some enhanced features are also located in the UART and the Timer 2

X2 Feature

The TS80C52X2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power
- Save power consumption while keeping same CPU power (oscillator power saving)
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes
- Increase CPU power by 2 while keeping same crystal frequency

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 1. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 2 shows the mode switching waveforms.

Figure 1. Clock Generation Diagram

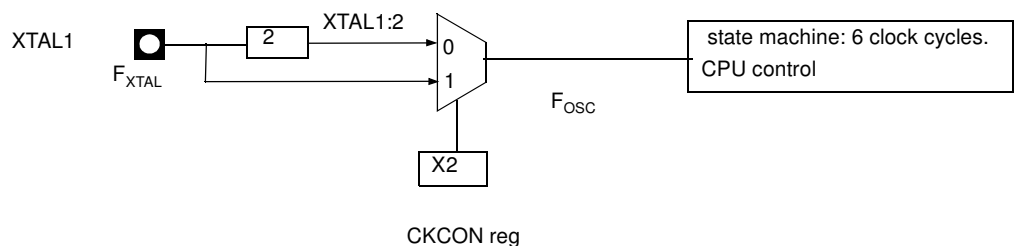
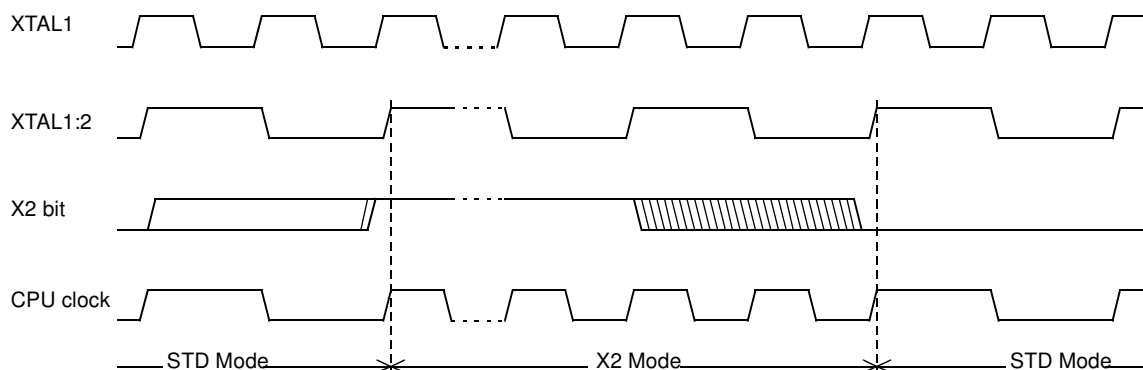


Figure 2. Mode Switching Waveforms



The X2 bit in the CKCON register (See Table 3.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

Note: In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.

Table 3. CKCON Register

CKCON - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	X2

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	X2	CPU and peripheral clock bit Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$).

Reset Value = XXXX XXX0b

Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (<http://www.atmel.com>)

Table 6. T2MOD Register
T2MOD - Timer 2 Mode Control Register (C9h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN
Bit Number	Bit Mnemonic	Description					
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
1	T2OE	Timer 2 Output Enable bit Clear to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.					
0	DCEN	Down Counter Enable bit Clear to disable timer 2 as up/down counter. Set to enable timer 2 as up/down counter.					

Reset Value = XXXX XX00b
Not bit addressable

Table 9. SCON Register
SCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0																									
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI																									
Bit Number	Bit Mnemonic	Description																														
7	FE	Framing Error bit (SMOD0=1) Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit																														
	SM0	Serial port Mode bit 0 Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit																														
6	SM1	Serial port Mode bit 1 <table><tr><th>SM0</th><th>SM1</th><th>Mode</th><th>Description</th><th>Baud Rate</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Shift Register</td><td>$F_{XTAL}/12$ (/6 in X2 mode)</td></tr><tr><td>0</td><td>1</td><td>1</td><td>8-bit UART</td><td>Variable</td></tr><tr><td>1</td><td>0</td><td>2</td><td>9-bit UART</td><td>$F_{XTAL}/64$ or $F_{XTAL}/32$ (/32, /16 in X2 mode)</td></tr><tr><td>1</td><td>1</td><td>3</td><td>9-bit UART</td><td>Variable</td></tr></table>						SM0	SM1	Mode	Description	Baud Rate	0	0	0	Shift Register	$F_{XTAL}/12$ (/6 in X2 mode)	0	1	1	8-bit UART	Variable	1	0	2	9-bit UART	$F_{XTAL}/64$ or $F_{XTAL}/32$ (/32, /16 in X2 mode)	1	1	3	9-bit UART	Variable
SM0	SM1	Mode	Description	Baud Rate																												
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1	1	3	9-bit UART	Variable																												
5	SM2	Serial port Mode 2 bit / Multiprocessor Communication Enable bit Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.																														
4	REN	Reception Enable bit Clear to disable serial reception. Set to enable serial reception.																														
3	TB8	Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3. Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.																														
2	RB8	Receiver Bit 8 / Ninth bit received in modes 2 and 3 Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.																														
1	TI	Transmit Interrupt flag Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.																														
0	RI	Receive Interrupt flag Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 7. and Figure 8. in the other modes.																														

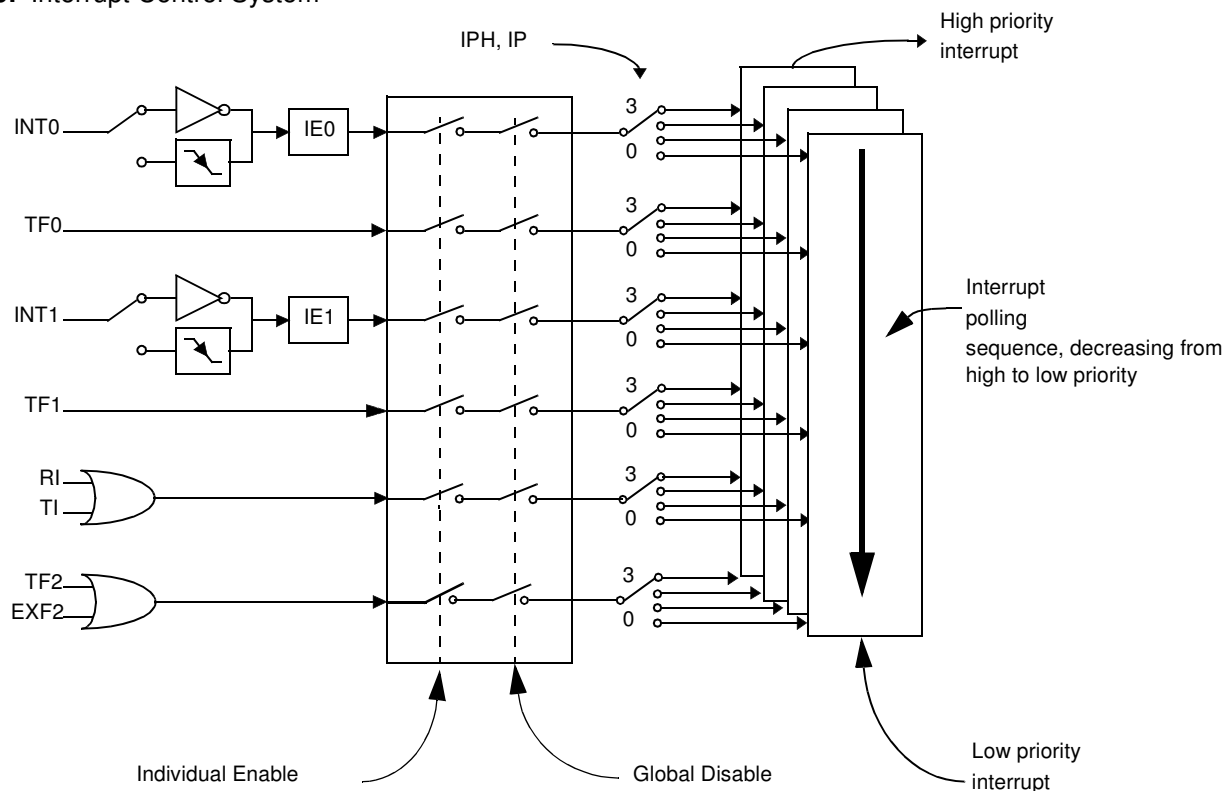
Reset Value = 0000 0000b

Bit addressable

Interrupt System

The TS80C52X2 has a total of 6 interrupt vectors: two external interrupts ($\overline{\text{INT0}}$ and $\overline{\text{INT1}}$), three timer interrupts (timers 0, 1 and 2) and the serial port interrupt. These interrupts are shown in Figure 9.

Figure 9. Interrupt Control System



Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 12.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 13.) and in the Interrupt Priority High register (See Table 14.). shows the bit values and priority levels associated with each combination.

Table 11. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level

Table 14. IPH Register
IPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Description															
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.															
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.															
5	PT2H	Timer 2 overflow interrupt Priority High bit <table> <tr> <th>PT2H</th><th>PT2</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PT2H	PT2	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT2H	PT2	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
4	PSH	Serial port Priority High bit <table> <tr> <th>PSH</th><th>PS</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PSH	PS	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PSH	PS	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
3	PT1H	Timer 1 overflow interrupt Priority High bit <table> <tr> <th>PT1H</th><th>PT1</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PT1H	PT1	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT1H	PT1	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
2	PX1H	External interrupt 1 Priority High bit <table> <tr> <th>PX1H</th><th>PX1</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PX1H	PX1	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PX1H	PX1	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
1	PT0H	Timer 0 overflow interrupt Priority High bit <table> <tr> <th>PT0H</th><th>PT0</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PT0H	PT0	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT0H	PT0	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
0	PX0H	External interrupt 0 Priority High bit <table> <tr> <th>PX0H</th><th>PX0</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PX0H	PX0	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PX0H	PX0	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															

Reset Value = XX00 0000b
Not bit addressable

Power-off Flag

The power-off flag allows the user to distinguish between a “cold start” reset and a “warm start” reset.

A cold start reset is the one induced by V_{CC} switch-on. A warm start reset occurs while V_{CC} is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 17.). POF is set by hardware when V_{CC} rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a V_{CC} range from 4.5V to 5.5V. For lower V_{CC} value, reading POF bit will return indeterminate value.

Table 17. PCON Register
PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
Bit Number	Bit Mnemonic	Description					
7	SMOD1	Serial port Mode bit 1 Set to select double baud rate in mode 1, 2 or 3.					
6	SMOD0	Serial port Mode bit 0 Clear to select SM0 bit in SCON register. Set to select FE bit in SCON register.					
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
4	POF	Power-off Flag Clear to recognize next reset type. Set by hardware when V_{CC} rises from 0 to its nominal voltage. Can also be set by software.					
3	GF1	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.					
2	GF0	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.					
1	PD	Power-down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.					
0	IDL	Idle mode bit Clear by hardware when interrupt or reset occurs. Set to enter idle mode.					

Reset Value = 00X1 0000b

Not bit addressable

Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 18. AUXR Register
AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	AO

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	AO	ALE Output bit Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = XXXX XXX0b

Not bit addressable

EPROM Structure

The TS87C52X2 is divided in two different arrays:

- the code array: 8 Kbytes
- the encryption array: 64 bytes

In addition a third non programmable array is implemented:

- the signature array: 4 bytes

EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

Program Lock Bits

The three lock bits, when programmed according to Table 1., will provide different level of protection for the on-chip code and data.

Program Lock Bits				Protection Description
Security level	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	P	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the EPROM is disabled.
3	U	P	U	Same as 2, also verify is disabled.
4	U	U	P	Same as 3, also external execution is disabled.

U: unprogrammed

P: programmed

WARNING: Security level 2 and 3 should only be programmed after EPROM and Core verification.

Signature Bytes

The TS80/87C52X2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 9.

EPROM Programming

Set-up modes

In order to program and verify the EPROM or to read the signature bytes, the TS87C52X2 is placed in specific set-up modes (See Figure 11.).

Electrical Characteristics

Absolute Maximum Ratings⁽¹⁾

Ambient Temperature Under Bias:

C = commercial.....0°C to 70°C
 I = industrial-40°C to 85°C
 Storage Temperature -65°C to + 150°C
 Voltage on V_{CC} to V_{SS}-0.5V to + 7 V
 Voltage on V_{PP} to V_{SS} -0.5V to + 13 V
 Voltage on Any Pin to V_{SS}-0.5V to $V_{CC} + 0.5V$
 Power Dissipation 1 W⁽²⁾

- Notes: 1. Stresses at or above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

Power Consumption Measurement

Since the introduction of the first C51 devices, every manufacturer made operating I_{CC} measurements under reset, which made sense for the designs where the CPU was running under reset. In Atmel new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That's why, while keeping measurements under Reset, Atmel presents a new way to measure the operating I_{CC} :

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = V_{CC} , RST = V_{SS} , XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating I_{CC} .

DC Parameters for Standard Voltage

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{SS} = 0\text{ V}$; $V_{CC} = 5V \pm 10\%$; $F = 0$ to 40 MHz.

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; $V_{SS} = 0\text{ V}$; $V_{CC} = 5V \pm 10\%$; $F = 0$ to 40 MHz.

Table 22. DC Parameters in Standard Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		$0.2 V_{CC} - 0.1$	V	
V_{IH}	Input High Voltage except XTAL1, RST	$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage, XTAL1, RST	$0.7 V_{CC}$		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage, ports 1, 2, 3 ⁽⁶⁾			0.3	V	$I_{OL} = 100\text{ }\mu\text{A}^{(4)}$
				0.45	V	$I_{OL} = 1.6\text{ mA}^{(4)}$
				1.0	V	$I_{OL} = 3.5\text{ mA}^{(4)}$
V_{OL1}	Output Low Voltage, port 0 ⁽⁶⁾			0.3	V	$I_{OL} = 200\text{ }\mu\text{A}^{(4)}$
				0.45	V	$I_{OL} = 3.2\text{ mA}^{(4)}$
				1.0	V	$I_{OL} = 7.0\text{ mA}^{(4)}$
V_{OL2}	Output Low Voltage, ALE, $\overline{\text{PSEN}}$			0.3	V	$I_{OL} = 100\text{ }\mu\text{A}^{(4)}$
				0.45	V	$I_{OL} = 1.6\text{ mA}^{(4)}$
				1.0	V	$I_{OL} = 3.5\text{ mA}^{(4)}$

Table 27. AC Parameters for Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T	25		33		25		50		33		ns
T _{LHLL}	40		25		42		35		52		ns
T _{AVLL}	10		4		12		5		13		ns
T _{LLAX}	10		4		12		5		13		ns
T _{LLIV}		70		45		78		65		98	ns
T _{LLPL}	15		9		17		10		18		ns
T _{PLPH}	55		35		60		50		75		ns
T _{PLIV}		35		25		50		30		55	ns
T _{PXIX}	0		0		0		0		0		ns
T _{PXIZ}		18		12		20		10		18	ns
T _{AVIV}		85		53		95		80		122	ns
T _{PLAZ}		10		10		10		10		10	ns

Table 28. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T _{LHLL}	Min	2 T - x	T - x	10	8	15	ns
T _{AVLL}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLAX}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLIV}	Max	4 T - x	2 T - x	30	22	35	ns
T _{LLPL}	Min	T - x	0.5 T - x	10	8	15	ns
T _{PLPH}	Min	3 T - x	1.5 T - x	20	15	25	ns
T _{PLIV}	Max	3 T - x	1.5 T - x	40	25	45	ns
T _{PXIX}	Min	x	x	0	0	0	ns
T _{PXIZ}	Max	T - x	0.5 T - x	7	5	15	ns
T _{AVIV}	Max	5 T - x	2.5 T - x	40	30	45	ns
T _{PLAZ}	Max	x	x	10	10	10	ns

EPROM Programming and Verification Characteristics

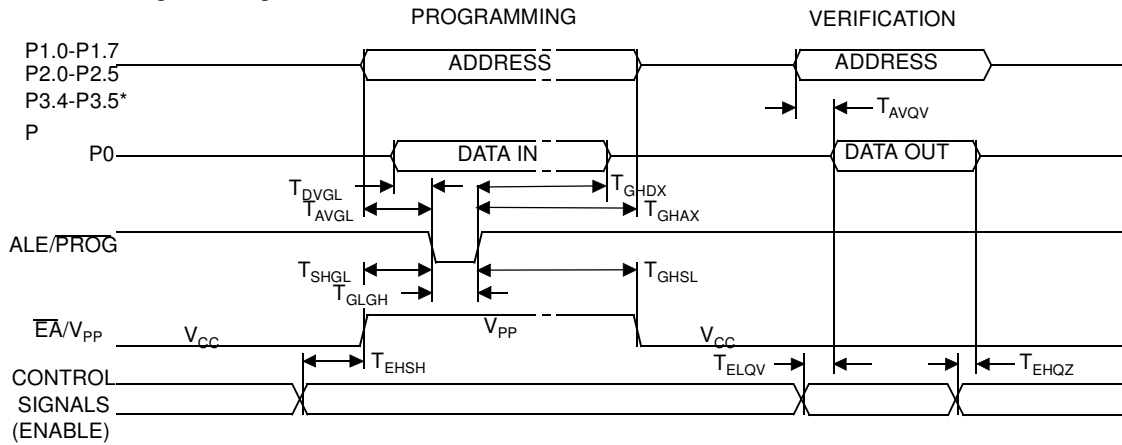
$T_A = 21^\circ\text{C}$ to 27°C ; $V_{SS} = 0\text{V}$; $V_{CC} = 5\text{V} \pm 10\%$ while programming. V_{CC} = operating range while verifying.

Table 35. EPROM Programming Parameters

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13	V
I_{PP}	Programming Supply Current		75	mA
$1/T_{CLCL}$	Oscillator Frequency	4	6	MHz
T_{AVGL}	Address Setup to $\overline{\text{PROG}}$ Low	$48 T_{CLCL}$		
T_{GHAX}	Address Hold after $\overline{\text{PROG}}$	$48 T_{CLCL}$		
T_{DVGL}	Data Setup to $\overline{\text{PROG}}$ Low	$48 T_{CLCL}$		
T_{GHDX}	Data Hold after $\overline{\text{PROG}}$	$48 T_{CLCL}$		
T_{EHS}	(Enable) High to V_{PP}	$48 T_{CLCL}$		
T_{SHGL}	V_{PP} Setup to $\overline{\text{PROG}}$ Low	10		μs
T_{GHSL}	V_{PP} Hold after $\overline{\text{PROG}}$	10		μs
T_{GLGH}	$\overline{\text{PROG}}$ Width	90	110	μs
T_{AVQV}	Address to Valid Data		$48 T_{CLCL}$	
T_{ELQV}	ENABLE Low to Data Valid		$48 T_{CLCL}$	
T_{EHQZ}	Data Float after ENABLE	0	$48 T_{CLCL}$	

EPROM Programming and Verification Waveforms

Figure 22. EPROM Programming and Verification Waveforms



* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

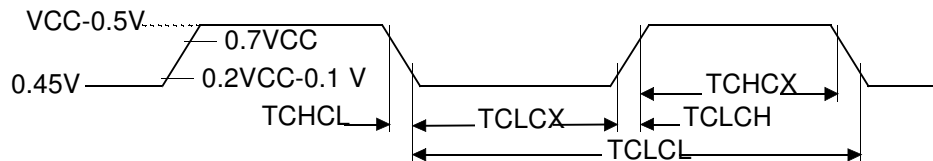
External Clock Drive Characteristics (XTAL1)

Table 36. AC Parameters

Symbol	Parameter	Min	Max	Units
T_{CLCL}	Oscillator Period	25		ns
T_{CHCX}	High Time	5		ns
T_{CLCX}	Low Time	5		ns
T_{CLCH}	Rise Time		5	ns
T_{CHCL}	Fall Time		5	ns
T_{CHCX}/T_{CLCX}	Cyclic ratio in X2 mode	40	60	%

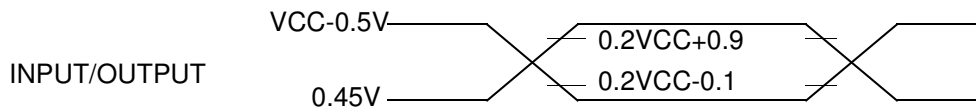
External Clock Drive Waveforms

Figure 23. External Clock Drive Waveforms



AC Testing Input/Output Waveforms

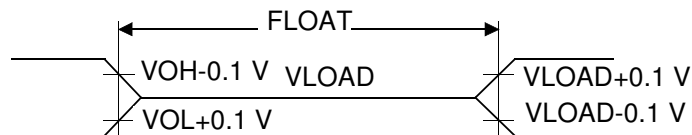
Figure 24. AC Testing Input/Output Waveforms



AC inputs during testing are driven at $V_{CC} - 0.5$ for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at V_{IH} min for a logic “1” and V_{IL} max for a logic “0”.

Float Waveforms

Figure 25. Float Waveforms

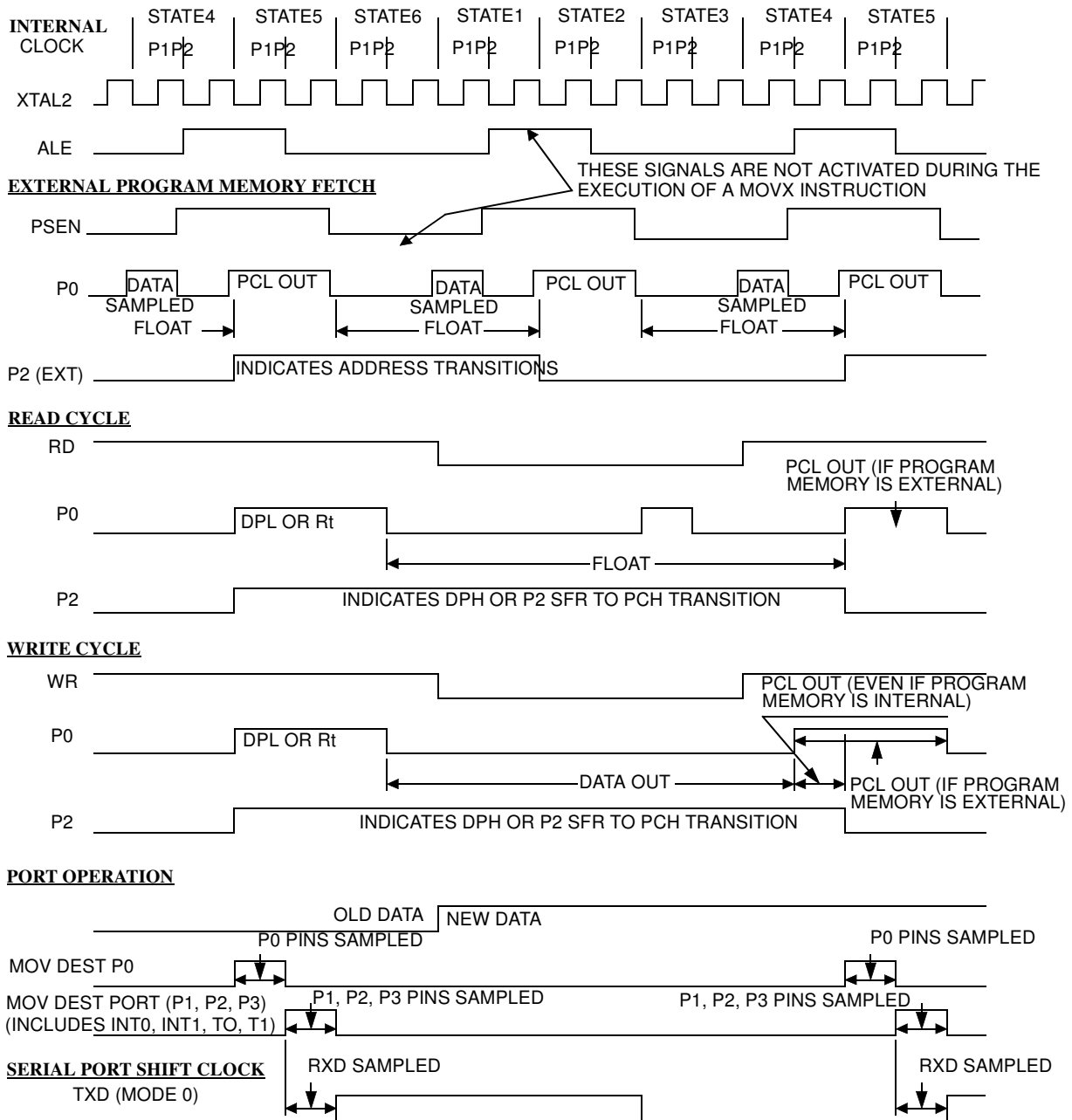


For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20mA$.

Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 signal must be changed to XTAL2 divided by two.

Figure 26. Clock Waveforms



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though ($T_A = 25^\circ\text{C}$ fully loaded) RD and WR propagation delays are approximately 50ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

Table 37. Possible Ordering Entries (Continued)

Part Number ⁽³⁾	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT80C52X2zzz-RLTUM	8K ROM	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	VQFP44	Tray
AT80C52X2zzz-3CSUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PDIL40	Stick
AT80C52X2zzz-SLSUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PLCC44	Stick
AT80C52X2zzz-RLTUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	VQFP44	Tray
AT80C52X2zzz-3CSUV	8K ROM	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	PDIL40	Stick
AT80C52X2zzz-SLSUV	8K ROM	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	PLCC44	Stick
AT80C52X2zzz-RLTUV	8K ROM	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	VQFP44	Tray
TS87C52X2-MCA	OBSOLETE					
TS87C52X2-MCB						
TS87C52X2-MCC						
TS87C52X2-MCE						
TS87C52X2-LCA						
TS87C52X2-LCB						
TS87C52X2-LCC						
TS87C52X2-LCE						
TS87C52X2-VCA						
TS87C52X2-VCB						
TS87C52X2-VCC						
TS87C52X2-VCE						
TS87C52X2-MIA						
TS87C52X2-MIB						
TS87C52X2-MIC						
TS87C52X2-MIE						
TS87C52X2-LIA						
TS87C52X2-LIB						
TS87C52X2-LIC						
TS87C52X2-LIE						
TS87C52X2-VIA						
TS87C52X2-VIB						
TS87C52X2-VIC						
TS87C52X2-VIE						
AT87C52X2-3CSUM	8K OTP	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	PDIL40	Stick

Table 37. Possible Ordering Entries (Continued)

Part Number ⁽³⁾	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT87C52X2-SLSUM	8K OTP	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	PLCC44	Stick
AT87C52X2-RLTUM	8K OTP	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	VQFP44	Tray
AT87C52X2-3CSUL	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PDIL40	Stick
AT87C52X2-SLSUL	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PLCC44	Stick
AT87C52X2-RLTUL	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	VQFP44	Tray
AT87C52X2-3CSUV	8K OTP	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	PDIL40	Stick
AT87C52X2-SLSUV	8K OTP	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	PLCC44	Stick
AT87C52X2-RLTUV	8K OTP	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	VQFP44	Tray

Notes: 1. 20 MHz in X2 Mode.
2. Tape and Reel available for SL, PQFP and RL packages
3. 30 MHz in X2 Mode.