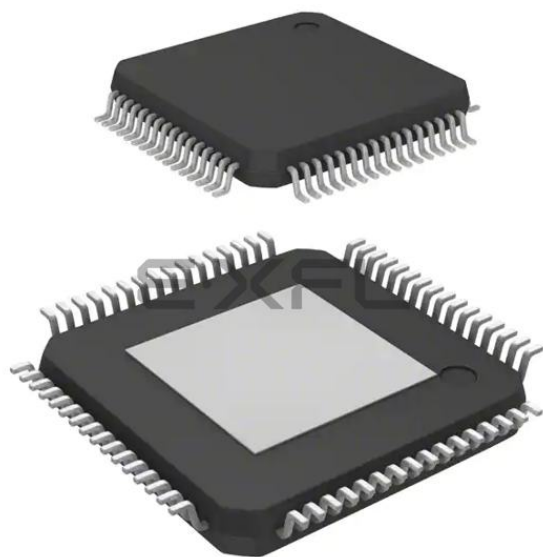




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I ² S, POR, PWM, WDT
Number of I/O	48
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1401f064f0064aaxuma1

XMC1400 Data Sheet
Revision History: V1.3 2016-10

Previous Versions:

V1.2 2016-08

V1.1 2016-06

V1.0 2016-02

V0.3 2015-10

Page	Subjects
42, 43	In Absolute Maximum Ratings renamed parameter V_{CM} to V_{INP2} , as the limitation is related to most P2 pins, also if no ACMP is available. Clarified limit to pins P2.[1,2,6:9,11] in Overload specification.
13	Corrected XMC1402-T038X0200 and XMC1402-Q048X0200 marking variants in Table 2
V1.2 2016-08	
many	Added XMC™ trademark
11, 13, 15	Added XMC1402-T038X0200, XMC1402-Q040X0200 and XMC1402-Q048X0200 marking variants
V1.1 2016-06	
many	Added TSSOP-38-9 package
11, 13, 15	Added XMC1402-T038 marking variants in TSSOP-38
11, 13, 15	Added XMC1403-Q040 marking variants
V1.0 2016-02	
10	The device provides four USIC channels.
11	XMC1401 devices available for max. ambient temperature of 85°C.
33	Reformatted pinout table.
58	Updated footnote to the definition of the start-up times of OSC_XTAL and RTC_XTAL oscillators.
73	Added Δf_{LT} parameter to on-chip oscillators DCO1 and DCO2.
85	Updated package outline drawings.

About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC1400 series devices.

The document describes the characteristics of a superset of the XMC1400 series devices. For simplicity, the various device types are referred to by the collective term XMC1400 throughout this document.

XMC1000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
 - describes the functionality of the superset of devices.
- **Data Sheets**
 - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
 - list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to <http://www.infineon.com/xmc1000> to get access to the latest versions of those documents.

Table 1 Features of XMC1400 Device Types¹⁾ (cont'd)

Features		XMC1401-Q048	XMC1401-F064	XMC1402-T038	XMC1402-Q040	XMC1402-Q048	XMC1402-Q064	XMC1402-F064	XMC1403-Q040	XMC1403-Q048	XMC1403-Q064	XMC1404-Q048	XMC1404-Q064	XMC1404-F064
Analog	ADC (kernels / analog inputs)	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12
	ACMP	-	-	3	3	4	4	4	-	-	-	4	4	4
GPIOs		34	48	26	27	34	48	48	27	34	48	34	48	48
GPIOs		8	8	8	8	8	8	8	8	8	8	8	8	8
Packages		VQFN-48	LQFP-64	TSSOP-38	VQFN-40	VQFN-48	VQFN-64	LQFP-64	VQFN-40	VQFN-48	VQFN-64	VQFN-48	VQFN-64	LQFP-64

1) Features that are not included in this table are available in all the derivatives

1.2 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code "XMC1<DDD>-<Z><PPP><T><FFFF>" identifies:

- <DDD> the derivatives function set
- <Z> the package variant
 - T: TSSOP
 - Q: VQFN
 - F: LQFP
- <PPP> package pin count
- <T> the temperature range:
 - F: -40°C to 85°C
 - X: -40°C to 105°C
- <FFFF> the Flash memory size in Kbytes.

For ordering codes for the XMC1400 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1400 series, some descriptions may not apply to a specific product. Please see [Table 2](#).

For simplicity the term **XMC1400** is used for all derivatives throughout this document.

1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is an 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location : 1000 0F00_H (MSB) - 1000 0F1B_H (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

Table 3 XMC1400 Chip Identification Number

Derivative	Value	Marking
XMC1401-Q048F0064	00014082 07CF00FF 1E071FF7 20006000 00000D00 00001000 00011000 10204083 _H	AA
XMC1401-Q048F0128	00014082 07CF00FF 1E071FF7 20006000 00000D00 00001000 00021000 10204083 _H	AA
XMC1401-F064F0064	000140A2 07CF00FF 1E071FF7 20006000 00000D00 00001000 00011000 10204083 _H	AA
XMC1401-F064F0128	000140A2 07CF00FF 1E071FF7 20006000 00000D00 00001000 00021000 10204083 _H	AA
XMC1402-T038X0032	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00009000 10204083 _H	AA
XMC1402-T038X0064	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00011000 10204083 _H	AA
XMC1402-T038X0128	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00021000 10204083 _H	AA
XMC1402-T038X0200	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00033000 10204083 _H	AA
XMC1402-Q040X0032	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00009000 10204083 _H	AA
XMC1402-Q040X0064	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00011000 10204083 _H	AA
XMC1402-Q040X0128	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00021000 10204083 _H	AA
XMC1402-Q040X0200	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00033000 10204083 _H	AA
XMC1402-Q048X0032	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00009000 10204083 _H	AA

Table 3 XMC1400 Chip Identification Number (cont'd)

Derivative	Value	Marking
XMC1402-Q048X0064	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00011000 10204083 _H	AA
XMC1402-Q048X0128	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00021000 10204083 _H	AA
XMC1402-Q048X0200	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00033000 10204083 _H	AA
XMC1402-Q064X0064	00014093 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00011000 10204083 _H	AA
XMC1402-Q064X0128	00014093 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00021000 10204083 _H	AA
XMC1402-Q064X0200	00014093 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00033000 10204083 _H	AA
XMC1402-F064X0064	000140A3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00011000 10204083 _H	AA
XMC1402-F064X0128	000140A3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00021000 10204083 _H	AA
XMC1402-F064X0200	000140A3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00033000 10204083 _H	AA
XMC1403-Q040X0064	00014043 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00011000 10204083 _H	AA
XMC1403-Q040X0128	00014043 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00021000 10204083 _H	AA
XMC1403-Q040X0200	00014043 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00033000 10204083 _H	AA
XMC1403-Q048X0064	00014083 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00011000 10204083 _H	AA
XMC1403-Q048X0128	00014083 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00021000 10204083 _H	AA
XMC1403-Q048X0200	00014083 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00033000 10204083 _H	AA
XMC1403-Q064X0064	00014093 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00011000 10204083 _H	AA
XMC1403-Q064X0128	00014093 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00021000 10204083 _H	AA

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

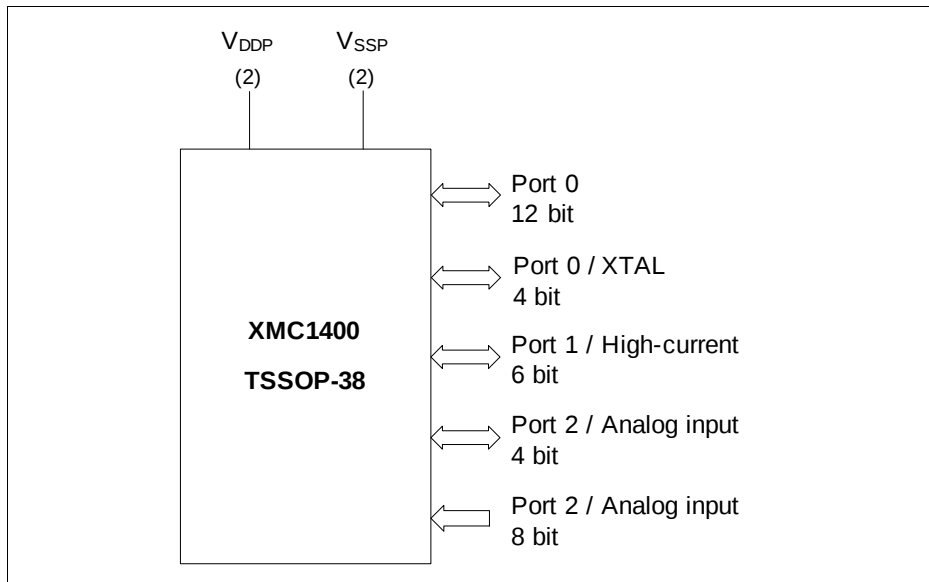


Figure 2 XMC1400 Logic Symbol for TSSOP-38-9

2.2.4 Hardware Controlled I/O Function Description

The following general building block is used to describe the hardware I/O and pull control functions of each PORT pin:

Table 8 Hardware Controlled I/O Function Description

Function	Outputs	Inputs	Pull Control	
	HWO0	HWI0	HW0_PD	HW0_PU
P0.0	MODB.OUT	MODB.INA		
Pn.y			MODC.OUT	MODC.OUT

By Pn_HWSEL, it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers. Additional hardware signals HW0_PD/HW1_PD and HW0_PU/HW1_PU controlled by the peripherals can be used to control the pull devices of the pin.

Please refer to the [Hardware Controlled I/O Functions](#) table for the complete hardware I/O and pull control function mapping.

Table 10 Hardware I/O Controlled Functions

Function	Outputs	Outputs	Inputs	Inputs	Pull Control	Pull Control	Pull Control	Pull Control
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P0.0	LEDS0. EXTENDED7		LEDS0.TSIN7	LEDS0.TSIN7	Reserved for LEDTS Scheme A: pull-down disabled always	Reserved for LEDTS Scheme A: pull-down enabled always	Reserved for LEDTS Scheme B: pull-up enabled and pull-down disabled, and vice versa	
P0.1	LEDS0. EXTENDED6		LEDS0.TSIN6	LEDS0.TSIN6				
P0.2	LEDS0. EXTENDED5		LEDS0.TSIN5	LEDS0.TSIN5				
P0.3	LEDS0. EXTENDED4		LEDS0.TSIN4	LEDS0.TSIN4				
P0.4	LEDS0. EXTENDED3		LEDS0.TSIN3	LEDS0.TSIN3				
P0.5	LEDS0. EXTENDED2		LEDS0.TSIN2	LEDS0.TSIN2				
P0.6	LEDS0. EXTENDED1		LEDS0.TSIN1	LEDS0.TSIN1				
P0.7	LEDS0. EXTENDED0		LEDS0.TSIN0	LEDS0.TSIN0				
P0.8	LEDS1. EXTENDED0		LEDS1.TSIN0	LEDS1.TSIN0				
P0.9	LEDS1. EXTENDED1		LEDS1.TSIN1	LEDS1.TSIN1				
P0.10	LEDS1. EXTENDED2		LEDS1.TSIN2	LEDS1.TSIN2				
P0.11	LEDS1. EXTENDED3		LEDS1.TSIN3	LEDS1.TSIN3				
P0.12	LEDS1. EXTENDED4		LEDS1.TSIN4	LEDS1.TSIN4				
P0.13	LEDS1. EXTENDED5		LEDS1.TSIN5	LEDS1.TSIN5				
P0.14	LEDS1. EXTENDED6		LEDS1.TSIN6	LEDS1.TSIN6				
P0.15	LEDS1. EXTENDED7		LEDS1.TSIN7	LEDS1.TSIN7				
P1.0		USIC0_CH0.DOUT0		USIC0_CH0.HWIN0	BCCU0.OUT2	BCCU0.OUT2		
P1.1		USIC0_CH0.DOUT1		USIC0_CH0.HWIN1	BCCU0.OUT3	BCCU0.OUT3		
P1.2		USIC0_CH0.DOUT2		USIC0_CH0.HWIN2	BCCU0.OUT4	BCCU0.OUT4		

3.2 DC Parameters

3.2.1 Input/Output Characteristics

Table 16 provides the characteristics of the input/output pins of the XMC1400.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.

Table 16 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Output low voltage on port pins (with standard pads)	V_{OLP}	CC	–	1.0	V	$I_{OL} = 11 \text{ mA}$ (5 V) $I_{OL} = 7 \text{ mA}$ (3.3 V)
			–	0.4	V	$I_{OL} = 5 \text{ mA}$ (5 V) $I_{OL} = 3.5 \text{ mA}$ (3.3 V)
Output low voltage on high current pads	V_{OLP1}	CC	–	1.0	V	$I_{OL} = 50 \text{ mA}$ (5 V) $I_{OL} = 25 \text{ mA}$ (3.3 V)
			–	0.32	V	$I_{OL} = 10 \text{ mA}$ (5 V)
			–	0.4	V	$I_{OL} = 5 \text{ mA}$ (3.3 V)
Output high voltage on port pins (with standard pads)	V_{OHP}	CC	$V_{DDP} - 1.0$	–	V	$I_{OH} = -10 \text{ mA}$ (5 V) $I_{OH} = -7 \text{ mA}$ (3.3 V)
			$V_{DDP} - 0.4$	–	V	$I_{OH} = -4.5 \text{ mA}$ (5 V) $I_{OH} = -2.5 \text{ mA}$ (3.3 V)
Output high voltage on high current pads	V_{OHP1}	CC	$V_{DDP} - 0.32$	–	V	$I_{OH} = -6 \text{ mA}$ (5 V)
			$V_{DDP} - 1.0$	–	V	$I_{OH} = -8 \text{ mA}$ (3.3 V)
			$V_{DDP} - 0.4$	–	V	$I_{OH} = -4 \text{ mA}$ (3.3 V)
Input low voltage on port pins (Standard Hysteresis)	V_{ILPS}	SR	–	$0.19 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input high voltage on port pins (Standard Hysteresis)	V_{IHPS}	SR	$0.7 \times V_{DDP}$	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)

Table 17 ADC Characteristics (Operating Conditions apply)¹⁾ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain settings	$G_{IN\ CC}$	1			–	GNCTRxz.GAINy = 00 _B (unity gain)
		3			–	GNCTRxz.GAINy = 01 _B (gain g1)
		6			–	GNCTRxz.GAINy = 10 _B (gain g2)
		12			–	GNCTRxz.GAINy = 11 _B (gain g3)
Sample Time	$t_{sample\ CC}$	5	–	–	1 / f_{ADC}	$V_{DD} = 5.0\ V$, $f_{ADCI} = 48\ MHz$
		3	–	–	1 / f_{ADC}	$V_{DD} = 5.0\ V$, $f_{ADCI} = 32\ MHz$
		3	–	–	1 / f_{ADC}	$V_{DD} = 3.3\ V$, $f_{ADCI} = 32\ MHz$
		30	–	–	1 / f_{ADC}	$V_{DD} = 2.0\ V$, $f_{ADCI} = 32\ MHz$
Conversion time in fast compare mode	$t_{CF\ CC}$	9			1 / f_{ADC}	³⁾
Conversion time in 12-bit mode	$t_{C12\ CC}$	20			1 / f_{ADC}	³⁾
Maximum sample rate in 12-bit mode ⁴⁾	$f_{C12\ CC}$	–	–	$f_{ADC} / 42.5$	–	1 sample pending
		–	–	$f_{ADC} / 62.5$	–	2 samples pending
Conversion time in 10-bit mode	$t_{C10\ CC}$	18			1 / f_{ADC}	³⁾
Maximum sample rate in 10-bit mode ⁴⁾	$f_{C10\ CC}$	–	–	$f_{ADC} / 40.5$	–	1 sample pending
		–	–	$f_{ADC} / 58.5$	–	2 samples pending
Conversion time in 8-bit mode	$t_{C8\ CC}$	16			1 / f_{ADC}	³⁾

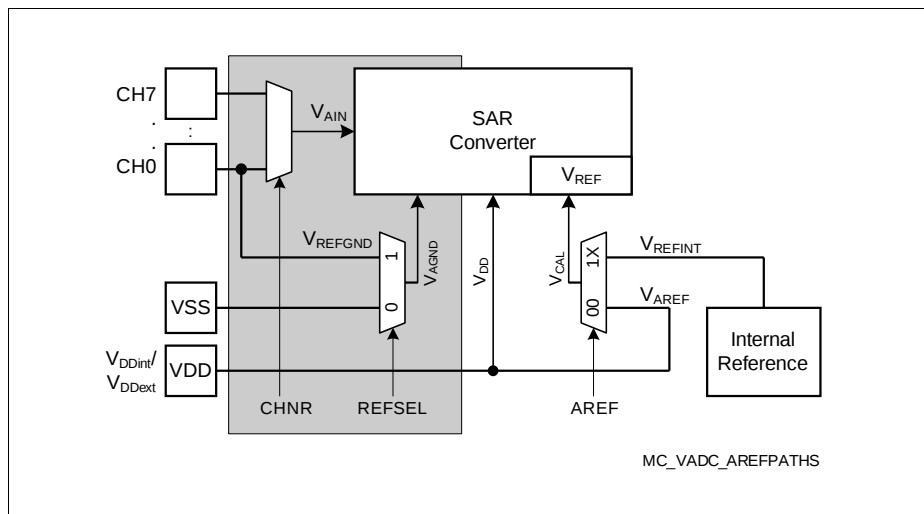


Figure 12 ADC Voltage Supply

3.2.5 Temperature Sensor Characteristics

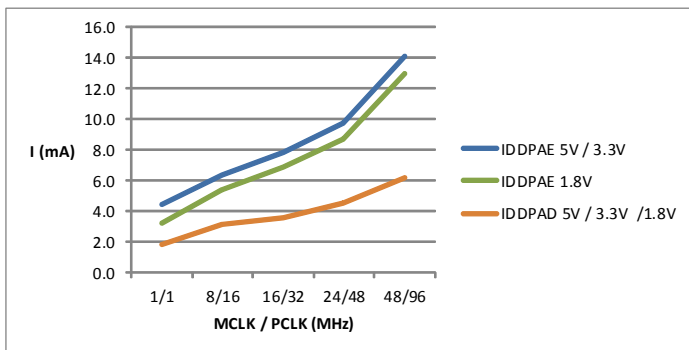
Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 20 Temperature Sensor Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	10	ms	
Temperature sensor range	T_{SR} SR	-40	–	115	°C	
Sensor Accuracy ¹⁾	T_{TSAL} CC	-6	–	6	°C	$T_J > 20^\circ\text{C}$
		-10	–	10	°C	$0^\circ\text{C} \leq T_J \leq 20^\circ\text{C}$
		–	-/+8	–	°C	$T_J < 0^\circ\text{C}$
Start-up time	t_{TSS} SR	–	–	15	μs	

1) The temperature sensor accuracy is independent of the supply voltage.

Figure 17 shows typical graphs for active mode supply current for $V_{DDP} = 5\text{ V}$, $V_{DDP} = 3.3\text{ V}$, $V_{DDP} = 1.8\text{ V}$ across different clock frequencies.



Condition
1. $T_A = +25^\circ\text{C}$

Figure 17 Active mode, a) peripherals clocks enabled, b) peripherals clocks disabled: Supply current I_{DDPA} over supply voltage V_{DDP} for different clock frequencies

Figure 18 shows typical graphs for sleep mode current for $V_{DDP} = 5\text{ V}$, $V_{DDP} = 3.3\text{ V}$, $V_{DDP} = 1.8\text{ V}$ across different clock frequencies.

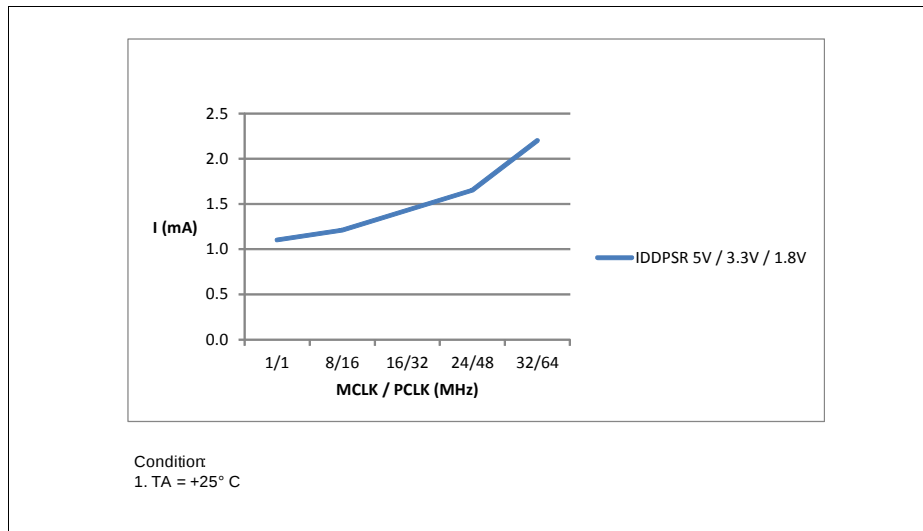


Figure 18 Sleep mode, peripherals clocks disabled, Flash powered down:
Supply current I_{DDPSD} over supply voltage V_{DDP} for different clock frequencies

3.2.8 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase time per page / sector	$t_{\text{ERASE CC}}$	6.8	7.1	7.6	ms	
Program time per block	$t_{\text{PSER CC}}$	102	152	204	μs	
Wake-Up time	$t_{\text{WU CC}}$	–	32.2	–	μs	
Read time per word	$t_{\text{a CC}}$	–	50	–	ns	
Data Retention Time	$t_{\text{RET CC}}$	10	–	–	years	Max. 100 erase / program cycles
Flash Wait States ¹⁾	$N_{\text{WSFLASH CC}}$	0	0	0		$f_{\text{MCLK}} = 8 \text{ MHz}$
		0	1	1		$f_{\text{MCLK}} = 16 \text{ MHz}$
		1	2	2		$f_{\text{MCLK}} = 32 \text{ MHz}$
		2	2	3		$f_{\text{MCLK}} = 48 \text{ MHz}$
Erase Cycles	$N_{\text{ECYC CC}}$	–	–	$5 \cdot 10^4$	cycles	Sum of page and sector erase cycles
Total Erase Cycles	$N_{\text{TECYC CC}}$	–	–	$2 \cdot 10^6$	cycles	

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

3.3.2 Power-Up and Supply Threshold Characteristics

Table 26 provides the characteristics of the supply threshold in XMC1400.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DDP} is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 26 Power-Up and Supply Threshold Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} ramp-up time	t_{RAMPUP} SR	$V_{DDP}/S_{VDDPrise}$	–	10^7	μs	
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	$V/\mu s$	Slope during normal operation
	S_{VDDP10} SR	0	–	10	$V/\mu s$	Slope during fast transient within +/- 10% of V_{DDP}
	$S_{VDDPrise}$ SR	0	–	10	$V/\mu s$	Slope during power-on or restart after brownout event
	$S_{VDDPfall}^{1)}$ SR	0	–	0.25	$V/\mu s$	Slope during supply falling out of the +/- 10% limits ²⁾
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00 _B
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01 _B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10 _B

Table 32 USIC SSC Slave Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 hold after last clock input DX1 receive edge ¹⁾	t_{11} SR	17	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge ¹⁾	t_{12} SR	21	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge ¹⁾	t_{13} SR	15	–	–	ns	
Data output DOUT[3:0] valid time	t_{14} CC	-	–	71	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

Table 34 USIC IIC Fast Mode Timing¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + $0.1 \cdot C_b$ ²⁾	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + $0.1 \cdot C_b$	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	μs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	μs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	μs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	μs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	μs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	μs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	μs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

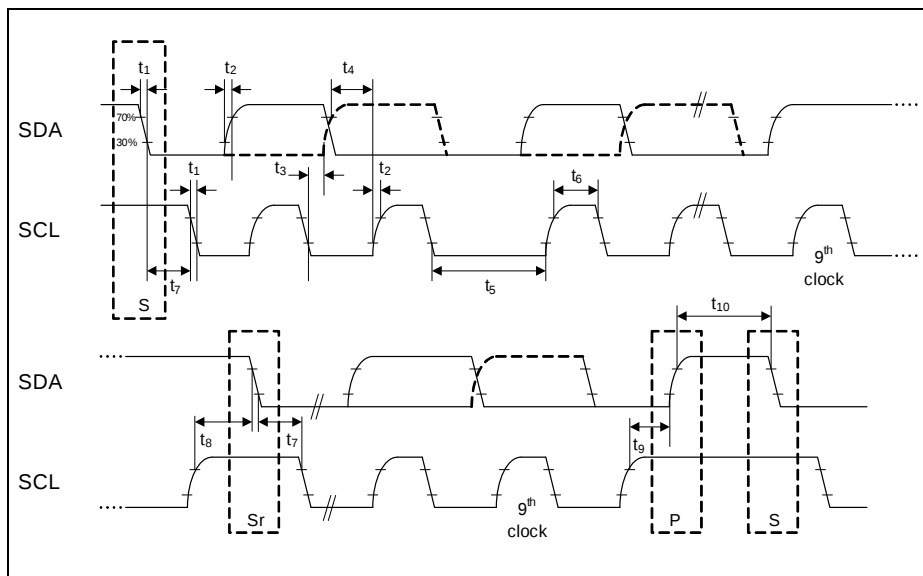


Figure 26 USIC IIC Timing

3.3.6.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: Operating Conditions apply.

Table 35 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	t_2 CC	$0.35 \times t_{1min}$	-	-	ns	
Clock Low	t_3 CC	$0.35 \times t_{1min}$	-	-	ns	
Hold time	t_4 CC	0	-	-	ns	
Clock rise time	t_5 CC	-	-	$0.15 \times t_{1min}$	ns	

4 Package and Reliability

The XMC1400 is a member of the XMC1000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 37 provides the thermal characteristics of the packages used in XMC1400.

Table 37 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	3.7 × 3.7	mm	PG-VQFN-40-17
		-	4.2 × 4.2	mm	PG-VQFN-48-73
		-	4.6 × 4.6	mm	PG-VQFN-64-6
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	86.0	K/W	PG-TSSOP-38-9 ¹⁾
		-	45.3	K/W	PG-VQFN-40-17 ¹⁾
		-	44.9	K/W	PG-VQFN-48-73 ¹⁾
		-	66.7	K/W	PG-LQFP-64-26 ¹⁾
		-	44.7	K/W	PG-VQFN-64-6 ¹⁾

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SSP} , independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC1400 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The "Thermal resistance $R_{\Theta JA}$ " quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.