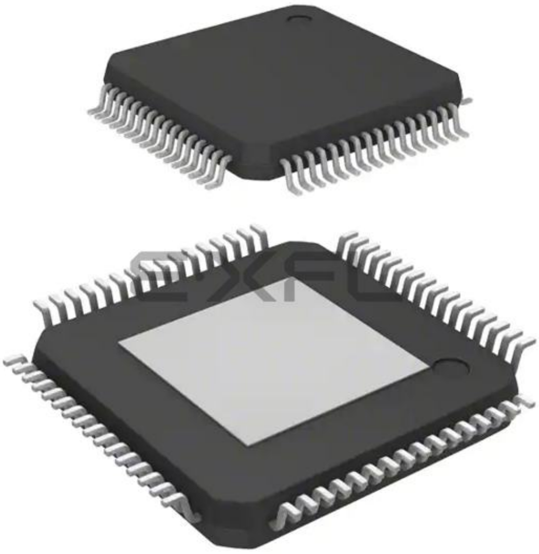

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1401f064f0128aaxuma1

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1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is an 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location : 1000 $0F00_H$ (MSB) - 1000 $0F1B_H$ (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

Table 3 XMC1400 Chip Identification Number

Derivative	Value	Marking
XMC1401-Q048F0064	00014082 07CF00FF 1E071FF7 20006000 00000D00 00001000 00011000 10204083_H	AA
XMC1401-Q048F0128	00014082 07CF00FF 1E071FF7 20006000 00000D00 00001000 00021000 10204083_H	AA
XMC1401-F064F0064	000140A2 07CF00FF 1E071FF7 20006000 00000D00 00001000 00011000 10204083_H	AA
XMC1401-F064F0128	000140A2 07CF00FF 1E071FF7 20006000 00000D00 00001000 00021000 10204083_H	AA
XMC1402-T038X0032	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00009000 10204083_H	AA
XMC1402-T038X0064	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00011000 10204083_H	AA
XMC1402-T038X0128	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00021000 10204083_H	AA
XMC1402-T038X0200	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00033000 10204083_H	AA
XMC1402-Q040X0032	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00009000 10204083_H	AA
XMC1402-Q040X0064	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00011000 10204083_H	AA
XMC1402-Q040X0128	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00021000 10204083_H	AA
XMC1402-Q040X0200	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00033000 10204083_H	AA
XMC1402-Q048X0032	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00009000 10204083_H	AA

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

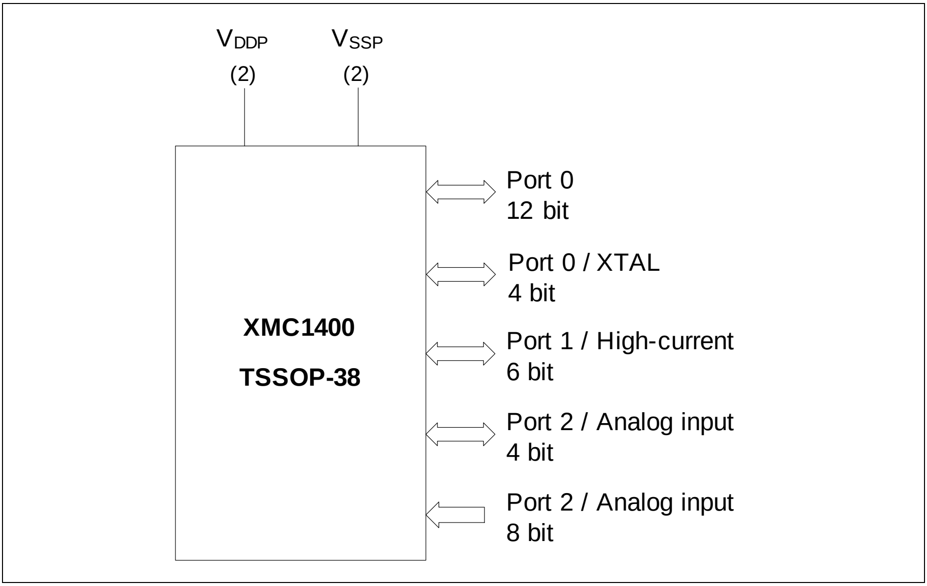


Figure 2 XMC1400 Logic Symbol for TSSOP-38-9

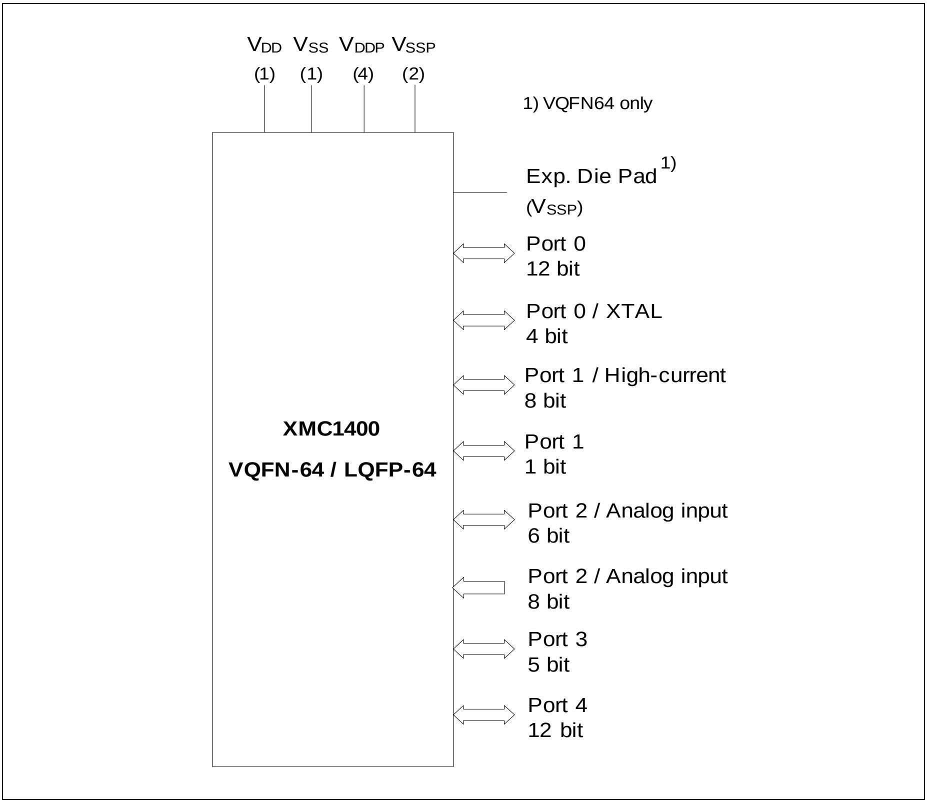


Figure 5 XMC1400 Logic Symbol for PG-LQFP-64-26 / PG-VQFN-64-6

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

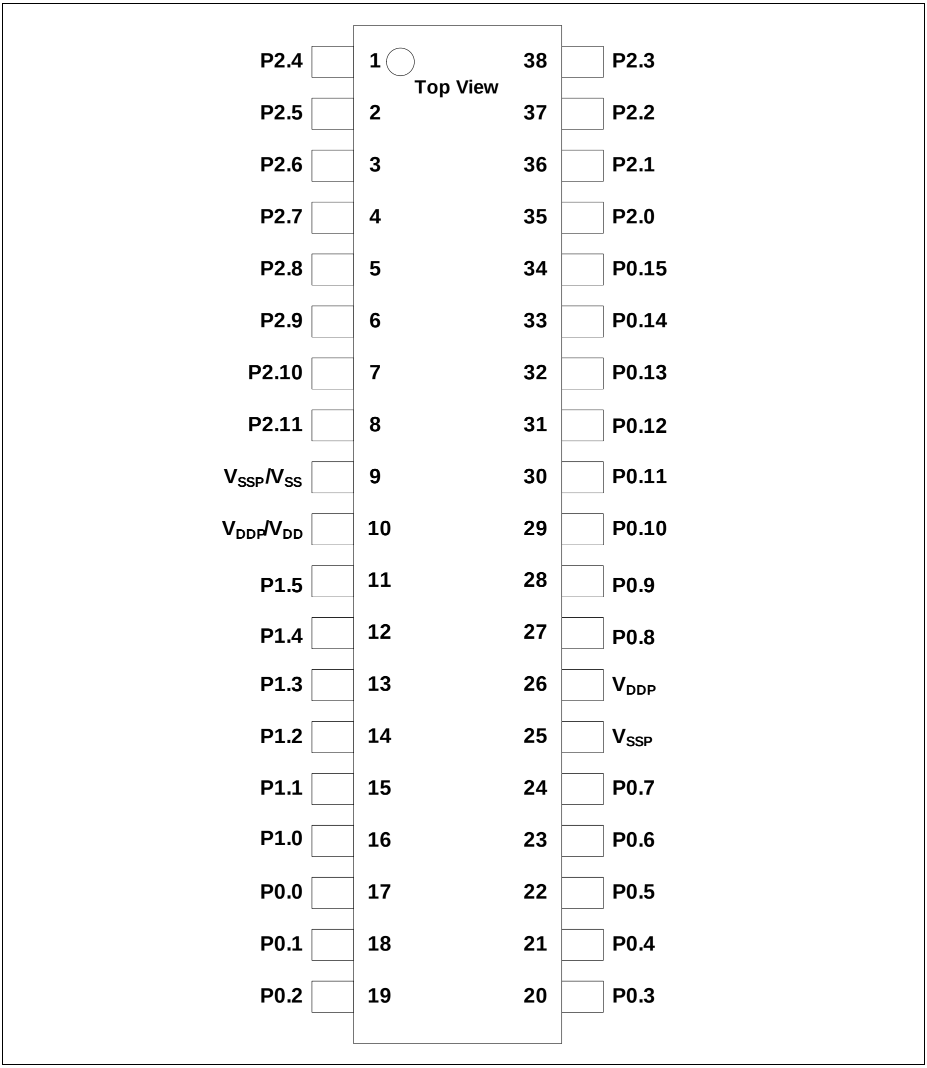


Figure 6 XMC1400 PG-TSSOP-38-9 Pin Configuration (top view)

2.2.2 Port Pin for Boot Modes

Port functions can be overruled by the boot mode selected. The type of boot mode is selected via BMI. **Table 6** shows the port pins used for the various boot modes.

Table 6 Port Pin for Boot Modes

Pin	Boot	Boot Description
P0.13	CS(O)	SSC BSL mode
P0.14	SWDIO_0	Debug mode (SWD)
	SPD_0	Debug mode (SPD)
	RX/TX	ASC BSL half-duplex mode
	RX	ASC BSL full-duplex mode
	RX	CAN BSL mode
	SCLK(O)	SSC BSL mode
P0.15	SWDCLK_0	Debug mode (SWD)
	TX	ASC BSL full-duplex mode
	TX	CAN BSL mode
	DATA(I/O)	SSC BSL mode
P1.2	SWDCLK_1	Debug mode (SWD)
	TX	ASC BSL full-duplex mode
	TX	CAN BSL mode
P1.3	SWDIO_1	Debug mode (SWD)
	SPD_1	Debug mode (SPD)
	RX/TX	ASC BSL half-duplex mode
	RX	ASC BSL full-duplex mode
	RX	CAN BSL mode
P4.6	HWCON0	Boot Pins (Boot from pins mode must be selected)
P4.7	HWCON1	

Table 9 Port I/O Functions (cont'd)

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P3.2	BCCU0.OUT2	USIC1_CH1.SCLKOUT		LEDTS2.COL1	CCU80.OUT11	ACMP2.OUT	USIC1_CH0.SCLKOUT	CCU81.OUT11	CCU41.OUT2							USIC1_CH0.DX3C	USIC1_CH0.DX4C	USIC1_CH1.DX3D	USIC1_CH1.DX4D		ERU1.2A1
P3.3	BCCU0.OUT5	USIC1_CH0.DOUT0		LEDTS2.COL2	CCU80.OUT10	ACMP0.OUT	USIC1_CH1.SELO0	CCU81.OUT10	CCU41.OUT3							USIC1_CH0.DX0E			USIC1_CH1.DX2A		ERU1.1A3
P3.4	BCCU0.OUT6	USIC1_CH0.DOUT0	USIC1_CH0.SCLKOUT	LEDTS2.COL3	CCU80.OUT01	USIC1_CH1.MCLKOUT	USIC1_CH1.SELO1	CCU81.OUT01								USIC1_CH0.DX0F	USIC1_CH0.DX1E		USIC1_CH1.DX2B		ERU1.2A3
P4.0	BCCU0.OUT0	ERU1.PDOUT0	LEDTS2.COL5	ERU1.GOUT0	CCU40.OUT0	ACMP1.OUT	USIC1_CH1.SELO1	CCU81.OUT10	CCU41.OUT0		CCU40.IN0BA	CCU41.IN0AC	CCU80.IN0AU			USIC1_CH0.DX3D	USIC1_CH0.DX4D				
P4.1	BCCU0.OUT8	ERU1.PDOUT1	LEDTS2.COL4	ERU1.GOUT1	CCU40.OUT1	ACMP3.OUT	USIC1_CH1.SELO2	CCU81.OUT11	CCU41.OUT1		CCU40.IN1BA	CCU41.IN1AC	CCU80.IN1AU		POSIF1.IN0B	USIC1_CH0.DX5C					
P4.2	BCCU0.OUT4	ERU1.PDOUT2	CCU81.OUT20	ERU1.GOUT2	CCU40.OUT2	ACMP2.OUT	USIC1_CH1.SELO3	CCU81.OUT12	CCU41.OUT2		CCU40.IN2BA	CCU41.IN2AC	CCU80.IN2AU	CCU81.IN1AB	POSIF1.IN1B	USIC1_CH0.DX5D					
P4.3	BCCU0.OUT5	ERU1.PDOUT3	CCU81.OUT21	ERU1.GOUT3	CCU40.OUT3	ACMP0.OUT	USIC1_CH0.SCLKOUT	CCU81.OUT13	CCU41.OUT3		CCU40.IN3BA	CCU41.IN3AC	CCU80.IN3AU		POSIF1.IN2B		USIC1_CH0.DX1B				
P4.4	BCCU0.OUT0	LEDTS2.LINE0		LEDTS1.COLA	CCU80.OUT00	USIC1_CH0.DOUT0		CCU81.OUT00	CCU41.OUT0			CCU41.IN0AV				USIC1_CH0.DX0C		USIC1_CH1.DX5F			ERU1.0A2
P4.5	BCCU0.OUT8	LEDTS2.LINE1		LEDTS1.COL6	CCU80.OUT01	USIC1_CH0.DOUT0	USIC1_CH0.SCLKOUT	CCU81.OUT01	CCU41.OUT1			CCU41.IN1AV				USIC1_CH0.DX0D	USIC1_CH0.DX1C				ERU1.1A2
P4.6	BCCU0.OUT2	LEDTS2.LINE2	CCU81.OUT10	LEDTS1.COL5	CCU80.OUT10		USIC1_CH0.SCLKOUT	CCU81.OUT02	CCU41.OUT2			CCU41.IN2AV		CCU81.IN0AB			USIC1_CH0.DX1D				ERU1.2A2
P4.7	BCCU0.OUT5	LEDTS2.LINE3	CCU81.OUT11	LEDTS1.COL4	CCU80.OUT11		USIC1_CH0.SELO0	CCU81.OUT03	CCU41.OUT3			CCU41.IN3AV					USIC1_CH0.DX2A				ERU1.0A3
P4.8	BCCU0.OUT7	LEDTS2.LINE4	LEDTS2.COL3	LEDTS1.COL3	CCU80.OUT30	CCU40.OUT0	USIC1_CH0.SELO1	CCU81.OUT30	CAN.N1_TXD		CCU40.IN0AV	CCU41.IN0BA					USIC1_CH0.DX2B			CAN.N1_RXDC	
P4.9	BCCU0.OUT3	LEDTS2.LINE5	LEDTS2.COL2	LEDTS1.COL2	CCU80.OUT31	CCU40.OUT1	USIC1_CH0.SELO2	CCU81.OUT31	CAN.N1_TXD		CCU40.IN1AV	CCU41.IN1BA					USIC1_CH0.DX2C			CAN.N1_RXDD	

Table 10 Hardware I/O Controlled Functions

Function	Outputs	Outputs	Inputs	Inputs	Pull Control	Pull Control	Pull Control	Pull Control
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P0.0	LEDTS0. EXTENDED7		LEDTS0.TSIN7	LEDTS0.TSIN7	Reserved for LEDTS Scheme A: pull-down disabled always	Reserved for LEDTS Scheme A: pull-down enabled always	Reserved for LEDTS Scheme B: pull-up enabled and pull-down disabled, and vice versa	
P0.1	LEDTS0. EXTENDED6		LEDTS0.TSIN6	LEDTS0.TSIN6				
P0.2	LEDTS0. EXTENDED5		LEDTS0.TSIN5	LEDTS0.TSIN5				
P0.3	LEDTS0. EXTENDED4		LEDTS0.TSIN4	LEDTS0.TSIN4				
P0.4	LEDTS0. EXTENDED3		LEDTS0.TSIN3	LEDTS0.TSIN3				
P0.5	LEDTS0. EXTENDED2		LEDTS0.TSIN2	LEDTS0.TSIN2				
P0.6	LEDTS0. EXTENDED1		LEDTS0.TSIN1	LEDTS0.TSIN1				
P0.7	LEDTS0. EXTENDED0		LEDTS0.TSIN0	LEDTS0.TSIN0				
P0.8	LEDTS1. EXTENDED0		LEDTS1.TSIN0	LEDTS1.TSIN0				
P0.9	LEDTS1. EXTENDED1		LEDTS1.TSIN1	LEDTS1.TSIN1				
P0.10	LEDTS1. EXTENDED2		LEDTS1.TSIN2	LEDTS1.TSIN2				
P0.11	LEDTS1. EXTENDED3		LEDTS1.TSIN3	LEDTS1.TSIN3				
P0.12	LEDTS1. EXTENDED4		LEDTS1.TSIN4	LEDTS1.TSIN4				
P0.13	LEDTS1. EXTENDED5		LEDTS1.TSIN5	LEDTS1.TSIN5				
P0.14	LEDTS1. EXTENDED6		LEDTS1.TSIN6	LEDTS1.TSIN6				
P0.15	LEDTS1. EXTENDED7		LEDTS1.TSIN7	LEDTS1.TSIN7				
P1.0		USIC0_CH0.DOUT0		USIC0_CH0.HWIN0	$\overline{\text{BCCU0.OUT2}}$	BCCU0.OUT2		
P1.1		USIC0_CH0.DOUT1		USIC0_CH0.HWIN1	$\overline{\text{BCCU0.OUT3}}$	BCCU0.OUT3		
P1.2		USIC0_CH0.DOUT2		USIC0_CH0.HWIN2	$\overline{\text{BCCU0.OUT4}}$	BCCU0.OUT4		

Table 10 Hardware I/O Controlled Functions

Function	Outputs	Outputs	Inputs	Inputs	Pull Control	Pull Control	Pull Control	Pull Control
	HWO0	**HWO1**	**HWI0**	**HWI1**	**HW0_PD**	**HW0_PU**	**HW1_PD**	**HW1_PU**
P4.4	LEDTS2.EXTENDED0		LEDTS2.TSIN0	LEDTS2.TSIN0	Reserved for LEDTS Scheme A: pull-down disabled always	Reserved for LEDTS Scheme A: pull-down enabled always	Reserved for LEDTS Scheme B: pull-up enabled and pull-down disabled, and vice versa	
P4.5	LEDTS2.EXTENDED1		LEDTS2.TSIN1	LEDTS2.TSIN1				
P4.6	LEDTS2.EXTENDED2		LEDTS2.TSIN2	LEDTS2.TSIN2				
P4.7	LEDTS2.EXTENDED3		LEDTS2.TSIN3	LEDTS2.TSIN3				
P4.8	LEDTS2.EXTENDED4		LEDTS2.TSIN4	LEDTS2.TSIN4				
P4.9	LEDTS2.EXTENDED5		LEDTS2.TSIN5	LEDTS2.TSIN5				
P4.10	LEDTS2.EXTENDED6		LEDTS2.TSIN6	LEDTS2.TSIN6				
P4.11	LEDTS2.EXTENDED7		LEDTS2.TSIN7	LEDTS2.TSIN7				

3.2.2 Analog to Digital Converters (ADC)

Table 17 shows the Analog to Digital Converter (ADC) characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 17 ADC Characteristics (Operating Conditions apply)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	V_{DD_int} SR	2.0	–	3.0	V	SHSCFG.AREF = 11_B; CALCTR.CALGNSTC = $0C_H$ for f_{SH} = 32 MHz, 12_H for f_{SH} = 48 MHz
		3.0	–	5.5	V	SHSCFG.AREF = 10_B
Supply voltage range (external reference)	V_{DD_ext} SR	3.0	–	5.5	V	SHSCFG.AREF = 00_B
Analog input voltage range	V_{AIN} SR	V_{SSP} - 0.05	–	V_{DDP} + 0.05	V	
Auxiliary analog reference ground[2)]	V_{REFGND} SR	V_{SSP} - 0.05	–	1.0	V	G0CH0
		V_{SSP} - 0.05	–	0.2	V	G1CH0
Internal reference voltage (full scale value)	V_{REFINT} CC		5		V	
Switched capacitance of an analog input	C_{AINS} CC	–	1.2	2	pF	GNCTRxz.GAINy = 00_B (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01_B (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10_B (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11_B (gain g3)
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	

Table 17 ADC Characteristics (Operating Conditions apply)[1) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain settings	G_{IN} CC		1		–	GNCTRxz.GAINy = 00_B (unity gain)
			3		–	GNCTRxz.GAINy = 01_B (gain g1)
			6		–	GNCTRxz.GAINy = 10_B (gain g2)
			12		–	GNCTRxz.GAINy = 11_B (gain g3)
Sample Time	t_{sample} CC	5	–	–	1 / f_{ADC}	V_{DD} = 5.0 V, f_{ADCI} = 48 MHz
		3	–	–	1 / f_{ADC}	V_{DD} = 5.0 V, f_{ADCI} = 32 MHz
		3	–	–	1 / f_{ADC}	V_{DD} = 3.3 V, f_{ADCI} = 32 MHz
		30	–	–	1 / f_{ADC}	V_{DD} = 2.0 V, f_{ADCI} = 32 MHz
Conversion time in fast compare mode	t_{CF} CC		9		1 / f_{ADC}	3)
Conversion time in 12-bit mode	t_{C12} CC		20		1 / f_{ADC}	3)
Maximum sample rate in 12-bit mode[4)	f_{C12} CC	–	–	f_{ADC} / 42.5	–	1 sample pending
		–	–	f_{ADC} / 62.5	–	2 samples pending
Conversion time in 10-bit mode	t_{C10} CC		18		1 / f_{ADC}	3)
Maximum sample rate in 10-bit mode[4)	f_{C10} CC	–	–	f_{ADC} / 40.5	–	1 sample pending
		–	–	f_{ADC} / 58.5	–	2 samples pending
Conversion time in 8-bit mode	t_{C8} CC		16		1 / f_{ADC}	3)

Table 17 ADC Characteristics (Operating Conditions apply)[1] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum sample rate in 8-bit mode[4]	f_{C8} CC	–	–	f_{ADC} / 38.5	–	1 sample pending
		–	–	f_{ADC} / 54.5	–	2 samples pending
RMS noise[5]	EN_{RMS} CC	–	1.5	–	LSB 12	DC input, SHSCFG.AREF = 00_B, GNCTRxz.GAINy = 00_B (unity gain), V_{DD} = 5.0 V, V_{AIN} = 2.5 V, 25°C
DNL error	EA_{DNL} CC	–	±2.0	–	LSB 12	
INL error	EA_{INL} CC	–	±4.0	–	LSB 12	
Gain error with external reference	EA_{GAIN} CC	–	±0.5	–	%	SHSCFG.AREF = 00_B (calibrated)
Gain error with internal reference[6]	EA_{GAIN} CC	–	±3.6	–	%	SHSCFG.AREF = $1X_B$ (calibrated), -40°C - 110°C
		–	±2.0	–	%	SHSCFG.AREF = $1X_B$ (calibrated), 0°C - 85°C
Offset error	EA_{OFF} CC	–	±8.0	–	mV	Calibrated, V_{DD} = 5.0 V

1) The parameters are defined for ADC clock frequencies f_{SH} = 32 MHz for the full supply range, and f_{SH} = 48 MHz at V_{DD_int}, V_{DD_ext} = 5 V. Usage of any other frequencies may affect the ADC performance.

2) The alternate reference ground connection is separate for each converter. This mode, therefore, provides the lowest noise impact.

3) No pending samples assumed, excluding sampling time and calibration.

4) Includes synchronization and calibration (average of gain and offset calibration).

5) This parameter can also be defined as an SNR value: SNR[dB] = 20 × log(A_{MAXeff} / N_{RMS}).
With A_{MAXeff} = 2^N / 2, SNR[dB] = 20 × log (2048 / N_{RMS}) [N = 12].
N_{RMS} = 1.5 LSB12, therefore, equals SNR = 20 × log (2048 / 1.5) = 62.7 dB.

6) Includes error from the reference voltage.

3.2.5 Temperature Sensor Characteristics

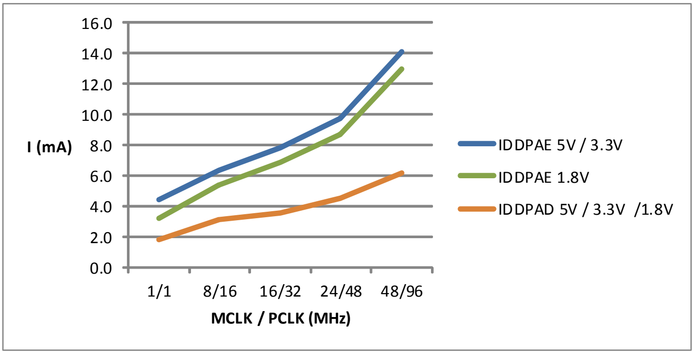
Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 20 Temperature Sensor Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	10	ms	
Temperature sensor range	T_{SR} SR	-40	–	115	°C	
Sensor Accuracy[1)]	T_{TSAL} CC	-6	–	6	°C	T_J > 20°C
		-10	–	10	°C	0°C ≤ T_J ≤ 20°C
		–	-/+8	–	°C	T_J < 0°C
Start-up time	t_{TSST} SR	–	–	15	µs	

1) The temperature sensor accuracy is independent of the supply voltage.

Figure 17 shows typical graphs for active mode supply current for V_{DDP} = 5 V, V_{DDP} = 3.3 V, V_{DDP} = 1.8 V across different clock frequencies.



Condition:
1. TA = +25° C

Figure 17 Active mode, a) peripherals clocks enabled, b) peripherals clocks disabled: Supply current I_{DDPA} over supply voltage V_{DDP} for different clock frequencies

3.3.3 On-Chip Oscillator Characteristics

Table 27 provides the characteristics of the 96 MHz digital controlled oscillator DCO1.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 27 96 MHz DCO1 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	–	96	–	MHz	under nominal conditions[1] after trimming
Accuracy with adjustment based on XTAL as reference	Δf_{LTX}	CC	-0.3	–	0.3	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0 °C to 85 °C)
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

Table 28 provides the characteristics of the 32 kHz digital controlled oscillator DCO2.

Table 28 32 kHz DCO2 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	–	32.75	–	kHz	under nominal conditions[1] after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0 °C to 85 °C)
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)[1]

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

3.3.6.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 33 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

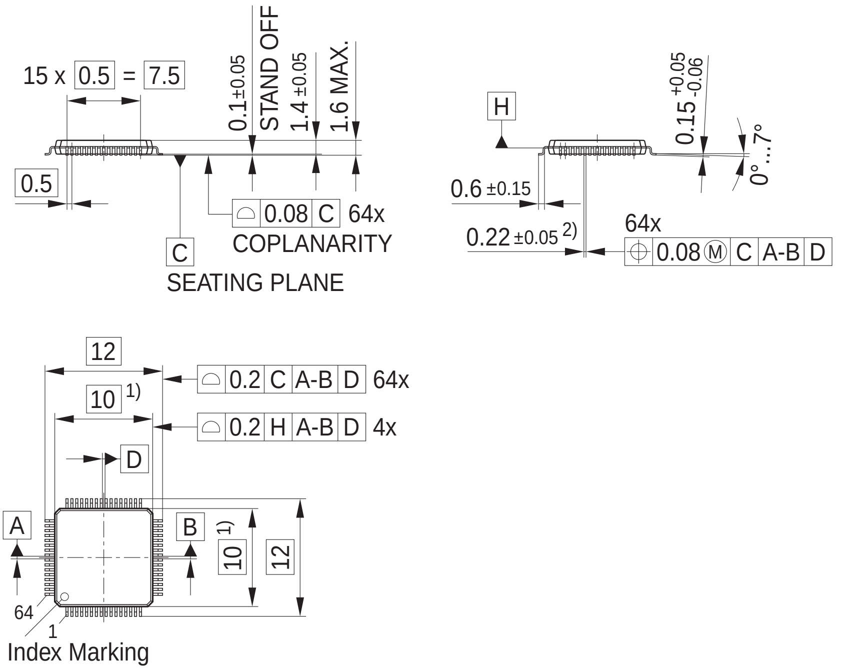
1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

Table 34 USIC IIC Fast Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1*C_b	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

PG-LQFP-64-10, -21, -26-PO V03

Figure 32 PG-LQFP-64-26

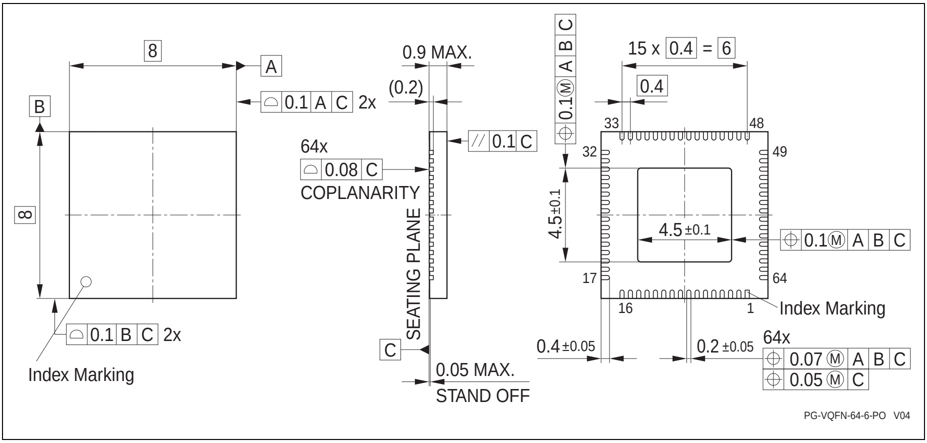


Figure 33 PG-VQFN-64-6

All dimensions in mm.

5 Quality Declaration

Table 38 shows the characteristics of the quality parameters in the XMC1400.

Table 38 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	-	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	-	3	-	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	-	260	°C	Profile according to JEDEC J-STD-020D