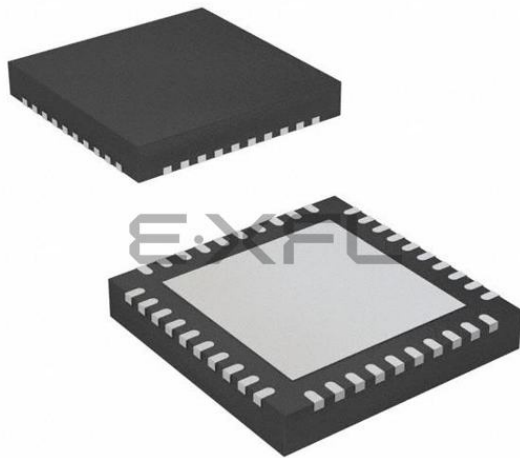




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I ² S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VQFN Exposed Pad
Supplier Device Package	PG-VQFN-40-17
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1402q040x0032aaxuma1

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About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC1400 series devices.

The document describes the characteristics of a superset of the XMC1400 series devices. For simplicity, the various device types are referred to by the collective term XMC1400 throughout this document.

XMC1000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
 - describes the functionality of the superset of devices.
- **Data Sheets**
 - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
 - list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to <http://www.infineon.com/xmc1000> to get access to the latest versions of those documents.

1.1 Device Overview

The following table lists the available features per device type for the XMC1400 series.

Table 1 Features of XMC1400 Device Types¹⁾

Features		XMC1401-Q048	XMC1401-F064	XMC1402-T038	XMC1402-Q040	XMC1402-Q048	XMC1402-Q064	XMC1402-F064	XMC1403-Q040	XMC1403-Q048	XMC1403-Q064	XMC1404-Q048	XMC1404-Q064	XMC1404-F064
CPU frequency		48 MHz												
Operating temperature (ambient)		-40 to 85 °C		-40 to 105 °C										
Operating voltage		1.8 V to 5.5 V												
Flash options (Kbytes)		64, 128	64, 128	32, 64, 128 200	32, 64, 128 200	32, 64, 128 200	64, 128 200	64, 128 200	64, 128 200	64, 128 200	64, 128 200	64, 128 200	64, 128 200	64, 128 200
SRAM (Kbytes)		16	16	16	16	16	16	16	16	16	16	16	16	16
MATH		-	-	1	1	1	1	1	-	-	-	1	1	1
Industrial Control	CCU4	2	2	2	2	2	2	2	2	2	2	2	2	2
	CCU8	-	-	2	2	2	2	2	-	-	-	2	2	2
	POSIF	-	-	1	1	2	2	2	-	-	-	2	2	2
	BCCU	-	-	1	1	1	1	1	-	-	-	1	1	1
Communication	USIC (modules / channels)	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2
	LEDTS	3	3	-	-	-	-	-	-	-	-	3	3	3
	MultiCAN+ (nodes / MOs)	-	-	-	-	-	-	-	2 / 32	2 / 32	2 / 32	2 / 32	2 / 32	2 / 32

Table 1 Features of XMC1400 Device Types¹⁾ (cont'd)

Features		XMC1401-Q048	XMC1401-F064	XMC1402-T038	XMC1402-Q040	XMC1402-Q048	XMC1402-Q064	XMC1402-F064	XMC1403-Q040	XMC1403-Q048	XMC1403-Q064	XMC1404-Q048	XMC1404-Q064	XMC1404-F064
Analog	ADC (kernels / analog inputs)	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12
	ACMP	-	-	3	3	4	4	4	-	-	-	4	4	4
GPIOs		34	48	26	27	34	48	48	27	34	48	34	48	48
GPIOs		8	8	8	8	8	8	8	8	8	8	8	8	8
Packages		VQFN-48	LQFP-64	TSSOP-38	VQFN-40	VQFN-48	VQFN-64	LQFP-64	VQFN-40	VQFN-48	VQFN-64	VQFN-48	VQFN-64	LQFP-64

1) Features that are not included in this table are available in all the derivatives

1.2 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code "XMC1<DDD>-<Z><PPP><T><FFFF>" identifies:

- <DDD> the derivatives function set
- <Z> the package variant
 - T: TSSOP
 - Q: VQFN
 - F: LQFP
- <PPP> package pin count
- <T> the temperature range:
 - F: -40°C to 85°C
 - X: -40°C to 105°C
- <FFFF> the Flash memory size in Kbytes.

For ordering codes for the XMC1400 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1400 series, some descriptions may not apply to a specific product. Please see [Table 2](#).

For simplicity the term **XMC1400** is used for all derivatives throughout this document.

1.3 Device Types

These device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 2 Synopsis of XMC1400 Device Types

Derivative	Package	Flash Kbytes
XMC1401-Q048F0064	PG-VQFN-48	64
XMC1401-Q048F0128	PG-VQFN-48	128
XMC1401-F064F0064	PG-LQFP-64	64
XMC1401-F064F0128	PG-LQFP-64	128
XMC1402-T038X0032	PG-TSSOP-38	32
XMC1402-T038X0064	PG-TSSOP-38	64
XMC1402-T038X0128	PG-TSSOP-38	128
XMC1402-T038X0200	PG-TSSOP-38	200
XMC1402-Q040X0032	PG-VQFN-40	32
XMC1402-Q040X0064	PG-VQFN-40	64
XMC1402-Q040X0128	PG-VQFN-40	128
XMC1402-Q040X0200	PG-VQFN-40	200
XMC1402-Q048X0032	PG-VQFN-48	32
XMC1402-Q048X0064	PG-VQFN-48	64
XMC1402-Q048X0128	PG-VQFN-48	128
XMC1402-Q048X0200	PG-VQFN-48	200
XMC1402-Q064X0064	PG-VQFN-64	64
XMC1402-Q064X0128	PG-VQFN-64	128
XMC1402-Q064X0200	PG-VQFN-64	200
XMC1402-F064X0064	PG-LQFP-64	64
XMC1402-F064X0128	PG-LQFP-64	128
XMC1402-F064X0200	PG-LQFP-64	200
XMC1403-Q040X0064	PG-VQFN-40	64
XMC1403-Q040X0128	PG-VQFN-40	128
XMC1403-Q040X0200	PG-VQFN-40	200
XMC1403-Q048X0064	PG-VQFN-48	64
XMC1403-Q048X0128	PG-VQFN-48	128

Table 3 XMC1400 Chip Identification Number (cont'd)

Derivative	Value	Marking
XMC1403-Q064X0200	00014093 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00033000 10204083 _H	AA
XMC1404-Q048X0064	00014083 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00011000 10204083 _H	AA
XMC1404-Q048X0128	00014083 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00021000 10204083 _H	AA
XMC1404-Q048X0200	00014083 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00033000 10204083 _H	AA
XMC1404-Q064X0064	00014093 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00011000 10204083 _H	AA
XMC1404-Q064X0128	00014093 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00021000 10204083 _H	AA
XMC1404-Q064X0200	00014093 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00033000 10204083 _H	AA
XMC1404-F064X0064	000140A3 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00011000 10204083 _H	AA
XMC1404-F064X0128	000140A3 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00021000 10204083 _H	AA
XMC1404-F064X0200	000140A3 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00033000 10204083 _H	AA

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

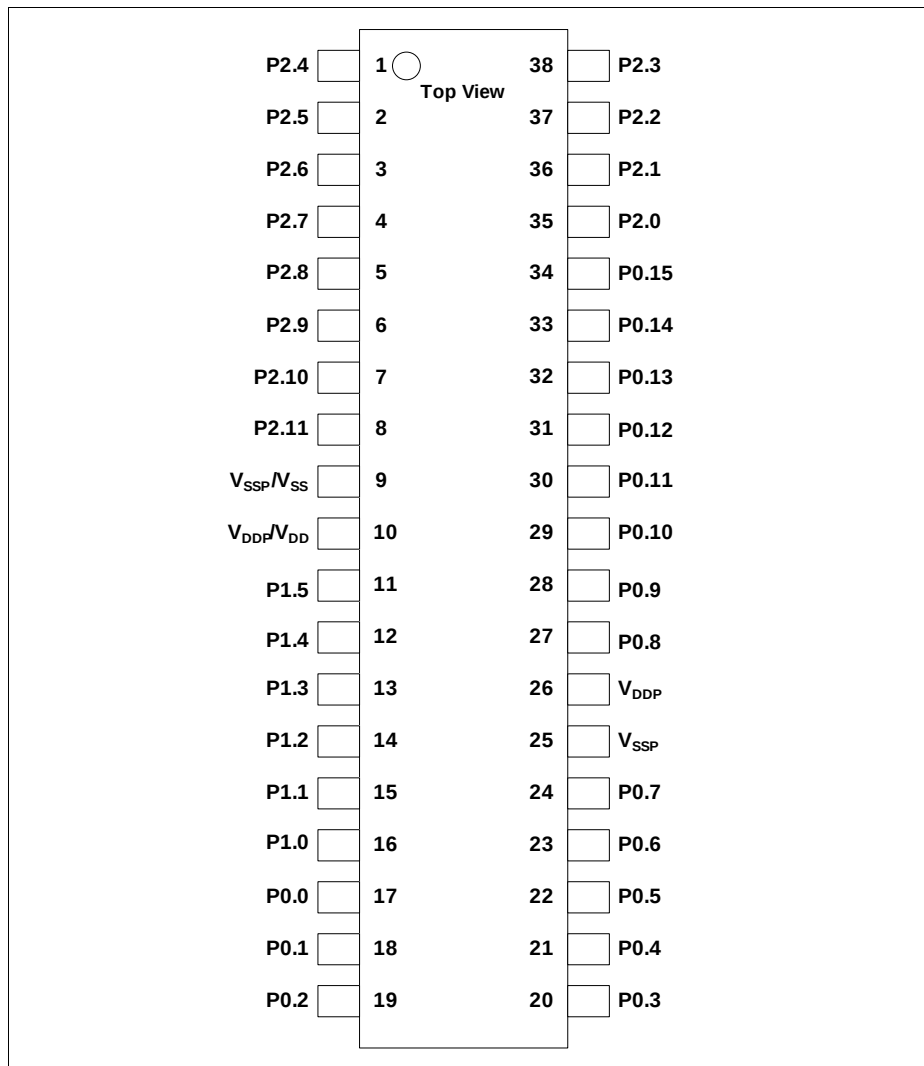


Figure 6 XMC1400 PG-TSSOP-38-9 Pin Configuration (top view)

General Device Information
Table 5 Package Pin Mapping (cont'd)

Function	LQFP 64, VQFN 64	VQFN 48	VQFN 40	TSSOP 38	Pad Type	Notes
P2.8	17	11	9	5	STD_IN/AN	
P2.9	18	12	10	6	STD_IN/AN	
P2.10	19	13	11	7	STD_INOUT /AN	
P2.11	20	14	12	8	STD_INOUT /AN	
P2.12	21	15	-	-	STD_INOUT /AN	
P2.13	22	16	-	-	STD_INOUT /AN	
P3.0	36	28	-	-	STD_INOUT	
P3.1	37	-	-	-	STD_INOUT	
P3.2	38	-	-	-	STD_INOUT	
P3.3	39	-	-	-	STD_INOUT	
P3.4	40	-	-	-	STD_INOUT	
P4.0	59	-	-	-	STD_INOUT	
P4.1	60	-	-	-	STD_INOUT	
P4.2	61	-	-	-	STD_INOUT	
P4.3	62	-	-	-	STD_INOUT	
P4.4	63	47	-	-	STD_INOUT	
P4.5	64	48	-	-	STD_INOUT	
P4.6	3	1	-	-	STD_INOUT	
P4.7	4	2	-	-	STD_INOUT	
P4.8	5	-	-	-	STD_INOUT	
P4.9	6	-	-	-	STD_INOUT	
P4.10	7	-	-	-	STD_INOUT	
P4.11	8	-	-	-	STD_INOUT	
VSS	23	17	13	9	Power	Supply GND, ADC reference GND

Port I/O Function Table

Table 9 Port I/O Functions

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0.P DOUT0	LEDTS0 .LINE7	ERU0.G OUT0	CCU40. OUT0	CCU80. OUT00	USIC0_ CH0.SE LO0	USIC0_ CH1.SE LO0	CCU81. OUT00	USIC1_ CH1.DO UT0	BCCU0. TRAPIN B	CCU40.I N0AC					USIC1_ CH1.DX 0A	USIC0_ CH0.D X2A		USIC0_ CH1.DX 2A		
P0.1	ERU0.P DOUT1	LEDTS0 .LINE6	ERU0.G OUT1	CCU40. OUT1	CCU80. OUT01	BCCU0. OUT8	SCU.VD ROP	USIC1_ CH1.SC LKOUT	USIC1_ CH1.DO UT0		CCU40.I N1AC					USIC1_ CH1.DX 0B	USIC1_ CH1.D X1A				
P0.2	ERU0.P DOUT2	LEDTS0 .LINE5	ERU0.G OUT2	CCU40. OUT2	CCU80. OUT02	VADC0. EMUX02	CCU80. OUT10	USIC1_ CH0.SC LKOUT	USIC1_ CH0.DO UT0		CCU40.I N2AC					USIC1_ CH0.DX 0A	USIC1_ CH0.D X1A				
P0.3	ERU0.P DOUT3	LEDTS0 .LINE4	ERU0.G OUT3	CCU40. OUT3	CCU80. OUT03	VADC0. EMUX01	CCU80. OUT11	USIC1_ CH1.SC LKOUT	USIC1_ CH0.DO UT0		CCU40.I N3AC					USIC1_ CH0.DX 0B					
P0.4	BCCU0. OUT0	LEDTS0 .LINE3	LEDTS0 .COL3	CCU40. OUT1	CCU80. OUT13	VADC0. EMUX00	WWDT. SERVIC E_OUT	USIC1_ CH1.SE LO0	CAN.N0 _TXD			CCU41.I N0AB	CCU80.I N0AB							CAN.N0 _RXDA	
P0.5	BCCU0. OUT1	LEDTS0 .LINE2	LEDTS0 .COL2	CCU40. OUT0	CCU80. OUT12	ACMP2. OUT	CCU80. OUT01	VADC0. EMUX10	CAN.N0 _TXD			CCU41.I N1AB	CCU80.I N1AB							CAN.N0 _RXDB	
P0.6	BCCU0. OUT2	LEDTS0 .LINE1	LEDTS0 .COL1	CCU40. OUT0	CCU80. OUT11	USIC0_ CH1.MC LKOUT	USIC0_ CH1.DO UT0	VADC0. EMUX11	CCU41. OUT0		CCU40.I N0AB	CCU41.I N2AB						USIC0_ CH1.DX 0C			
P0.7	BCCU0. OUT3	LEDTS0 .LINE0	LEDTS0 .COL0	CCU40. OUT1	CCU80. OUT10	USIC0_ CH0.SC LKOUT	USIC0_ CH1.DO UT0	VADC0. EMUX12	CCU41. OUT1		CCU40.I N1AB	CCU41.I N3AB				USIC0_ CH0.D X1C	USIC0_ CH1.DX 0D	USIC0_ CH1.DX 1C			
P0.8/ RTC_XTAL1	BCCU0. OUT4	LEDTS1 .LINE0	LEDTS0 _OUT2	CCU40. OUT20	CCU80. OUT20	USIC0_ CH0.SC LKOUT	USIC0_ CH1.SC LKOUT	CCU81. OUT20	CCU41. OUT2		CCU40.I N2AB					USIC0_ CH0.D X1B		USIC0_ CH1.DX 1B			
P0.9/ RTC_XTAL2	BCCU0. OUT5	LEDTS1 .LINE1	LEDTS0 _OUT3	CCU40. OUT3	CCU80. OUT21	USIC0_ CH0.SE LO0	USIC0_ CH1.SE LO0	CCU81. OUT21	CCU41. OUT3		CCU40.I N3AB					USIC0_ CH0.D X2B		USIC0_ CH1.DX 2B			
P0.10/ XTAL1	BCCU0. OUT6	LEDTS1 .LINE2	LEDTS0 _COL5	ACMP0. OUT	CCU80. OUT22	USIC0_ CH0.SE LO1	USIC0_ CH1.SE LO1	CCU81. OUT22				CCU80.I N2AB	CCU81.I N2AB			USIC0_ CH0.D X2C		USIC0_ CH1.DX 2C			
P0.11/ XTAL2	BCCU0. OUT7	LEDTS1 .LINE3	LEDTS0 _COL4	USIC0_ CH0.MC LKOUT	CCU80. OUT23	USIC0_ CH0.SE LO2	USIC0_ CH1.SE LO2	CCU81. OUT23								USIC0_ CH0.D X2D		USIC0_ CH1.DX 2D			
P0.12	BCCU0. OUT6	LEDTS1 .LINE4	LEDTS0 _COL3	LEDTS1 _COL3	CCU80. OUT33	USIC0_ CH0.SE LO3	CCU80. OUT20		CAN.N1 _TXD	BCCU0. TRAPIN A	CCU40.I N0AA	CCU40.I N1AA	CCU40.I N2AA	CCU81.I N0AU	CCU40.I N3AA	CCU80.I N0AA	USIC0_ CH0.D X2E	CCU80.I N1AA	CCU80.I N2AA	CAN.N1 _RXDA	CCU80.I N3AA

Table 9 Port I/O Functions (cont'd)

Function	Outputs									Inputs										
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P3.2	BCCU0. OUT2	USIC1_ CH1.SC LKOUT		LEDTS2 .COL1	CCU80. OUT11	ACMP2. OUT	USIC1_ CH0.SC LKOUT	CCU81. OUT11	CCU41. OUT2						USIC1_ CH0.DX 3C	USIC1_ CH0.D X4C	USIC1_ CH1.DX 3D	USIC1_ CH1.DX 4D		ERU1.2 A1
P3.3	BCCU0. OUT5	USIC1_ CH0.DO UT0		LEDTS2 .COL2	CCU80. OUT10	ACMP0. OUT	USIC1_ CH1.SE LO0	CCU81. OUT10	CCU41. OUT3						USIC1_ CH0.DX 0E			USIC1_ CH1.DX 2A		ERU1.1 A3
P3.4	BCCU0. OUT6	USIC1_ CH0.DO UT0	USIC1_ CH0.SC LKOUT	LEDTS2 .COL3	CCU80. OUT01	USIC1_ CH1.MC LKOUT	USIC1_ CH1.SE LO1	CCU81. OUT01							USIC1_ CH0.DX 0F	USIC1_ CH0.D X1E		USIC1_ CH1.DX 2B		ERU1.2 A3
P4.0	BCCU0. OUT0	ERU1.P DOUT0	LEDTS2 .COL5	ERU1.G OUT0	CCU40. OUT0	ACMP1. OUT	USIC1_ CH1.SE LO1	CCU81. OUT10	CCU41. OUT0		CCU40.I N0BA	CCU41.I N0AC	CCU80.I N0AU		USIC1_ CH0.DX 3D	USIC1_ CH0.D X4D				
P4.1	BCCU0. OUT8	ERU1.P DOUT1	LEDTS2 .COL4	ERU1.G OUT1	CCU40. OUT1	ACMP3. OUT	USIC1_ CH1.SE LO2	CCU81. OUT11	CCU41. OUT1		CCU40.I N1BA	CCU41.I N1AC	CCU80.I N1AU	POSIF1. IN0B	USIC1_ CH0.DX 5C					
P4.2	BCCU0. OUT4	ERU1.P DOUT2	CCU81. OUT20	ERU1.G OUT2	CCU40. OUT2	ACMP2. OUT	USIC1_ CH1.SE LO3	CCU81. OUT12	CCU41. OUT2		CCU40.I N2BA	CCU41.I N2AC	CCU80.I N2AU	CCU81.I N1AB	POSIF1. IN1B	USIC1_ CH0.DX 5D				
P4.3	BCCU0. OUT5	ERU1.P DOUT3	CCU81. OUT21	ERU1.G OUT3	CCU40. OUT3	ACMP0. OUT	USIC1_ CH0.SC LKOUT	CCU81. OUT13	CCU41. OUT3		CCU40.I N3BA	CCU41.I N3AC	CCU80.I N3AU	POSIF1. IN2B		USIC1_ CH0.D X1B				
P4.4	BCCU0. OUT0	LEDTS2 .LINE0		LEDTS1 .COLA	CCU80. OUT00	USIC1_ CH0.DO UT0		CCU81. OUT00	CCU41. OUT0			CCU41.I N0AV			USIC1_ CH0.DX 0C		USIC1_ CH1.DX 5F			ERU1.0 A2
P4.5	BCCU0. OUT8	LEDTS2 .LINE1		LEDTS1 .COL6	CCU80. OUT01	USIC1_ CH0.DO UT0	USIC1_ CH0.SC LKOUT	CCU81. OUT01	CCU41. OUT1			CCU41.I N1AV			USIC1_ CH0.DX 0D	USIC1_ CH0.D X1C				ERU1.1 A2
P4.6	BCCU0. OUT2	LEDTS2 .LINE2	CCU81. OUT10	LEDTS1 .COL5	CCU80. OUT10		USIC1_ CH0.SC LKOUT	CCU81. OUT02	CCU41. OUT2			CCU41.I N2AV		CCU81.I N0AB		USIC1_ CH0.D X1D				ERU1.2 A2
P4.7	BCCU0. OUT5	LEDTS2 .LINE3	CCU81. OUT11	LEDTS1 .COL4	CCU80. OUT11		USIC1_ CH0.SE LO0	CCU81. OUT03	CCU41. OUT3			CCU41.I N3AV				USIC1_ CH0.D X2A				ERU1.0 A3
P4.8	BCCU0. OUT7	LEDTS2 .LINE4	LEDTS2 .COL3	LEDTS1 .COL3	CCU80. OUT30	CCU40. OUT0	USIC1_ CH0.SE LO1	CCU81. OUT30	CAN.N1 _TXD		CCU40.I N0AV	CCU41.I N0BA				USIC1_ CH0.D X2B			CAN.N1 _RXDC	
P4.9	BCCU0. OUT3	LEDTS2 .LINE5	LEDTS2 .COL2	LEDTS1 .COL2	CCU80. OUT31	CCU40. OUT1	USIC1_ CH0.SE LO2	CCU81. OUT31	CAN.N1 _TXD		CCU40.I N1AV	CCU41.I N1BA				USIC1_ CH0.D X2C			CAN.N1 _RXDD	

Table 10 Hardware I/O Controlled Functions

Function	Outputs	Outputs	Inputs	Inputs	Pull Control	Pull Control	Pull Control	Pull Control
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P0.0	LEDTS0. EXTENDED7		LEDTS0.TSIN7	LEDTS0.TSIN7	Reserved for LEDTS Scheme A: pull-down disabled always	Reserved for LEDTS Scheme A: pull-down enabled always	Reserved for LEDTS Scheme B: pull-up enabled and pull-down disabled, and vice versa	
P0.1	LEDTS0. EXTENDED6		LEDTS0.TSIN6	LEDTS0.TSIN6				
P0.2	LEDTS0. EXTENDED5		LEDTS0.TSIN5	LEDTS0.TSIN5				
P0.3	LEDTS0. EXTENDED4		LEDTS0.TSIN4	LEDTS0.TSIN4				
P0.4	LEDTS0. EXTENDED3		LEDTS0.TSIN3	LEDTS0.TSIN3				
P0.5	LEDTS0. EXTENDED2		LEDTS0.TSIN2	LEDTS0.TSIN2				
P0.6	LEDTS0. EXTENDED1		LEDTS0.TSIN1	LEDTS0.TSIN1				
P0.7	LEDTS0. EXTENDED0		LEDTS0.TSIN0	LEDTS0.TSIN0				
P0.8	LEDTS1. EXTENDED0		LEDTS1.TSIN0	LEDTS1.TSIN0				
P0.9	LEDTS1. EXTENDED1		LEDTS1.TSIN1	LEDTS1.TSIN1				
P0.10	LEDTS1. EXTENDED2		LEDTS1.TSIN2	LEDTS1.TSIN2				
P0.11	LEDTS1. EXTENDED3		LEDTS1.TSIN3	LEDTS1.TSIN3				
P0.12	LEDTS1. EXTENDED4		LEDTS1.TSIN4	LEDTS1.TSIN4				
P0.13	LEDTS1. EXTENDED5		LEDTS1.TSIN5	LEDTS1.TSIN5				
P0.14	LEDTS1. EXTENDED6		LEDTS1.TSIN6	LEDTS1.TSIN6				
P0.15	LEDTS1. EXTENDED7		LEDTS1.TSIN7	LEDTS1.TSIN7				
P1.0		USIC0_CH0.DOUT0		USIC0_CH0.HWIN0	BCCU0.OUT2	BCCU0.OUT2		
P1.1		USIC0_CH0.DOUT1		USIC0_CH0.HWIN1	BCCU0.OUT3	BCCU0.OUT3		
P1.2		USIC0_CH0.DOUT2		USIC0_CH0.HWIN2	BCCU0.OUT4	BCCU0.OUT4		

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 12 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
 - pad supply levels (V_{DDP})
 - temperature

If a pin current is outside of the **Operating Conditions** but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 12 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	
Absolute sum of all input circuit currents during overload condition	I_{OVS} SR	–	–	25	mA	

Figure 11 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

Table 17 ADC Characteristics (Operating Conditions apply)¹⁾ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain settings	$G_{IN\ CC}$	1			–	GNCTRxz.GAINy = 00 _B (unity gain)
		3			–	GNCTRxz.GAINy = 01 _B (gain g1)
		6			–	GNCTRxz.GAINy = 10 _B (gain g2)
		12			–	GNCTRxz.GAINy = 11 _B (gain g3)
Sample Time	$t_{sample\ CC}$	5	–	–	1 / f_{ADC}	$V_{DD} = 5.0\ V$, $f_{ADCI} = 48\ MHz$
		3	–	–	1 / f_{ADC}	$V_{DD} = 5.0\ V$, $f_{ADCI} = 32\ MHz$
		3	–	–	1 / f_{ADC}	$V_{DD} = 3.3\ V$, $f_{ADCI} = 32\ MHz$
		30	–	–	1 / f_{ADC}	$V_{DD} = 2.0\ V$, $f_{ADCI} = 32\ MHz$
Conversion time in fast compare mode	$t_{CF\ CC}$	9			1 / f_{ADC}	³⁾
Conversion time in 12-bit mode	$t_{C12\ CC}$	20			1 / f_{ADC}	³⁾
Maximum sample rate in 12-bit mode ⁴⁾	$f_{C12\ CC}$	–	–	$f_{ADC} / 42.5$	–	1 sample pending
		–	–	$f_{ADC} / 62.5$	–	2 samples pending
Conversion time in 10-bit mode	$t_{C10\ CC}$	18			1 / f_{ADC}	³⁾
Maximum sample rate in 10-bit mode ⁴⁾	$f_{C10\ CC}$	–	–	$f_{ADC} / 40.5$	–	1 sample pending
		–	–	$f_{ADC} / 58.5$	–	2 samples pending
Conversion time in 8-bit mode	$t_{C8\ CC}$	16			1 / f_{ADC}	³⁾

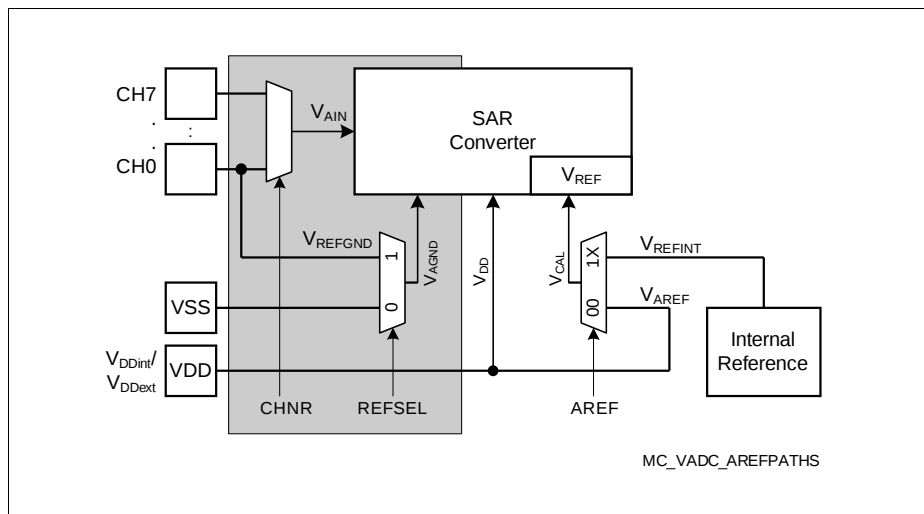


Figure 12 ADC Voltage Supply

3.2.3 Out of Range Comparator (ORC) Characteristics

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above V_{DDP} on selected input pins (ORCx.AIN) and generates a service request trigger (ORCx.OUT).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 18 Out of Range Comparator (ORC) Characteristics (Operating Conditions apply; $V_{DDP} = 3.0\text{ V} - 5.5\text{ V}$; $C_L = 0.25\text{ pF}$)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC}	CC	–	–	180	mV	$V_{AIN} \geq V_{DDP} + V_{ODC}$
Hysteresis	V_{OHYS}	CC	15	–	54	mV	
Always detected Overvoltage Pulse	t_{OPDD}	CC	103	–	–	ns	$V_{AIN} \geq V_{DDP} + 150\text{ mV}$
			88	–	–	ns	$V_{AIN} \geq V_{DDP} + 350\text{ mV}$
Never detected Overvoltage Pulse	t_{OPDN}	CC	–	–	21	ns	$V_{AIN} \geq V_{DDP} + 150\text{ mV}$
			–	–	11	ns	$V_{AIN} \geq V_{DDP} + 350\text{ mV}$
Detection Delay	t_{ODD}	CC	39	–	132	ns	$V_{AIN} \geq V_{DDP} + 150\text{ mV}$
			31	–	121	ns	$V_{AIN} \geq V_{DDP} + 350\text{ mV}$
Release Delay	t_{ORD}	CC	44	–	240	ns	$V_{AIN} \leq V_{DDP}$; $V_{DDP} = 5\text{ V}$
			57	–	340	ns	$V_{AIN} \leq V_{DDP}$; $V_{DDP} = 3.3\text{ V}$
Enable Delay	t_{OED}	CC	–	–	300	ns	ORCCTRL.ENORCx = 1

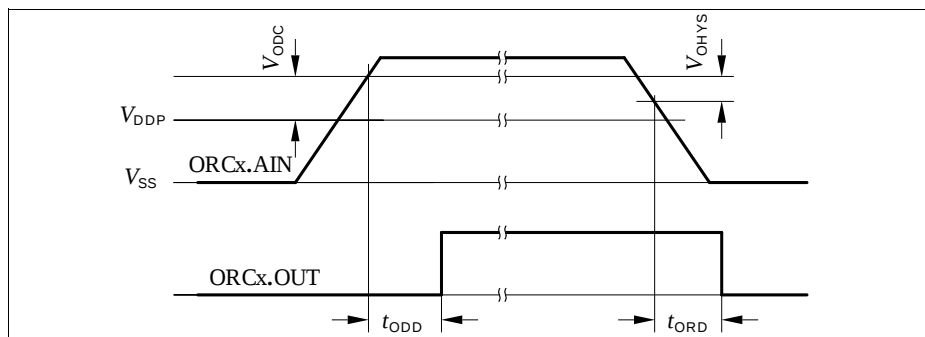


Figure 13 ORCx.OUT Trigger Generation

3.2.5 Temperature Sensor Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 20 Temperature Sensor Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	10	ms	
Temperature sensor range	T_{SR} SR	-40	–	115	°C	
Sensor Accuracy ¹⁾	T_{TSAL} CC	-6	–	6	°C	$T_J > 20^\circ\text{C}$
		-10	–	10	°C	$0^\circ\text{C} \leq T_J \leq 20^\circ\text{C}$
		–	-/+8	–	°C	$T_J < 0^\circ\text{C}$
Start-up time	t_{TSS} SR	–	–	15	μs	

1) The temperature sensor accuracy is independent of the supply voltage.

Table 24 provides the active current consumption of some modules operating at 5 V power supply at 25 °C. The typical values shown are used as a reference guide on the current consumption when these modules are enabled.

Table 24 Typical Active Current parameter table

Active Current Consumption	Symbol	Limit Values	Unit	Test Condition
		Typ.		
Baseload current	I_{CPUDDC}	4.14	mA	Modules including Core, SCU, PORT, memories, ANATOP ¹⁾
VADC and SHS	I_{ADCDDC}	3.73	mA	Set CGATCLR0.VADC to 1 ²⁾
USICx	$I_{USIC0DDC}$	1.35	mA	Set CGATCLR0.USIC0 to 1 ³⁾
CCU4x	$I_{CCU40DDC}$	0.99	mA	Set CGATCLR0.CCU40 to 1 ⁴⁾
CCU8x	$I_{CCU80DDC}$	1.00	mA	Set CGATCLR0.CCU80 to 1 ⁵⁾
POSIFx	$I_{PIF0DDC}$	1.05	mA	Set CGATCLR0.POSIF0 to 1 ⁶⁾
LEDTSx	$I_{LTSxDCC}$	1.14	mA	Set CGATCLR0.LEDTSx to 1 ⁷⁾
BCCU0	$I_{BCCU0DDC}$	0.29	mA	Set CGATCLR0.BCCU0 to 1 ⁸⁾
MATH	$I_{MATHDDC}$	0.50	mA	Set CGATCLR0.MATH to 1 ⁹⁾
WDT	I_{WDTDDC}	0.03	mA	Set CGATCLR0.WDT to 1 ¹⁰⁾
RTC	I_{RTCDCC}	0.01	mA	Set CGATCLR0.RTC to 1 ¹¹⁾
MultiCAN	$I_{MCANDCC}$	1.38	mA	Set CGATCLR0.MCAN0 to 1 ¹²⁾

1) Baseload current is measured with device running in user mode, MCLK=PCLK=48 MHz, with an endless loop in the flash memory. The clock to the modules stated in CGATSTAT0 are gated.

2) Active current is measured with: module enabled, MCLK=48 MHz, running in auto-scan conversion mode

3) Active current is measured with: module enabled, each of the 2 USIC channels sending alternate messages at 57.6 kbaud every 200 ms

4) Active current is measured with: module enabled, MCLK=PCLK=48 MHz, 1 CCU4 slice for PWM switching at 20kHz with duty cycle varying at 10%-90%, 1 CCU4 slice in capture mode for reading period and duty cycle

5) Active current is measured with: module enabled, MCLK=PCLK=48 MHz, 3 CCU8 slices with PWM frequency at 20kHz and a period match interrupt used to toggle duty cycle between 10% and 90%

6) Active current is measured with: module enabled, MCLK=48 MHz, PCLK=96 MHz, hall sensor mode

7) Active current is measured with: module enabled, MCLK=48 MHz, 1 LED column, 6 LED/TS lines, Pad Scheme A with large pad hysteresis config, time slice duration = 1.048 ms

8) Active current is measured with: module enabled, MCLK=48 MHz, PCLK=96MHz, FCLK=0.8 MHz, Normal mode (BCCU clock = FCLK/4), 4 BCCU Channels with packers enabled and 1 Dimming Engine, change color or dim every 1s

9) Active current is measured with: module enabled, MCLK=48 MHz, PCLK=96 MHz, tangent calculation in while loop; CORDIC circular rotation, no keep, autostart; 32-by-32 bit signed DIV, autostart, DVS right shift by 11

3.2.8 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase time per page / sector	$t_{\text{ERASE CC}}$	6.8	7.1	7.6	ms	
Program time per block	$t_{\text{PSER CC}}$	102	152	204	μs	
Wake-Up time	$t_{\text{WU CC}}$	–	32.2	–	μs	
Read time per word	$t_{\text{a CC}}$	–	50	–	ns	
Data Retention Time	$t_{\text{RET CC}}$	10	–	–	years	Max. 100 erase / program cycles
Flash Wait States ¹⁾	$N_{\text{WSFLASH CC}}$	0	0	0		$f_{\text{MCLK}} = 8 \text{ MHz}$
		0	1	1		$f_{\text{MCLK}} = 16 \text{ MHz}$
		1	2	2		$f_{\text{MCLK}} = 32 \text{ MHz}$
		2	2	3		$f_{\text{MCLK}} = 48 \text{ MHz}$
Erase Cycles	$N_{\text{ECYC CC}}$	–	–	$5 \cdot 10^4$	cycles	Sum of page and sector erase cycles
Total Erase Cycles	$N_{\text{TECYC CC}}$	–	–	$2 \cdot 10^6$	cycles	

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

3.3.5 SPD Timing Requirements

The optimum SPD decision time between 0_B and 1_B is $0.75 \mu s$. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles ($0.69 \mu s$).

Table 30 Optimum Number of Sample Clocks for SPD

Sample Freq.	Sampling Factor	Sample Clocks 0_B	Sample Clocks 1_B	Effective Decision Time ¹⁾	Remark
8 MHz	4	1 to 5	6 to 12	$0.69 \mu s$	The other closest option ($0.81 \mu s$) for the effective decision time is less robust.

1) Nominal sample frequency period multiplied with $0.5 + (\text{max. number of } 0_B \text{ sample clocks})$

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is $\pm 5\%$
- Effective decision time is between $0.69 \mu s$ and $0.75 \mu s$ (calculated with nominal sample frequency)

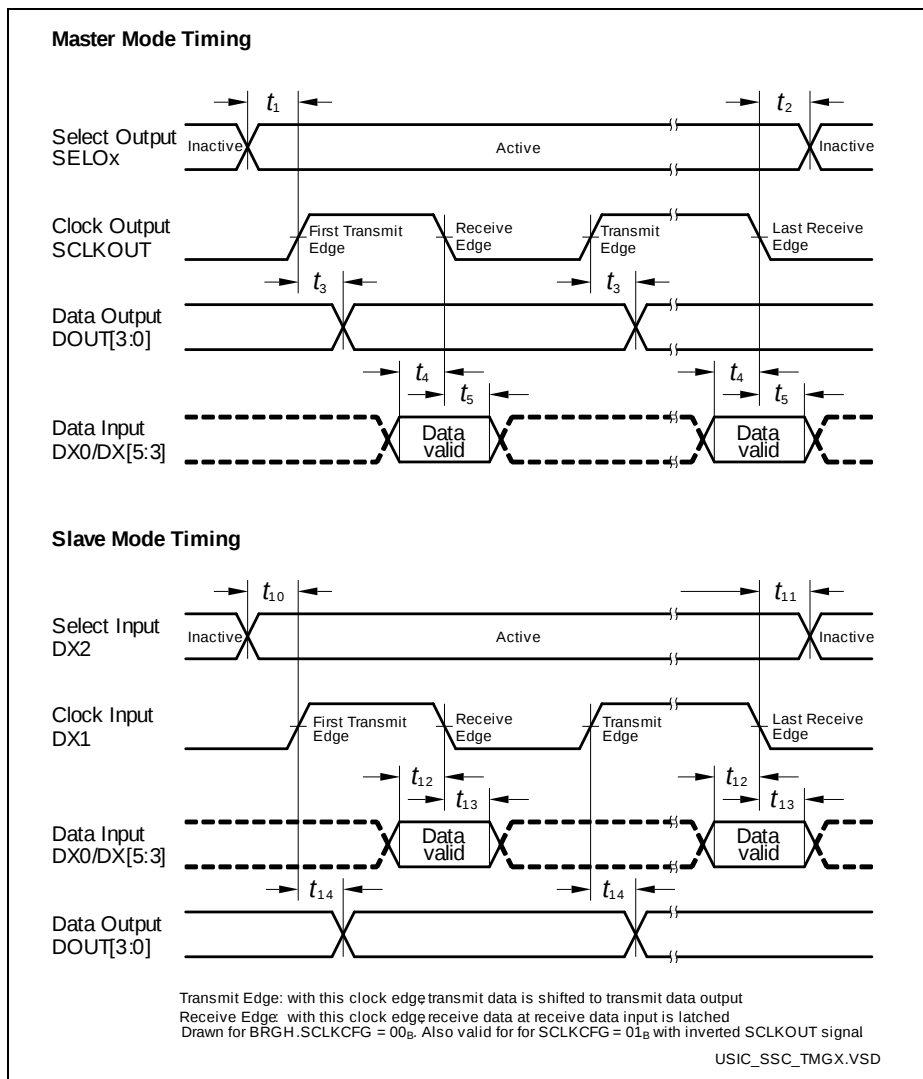


Figure 25 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.