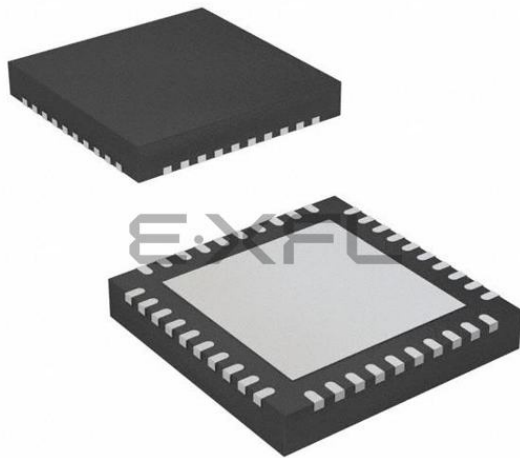




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I ² S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-40-17
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1402q040x0064aaxuma1

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Features

CPU subsystem

- 32-bit ARM Cortex-M0 CPU Core
 - 0.84 DMIPS/MHz (Dhrystone 2.1) at 48 MHz
- Nested Vectored Interrupt Controller
- 64 interrupt nodes
- MATH coprocessor
 - 24-bit trigonometric calculation (CORDIC)
 - 32-bit divide operation
- 2x4 channels ERU for event interconnections

On-Chip Memories

- 8 Kbyte ROM
- 16 Kbyte SRAM (with parity)
- up to 200 Kbyte Flash (with ECC)

Supply, Reset and Clock

- 1.8 V to 5.5 V supply with power on reset and brownout detector
- On-chip clock monitor
- External crystal oscillator support (32 kHz and 4 to 20 MHz)
- Internal slow and fast oscillators without the need of PLL

System Control

- Window watchdog
- Real time clock module
- Pseudo random number generator

Communication Peripherals

- Four USIC channels, usable as
 - UART (up to 12 Mb/s)
 - single-SPI (up to 12 Mb/s)
 - double-SPI (up to 2 × 12 Mb/s)
 - quad-SPI (up to 4 × 12 Mb/s)
 - IIC (up to 400 kb/s)
 - IIS (up to 12 Mb/s)
 - LIN interfaces (20kb/s)
- LEDTS in Human-Machine interface
 - up to 24 touch pads
 - drive up to 144 LEDs
- MultiCAN+, Full-CAN/Basic-CAN with 2 nodes, 32 message objects (up to 1 Mbaud)

Analog Frontend Peripherals

- A/D Converters (up to 12 analog inputs)
 - 2 sample and hold stages
 - fast 12-bit ADC (up to 1.1 MS/s), adjustable gain
 - 0 V to 5.5 V input range
- Up to 8 channels out of range comparators
- Up to 4 fast analog comparators
- Temperature Sensor

Industrial Control Peripherals

- 2x4 16-bit 96 MHz CCU4 timers for signal monitoring and PWM
- 2x4 16-bit 96 MHz CCU8 timers for complex PWM, complementary high/low side switches and multi phase control
- 2x POSIF for hall and quadrature encoders, motor positioning
- 9 channel BCCU (brightness and color control) for LED lighting applications

Up to 56 Input/Output Ports

- 1.8 V to 5.5 V capable
- up to 8 high current pads (50 mA sink)

On-Chip Debug Support

- 4 breakpoints, 2 watchpoints
- ARM serial wire debug, single-pin debug interfaces

Programming Support

- Single-pin bootloader
- Secure bootstrap loader SBSL (optional)

Packages

- TSSOP-38 (9.7 × 6.4 mm²)
- VQFN-40/48/64 (5×5/7×7/8×8 mm²)
- LQFP-64 (12 × 12 mm²)

Tools

- Free DAVE™ toolchain with low level drivers and apps

Table 3 XMC1400 Chip Identification Number (cont'd)

Derivative	Value	Marking
XMC1403-Q064X0200	00014093 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00033000 10204083 _H	AA
XMC1404-Q048X0064	00014083 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00011000 10204083 _H	AA
XMC1404-Q048X0128	00014083 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00021000 10204083 _H	AA
XMC1404-Q048X0200	00014083 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00033000 10204083 _H	AA
XMC1404-Q064X0064	00014093 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00011000 10204083 _H	AA
XMC1404-Q064X0128	00014093 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00021000 10204083 _H	AA
XMC1404-Q064X0200	00014093 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00033000 10204083 _H	AA
XMC1404-F064X0064	000140A3 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00011000 10204083 _H	AA
XMC1404-F064X0128	000140A3 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00021000 10204083 _H	AA
XMC1404-F064X0200	000140A3 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00033000 10204083 _H	AA

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

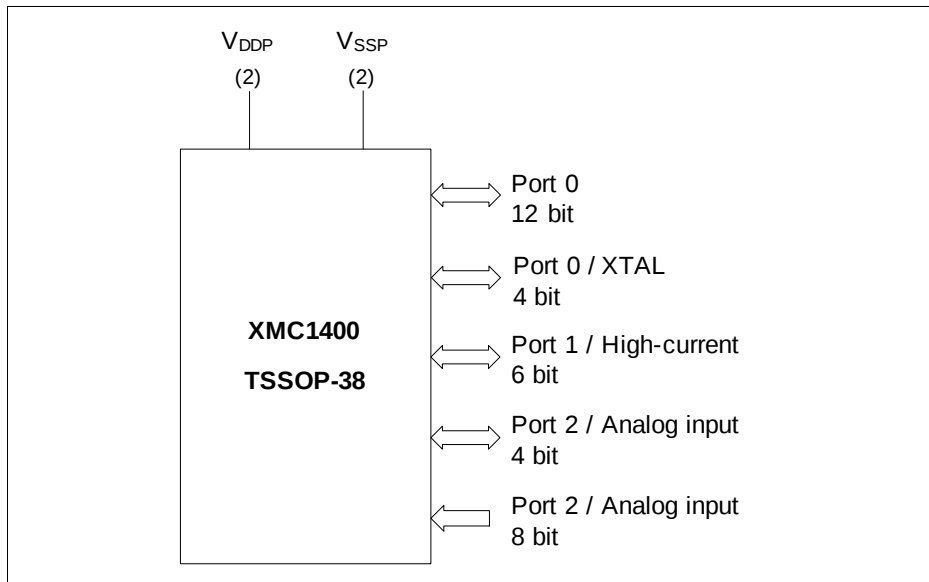


Figure 2 XMC1400 Logic Symbol for TSSOP-38-9

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

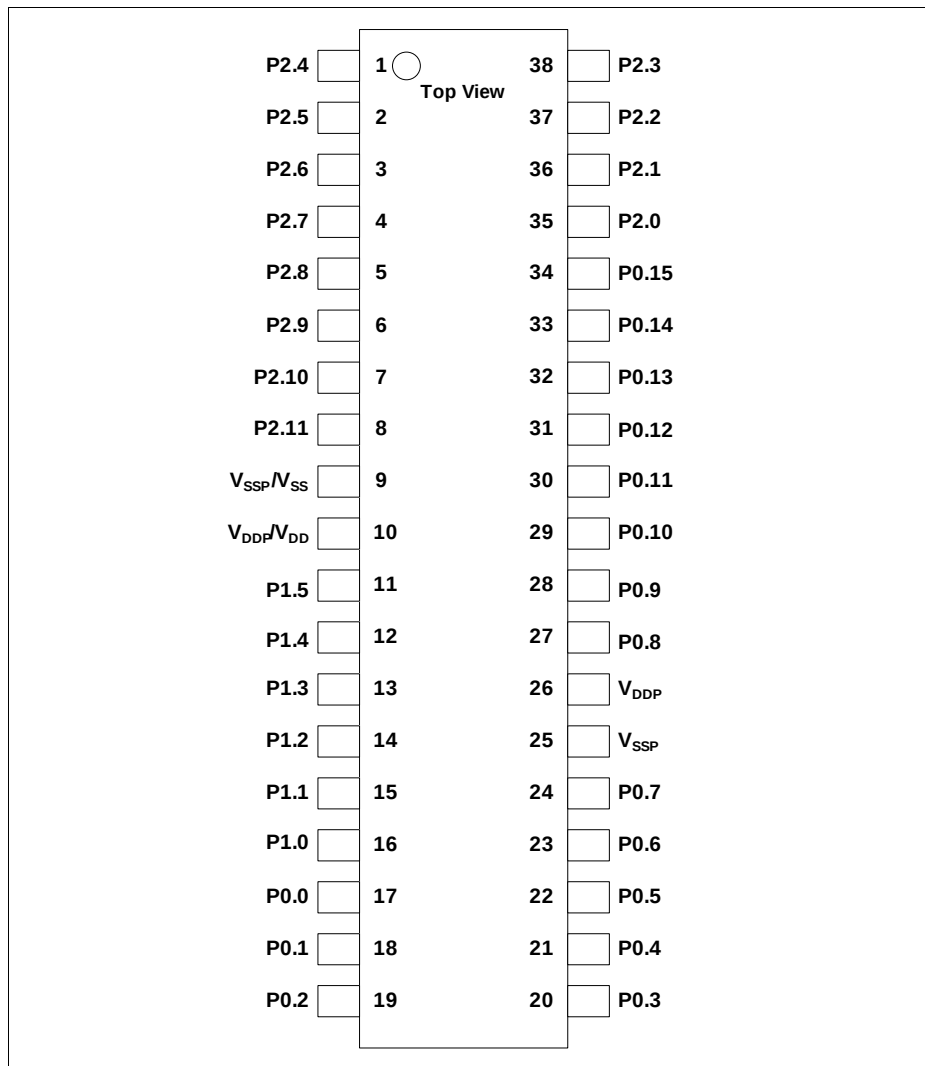


Figure 6 XMC1400 PG-TSSOP-38-9 Pin Configuration (top view)

2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

Table 4 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type
Px.y	N	N		Pad Class

The table is sorted by the "Function" column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The "Pad Type" indicates the employed pad type:

- STD_INOUT (standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- STD_INOUT/clock (standard bi-directional pads with oscillator function)
- High Current (high current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameter chapter.

Table 5 Package Pin Mapping

Function	LQFP 64, VQFN 64	VQFN 48	VQFN 40	TSSOP 38	Pad Type	Notes
P0.0	41	29	23	17	STD_INOUT	
P0.1	42	30	24	18	STD_INOUT	
P0.2	43	31	25	19	STD_INOUT	
P0.3	44	32	26	20	STD_INOUT	
P0.4	45	33	27	21	STD_INOUT	
P0.5	46	34	28	22	STD_INOUT	
P0.6	47	35	29	23	STD_INOUT	
P0.7	48	36	30	24	STD_INOUT	
P0.8/ RTC_ XTAL1	51	39	33	27	STD_INOUT /clock_IN	

2.2.3 Port I/O Function Description

The following general building block is used to describe the I/O functions of each PORT pin:

Table 7 Port I/O Function Description

Function	Outputs		Inputs	
	ALT1	ALTn	Input	Input
P0.0		MODA.OUT	MODC.INA	
Pn.y	MODA.OUT		MODA.INA	MODC.INB

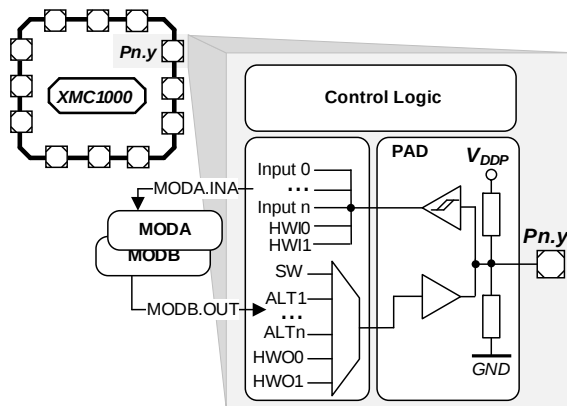


Figure 10 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to nine alternate output functions (ALT1 to ALT9) can be mapped to a single port pin, selected by Pn_IOC.R.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

Please refer to the [Port I/O Functions](#) table for the complete Port I/O function mapping.

Port I/O Function Table

Table 9 Port I/O Functions

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0.P DOUT0	LEDTS0 .LINE7	ERU0.G OUT0	CCU40. OUT0	CCU80. OUT00	USIC0_ CH0.SE LO0	USIC0_ CH1.SE LO0	CCU81. OUT00	USIC1_ CH1.DO UT0	BCCU0. TRAPIN B	CCU40.I N0AC					USIC1_ CH1.DX 0A	USIC0_ CH0.D X2A		USIC0_ CH1.DX 2A		
P0.1	ERU0.P DOUT1	LEDTS0 .LINE6	ERU0.G OUT1	CCU40. OUT1	CCU80. OUT01	BCCU0. OUT8	SCU.VD ROP	USIC1_ CH1.SC LKOUT	USIC1_ CH1.DO UT0		CCU40.I N1AC					USIC1_ CH1.DX 0B	USIC1_ CH1.D X1A				
P0.2	ERU0.P DOUT2	LEDTS0 .LINE5	ERU0.G OUT2	CCU40. OUT2	CCU80. OUT02	VADC0. EMUX02	CCU80. OUT10	USIC1_ CH0.SC LKOUT	USIC1_ CH0.DO UT0		CCU40.I N2AC					USIC1_ CH0.DX 0A	USIC1_ CH0.D X1A				
P0.3	ERU0.P DOUT3	LEDTS0 .LINE4	ERU0.G OUT3	CCU40. OUT3	CCU80. OUT03	VADC0. EMUX01	CCU80. OUT11	USIC1_ CH1.SC LKOUT	USIC1_ CH0.DO UT0		CCU40.I N3AC					USIC1_ CH0.DX 0B					
P0.4	BCCU0. OUT0	LEDTS0 .LINE3	LEDTS0 .COL3	CCU40. OUT1	CCU80. OUT13	VADC0. EMUX00	WWDT. SERVIC E_OUT	USIC1_ CH1.SE LO0	CAN.N0 _TXD			CCU41.I N0AB	CCU80.I N0AB							CAN.N0 _RXDA	
P0.5	BCCU0. OUT1	LEDTS0 .LINE2	LEDTS0 .COL2	CCU40. OUT0	CCU80. OUT12	ACMP2. OUT	CCU80. OUT01	VADC0. EMUX10	CAN.N0 _TXD			CCU41.I N1AB	CCU80.I N1AB							CAN.N0 _RXDB	
P0.6	BCCU0. OUT2	LEDTS0 .LINE1	LEDTS0 .COL1	CCU40. OUT0	CCU80. OUT11	USIC0_ CH1.MC LKOUT	USIC0_ CH1.DO UT0	VADC0. EMUX11	CCU41. OUT0		CCU40.I N0AB	CCU41.I N2AB						USIC0_ CH1.DX 0C			
P0.7	BCCU0. OUT3	LEDTS0 .LINE0	LEDTS0 .COL0	CCU40. OUT1	CCU80. OUT10	USIC0_ CH0.SC LKOUT	USIC0_ CH1.DO UT0	VADC0. EMUX12	CCU41. OUT1		CCU40.I N1AB	CCU41.I N3AB				USIC0_ CH0.D X1C	USIC0_ CH1.DX 0D	USIC0_ CH1.DX 1C			
P0.8/ RTC_XTAL1	BCCU0. OUT4	LEDTS1 .LINE0	LEDTS0 _COLA	CCU40. OUT20	CCU80. OUT20	USIC0_ CH0.SC LKOUT	USIC0_ CH1.SC LKOUT	CCU81. OUT20	CCU41. OUT2		CCU40.I N2AB					USIC0_ CH0.D X1B		USIC0_ CH1.DX 1B			
P0.9/ RTC_XTAL2	BCCU0. OUT5	LEDTS1 .LINE1	LEDTS0 _COL6	CCU40. OUT3	CCU80. OUT21	USIC0_ CH0.SE LO0	USIC0_ CH1.SE LO0	CCU81. OUT21	CCU41. OUT3		CCU40.I N3AB					USIC0_ CH0.D X2B		USIC0_ CH1.DX 2B			
P0.10/ XTAL1	BCCU0. OUT6	LEDTS1 .LINE2	LEDTS0 _COL5	ACMP0. OUT	CCU80. OUT22	USIC0_ CH0.SE LO1	USIC0_ CH1.SE LO1	CCU81. OUT22				CCU80.I N2AB	CCU81.I N2AB			USIC0_ CH0.D X2C		USIC0_ CH1.DX 2C			
P0.11/ XTAL2	BCCU0. OUT7	LEDTS1 .LINE3	LEDTS0 _COL4	USIC0_ CH0.MC LKOUT	CCU80. OUT23	USIC0_ CH0.SE LO2	USIC0_ CH1.SE LO2	CCU81. OUT23								USIC0_ CH0.D X2D		USIC0_ CH1.DX 2D			
P0.12	BCCU0. OUT6	LEDTS1 .LINE4	LEDTS0 _COL3	LEDTS1 _COL3	CCU80. OUT33	USIC0_ CH0.SE LO3	CCU80. OUT20		CAN.N1 _TXD	BCCU0. TRAPIN A	CCU40.I N0AA	CCU40.I N1AA	CCU40.I N2AA	CCU81.I N0AU	CCU40.I N3AA	CCU80.I N0AA	USIC0_ CH0.D X2E	CCU80.I N1AA	CCU80.I N2AA	CAN.N1 _RXDA	CCU80.I N3AA

Table 10 Hardware I/O Controlled Functions

Function	Outputs	Outputs	Inputs	Inputs	Pull Control	Pull Control	Pull Control	Pull Control
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P0.0	LEDTS0. EXTENDED7		LEDTS0.TSIN7	LEDTS0.TSIN7	Reserved for LEDTS Scheme A: pull-down disabled always	Reserved for LEDTS Scheme A: pull-down enabled always	Reserved for LEDTS Scheme B: pull-up enabled and pull-down disabled, and vice versa	
P0.1	LEDTS0. EXTENDED6		LEDTS0.TSIN6	LEDTS0.TSIN6				
P0.2	LEDTS0. EXTENDED5		LEDTS0.TSIN5	LEDTS0.TSIN5				
P0.3	LEDTS0. EXTENDED4		LEDTS0.TSIN4	LEDTS0.TSIN4				
P0.4	LEDTS0. EXTENDED3		LEDTS0.TSIN3	LEDTS0.TSIN3				
P0.5	LEDTS0. EXTENDED2		LEDTS0.TSIN2	LEDTS0.TSIN2				
P0.6	LEDTS0. EXTENDED1		LEDTS0.TSIN1	LEDTS0.TSIN1				
P0.7	LEDTS0. EXTENDED0		LEDTS0.TSIN0	LEDTS0.TSIN0				
P0.8	LEDTS1. EXTENDED0		LEDTS1.TSIN0	LEDTS1.TSIN0				
P0.9	LEDTS1. EXTENDED1		LEDTS1.TSIN1	LEDTS1.TSIN1				
P0.10	LEDTS1. EXTENDED2		LEDTS1.TSIN2	LEDTS1.TSIN2				
P0.11	LEDTS1. EXTENDED3		LEDTS1.TSIN3	LEDTS1.TSIN3				
P0.12	LEDTS1. EXTENDED4		LEDTS1.TSIN4	LEDTS1.TSIN4				
P0.13	LEDTS1. EXTENDED5		LEDTS1.TSIN5	LEDTS1.TSIN5				
P0.14	LEDTS1. EXTENDED6		LEDTS1.TSIN6	LEDTS1.TSIN6				
P0.15	LEDTS1. EXTENDED7		LEDTS1.TSIN7	LEDTS1.TSIN7				
P1.0		USIC0_CH0.DOUT0		USIC0_CH0.HWIN0	BCCU0.OUT2	BCCU0.OUT2		
P1.1		USIC0_CH0.DOUT1		USIC0_CH0.HWIN1	BCCU0.OUT3	BCCU0.OUT3		
P1.2		USIC0_CH0.DOUT2		USIC0_CH0.HWIN2	BCCU0.OUT4	BCCU0.OUT4		

Table 10 Hardware I/O Controlled Functions

Function	Outputs	Outputs	Inputs	Inputs	Pull Control	Pull Control	Pull Control	Pull Control
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P4.4	LEDTS2. EXTENDED0		LEDTS2.TSIN0	LEDTS2.TSIN0	Reserved for LEDTS Scheme A: pull-down disabled always	Reserved for LEDTS Scheme A: pull-down enabled always	Reserved for LEDTS Scheme B: pull-up enabled and pull-down disabled, and vice versa	
P4.5	LEDTS2. EXTENDED1		LEDTS2.TSIN1	LEDTS2.TSIN1				
P4.6	LEDTS2. EXTENDED2		LEDTS2.TSIN2	LEDTS2.TSIN2				
P4.7	LEDTS2. EXTENDED3		LEDTS2.TSIN3	LEDTS2.TSIN3				
P4.8	LEDTS2. EXTENDED4		LEDTS2.TSIN4	LEDTS2.TSIN4				
P4.9	LEDTS2. EXTENDED5		LEDTS2.TSIN5	LEDTS2.TSIN5				
P4.10	LEDTS2. EXTENDED6		LEDTS2.TSIN6	LEDTS2.TSIN6				
P4.11	LEDTS2. EXTENDED7		LEDTS2.TSIN7	LEDTS2.TSIN7				

3.2 DC Parameters

3.2.1 Input/Output Characteristics

Table 16 provides the characteristics of the input/output pins of the XMC1400.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.

Table 16 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Output low voltage on port pins (with standard pads)	V_{OLP}	CC	–	1.0	V	$I_{OL} = 11 \text{ mA}$ (5 V) $I_{OL} = 7 \text{ mA}$ (3.3 V)
			–	0.4	V	$I_{OL} = 5 \text{ mA}$ (5 V) $I_{OL} = 3.5 \text{ mA}$ (3.3 V)
Output low voltage on high current pads	V_{OLP1}	CC	–	1.0	V	$I_{OL} = 50 \text{ mA}$ (5 V) $I_{OL} = 25 \text{ mA}$ (3.3 V)
			–	0.32	V	$I_{OL} = 10 \text{ mA}$ (5 V)
			–	0.4	V	$I_{OL} = 5 \text{ mA}$ (3.3 V)
Output high voltage on port pins (with standard pads)	V_{OHP}	CC	$V_{DDP} - 1.0$	–	V	$I_{OH} = -10 \text{ mA}$ (5 V) $I_{OH} = -7 \text{ mA}$ (3.3 V)
			$V_{DDP} - 0.4$	–	V	$I_{OH} = -4.5 \text{ mA}$ (5 V) $I_{OH} = -2.5 \text{ mA}$ (3.3 V)
Output high voltage on high current pads	V_{OHP1}	CC	$V_{DDP} - 0.32$	–	V	$I_{OH} = -6 \text{ mA}$ (5 V)
			$V_{DDP} - 1.0$	–	V	$I_{OH} = -8 \text{ mA}$ (3.3 V)
			$V_{DDP} - 0.4$	–	V	$I_{OH} = -4 \text{ mA}$ (3.3 V)
Input low voltage on port pins (Standard Hysteresis)	V_{ILPS}	SR	–	$0.19 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input high voltage on port pins (Standard Hysteresis)	V_{IHPS}	SR	$0.7 \times V_{DDP}$	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)

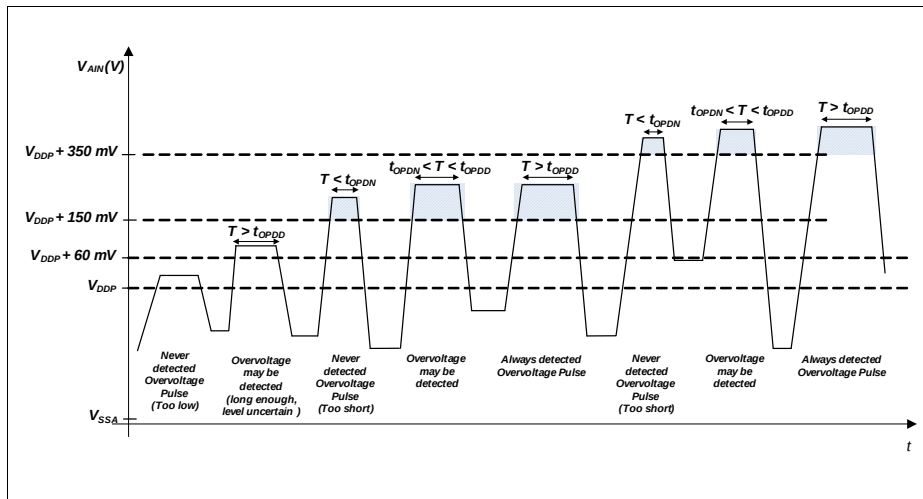


Figure 14 ORC Detection Ranges

3.2.4 Analog Comparator Characteristics

Table 19 below shows the Analog Comparator characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 19 Analog Comparator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Notes/ Test Conditions
			Min.	Typ.	Max.		
Input Voltage	V_{CMP}	SR	-0.05	—	$V_{DDP} + 0.05$	V	
Input Offset	V_{CMPOFF}	CC	—	+/-3	—	mV	High power mode $\Delta V_{CMP} < 200$ mV
Propagation Delay ¹⁾	t_{PDELAY}	CC	—	25	—	ns	High power mode, $\Delta V_{CMP} = 100$ mV
			—	80	—	ns	High power mode, $\Delta V_{CMP} = 25$ mV
			—	250	—	ns	Low power mode, $\Delta V_{CMP} = 100$ mV
			—	700	—	ns	Low power mode, $\Delta V_{CMP} = 25$ mV
Current Consumption	I_{ACMP}	CC	—	100	—	μA	First active ACMP in high power mode, $\Delta V_{CMP} > 30$ mV
			—	66	—	μA	Each additional ACMP in high power mode, $\Delta V_{CMP} > 30$ mV
			—	10	—	μA	First active ACMP in low power mode
			—	6	—	μA	Each additional ACMP in low power mode
Input Hysteresis	V_{HYS}	CC	—	+/-15	—	mV	
Filter Delay ¹⁾	t_{FDELAY}	CC	—	5	—	ns	

1) Total Analog Comparator Delay is the sum of Propagation Delay and Filter Delay.

Table 21 OSC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	4	–	48	MHz	Direct Input Mode
		4	–	20	MHz	External Crystal Mode
Oscillator start-up time ¹⁾²⁾	t_{OSCS} CC	–	–	10	ms	
Input voltage at XTAL1	V_{IX} SR	-0.3	–	1.5	V	External Crystal Mode
		-0.3	–	5.5	V	Direct Input Mode
Input amplitude (peak-to-peak) at XTAL1 ²⁾³⁾	V_{PPX} SR	0.6	–	1.7	V	External Crystal Mode

1) t_{OSCS} is defined from the moment the oscillator is enabled with SCU_ANAOSCHPCTRL.MODE until the oscillations reach an amplitude at XTAL1 of $0.9 * V_{PPX}$.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) If the shaper unit is enabled and not bypassed.

3.2.8 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase time per page / sector	$t_{\text{ERASE CC}}$	6.8	7.1	7.6	ms	
Program time per block	$t_{\text{PSER CC}}$	102	152	204	μs	
Wake-Up time	$t_{\text{WU CC}}$	–	32.2	–	μs	
Read time per word	$t_{\text{a CC}}$	–	50	–	ns	
Data Retention Time	$t_{\text{RET CC}}$	10	–	–	years	Max. 100 erase / program cycles
Flash Wait States ¹⁾	$N_{\text{WSFLASH CC}}$	0	0	0		$f_{\text{MCLK}} = 8 \text{ MHz}$
		0	1	1		$f_{\text{MCLK}} = 16 \text{ MHz}$
		1	2	2		$f_{\text{MCLK}} = 32 \text{ MHz}$
		2	2	3		$f_{\text{MCLK}} = 48 \text{ MHz}$
Erase Cycles	$N_{\text{ECYC CC}}$	–	–	$5 \cdot 10^4$	cycles	Sum of page and sector erase cycles
Total Erase Cycles	$N_{\text{TECYC CC}}$	–	–	$2 \cdot 10^6$	cycles	

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

3.3.4 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 29 SWD Interface Timing Parameters(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SWDCLK high time	t_1 SR	50	—	500000	ns	—
SWDCLK low time	t_2 SR	50	—	500000	ns	—
SWDIO input setup to SWDCLK rising edge	t_3 SR	10	—	—	ns	—
SWDIO input hold after SWDCLK rising edge	t_4 SR	10	—	—	ns	—
SWDIO output valid time after SWDCLK rising edge	t_5 CC	—	—	68	ns	$C_L = 50$ pF
		—	—	62	ns	$C_L = 30$ pF
SWDIO output hold time from SWDCLK rising edge	t_6 CC	4	—	—	ns	

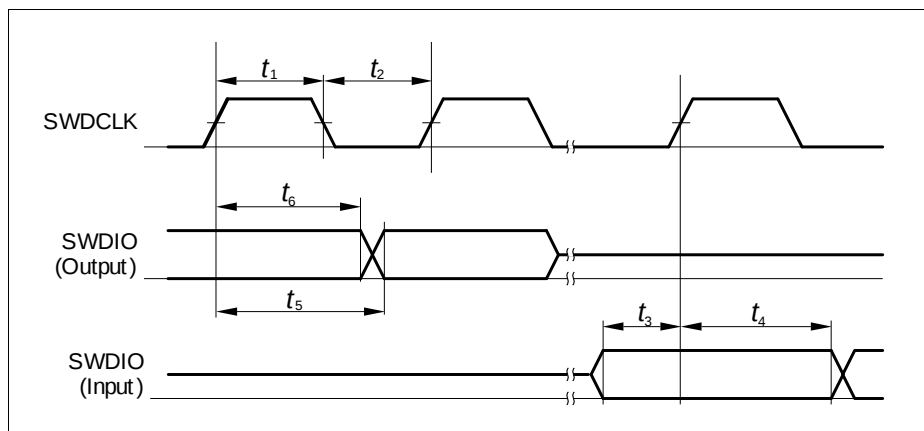


Figure 24 SWD Timing

Table 32 USIC SSC Slave Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 hold after last clock input DX1 receive edge ¹⁾	t_{11} SR	17	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge ¹⁾	t_{12} SR	21	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge ¹⁾	t_{13} SR	15	–	–	ns	
Data output DOUT[3:0] valid time	t_{14} CC	-	–	71	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

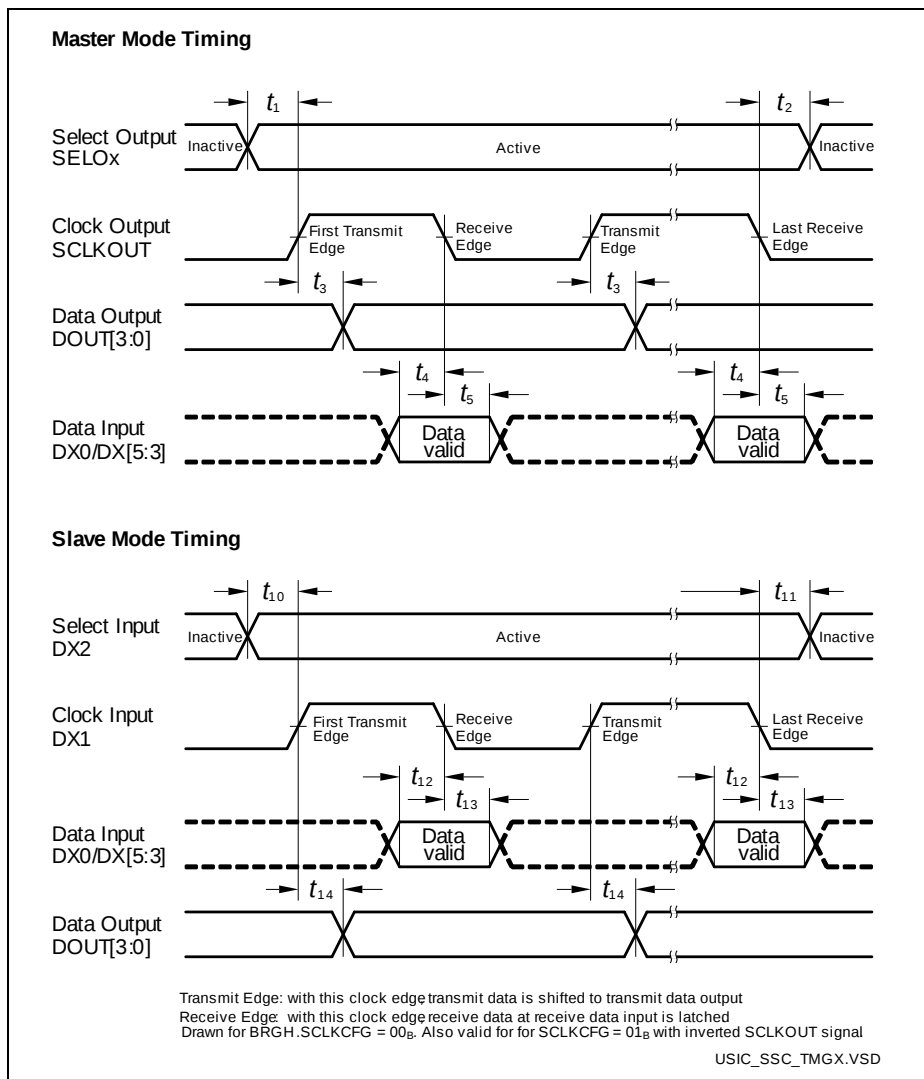


Figure 25 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

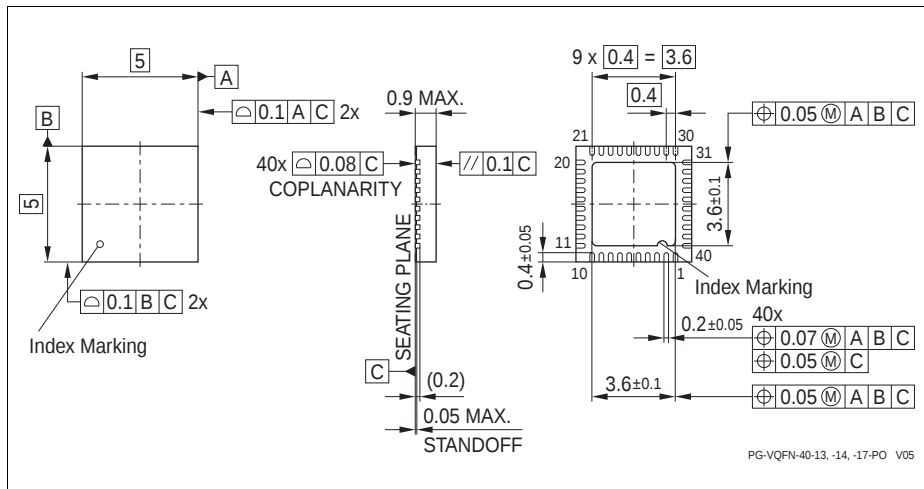


Figure 30 PG-VQFN-40-17

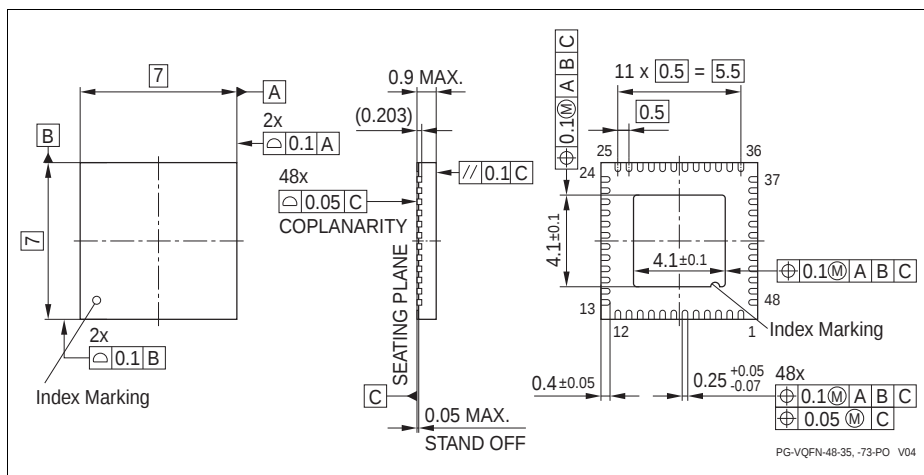


Figure 31 PG-VQFN-48-73

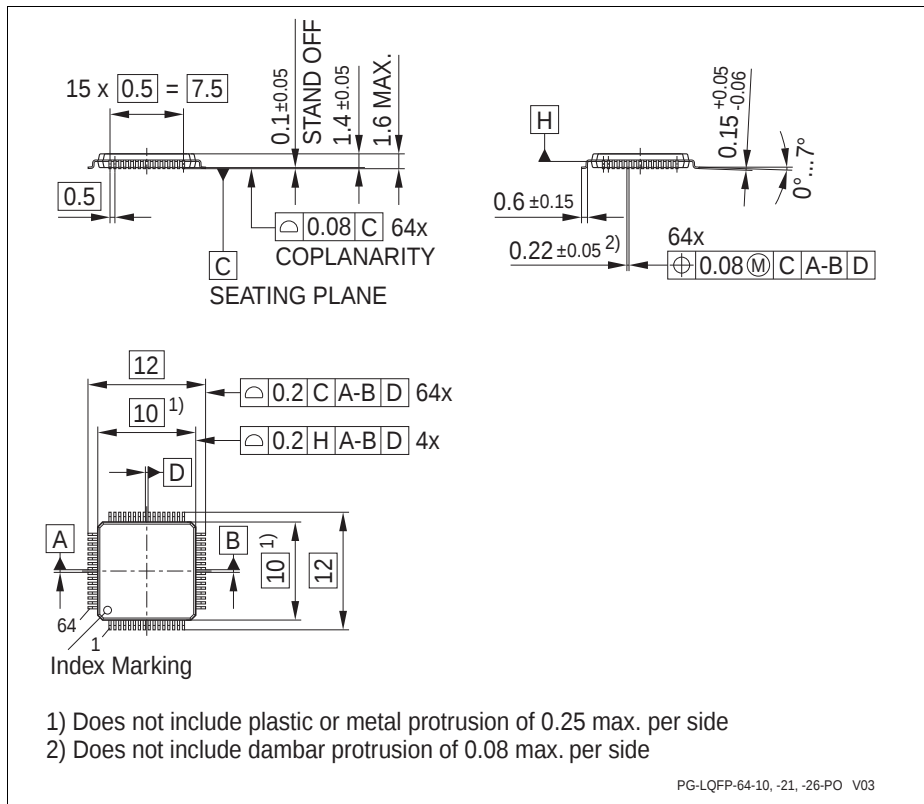


Figure 32 PG-LQFP-64-26