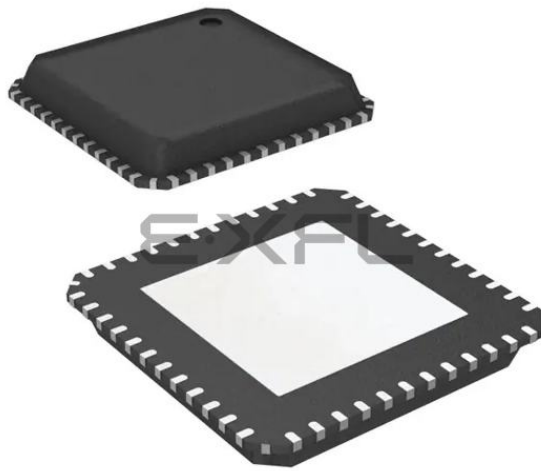




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I ² S, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-73
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1402q048x0032aaxuma1

Table of Contents

4.1.1	Thermal Considerations	83
4.2	Package Outlines	85
5	Quality Declaration	88

Table 1 Features of XMC1400 Device Types¹⁾ (cont'd)

Features		XMC1401-Q048	XMC1401-F064	XMC1402-T038	XMC1402-Q040	XMC1402-Q048	XMC1402-Q064	XMC1402-F064	XMC1403-Q040	XMC1403-Q048	XMC1403-Q064	XMC1404-Q048	XMC1404-Q064	XMC1404-F064
Analog	ADC (kernels / analog inputs)	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12	2 / 12
	ACMP	-	-	3	3	4	4	4	-	-	-	4	4	4
GPIOs		34	48	26	27	34	48	48	27	34	48	34	48	48
GPIOs		8	8	8	8	8	8	8	8	8	8	8	8	8
Packages		VQFN-48	LQFP-64	TSSOP-38	VQFN-40	VQFN-48	VQFN-64	LQFP-64	VQFN-40	VQFN-48	VQFN-64	VQFN-48	VQFN-64	LQFP-64

1) Features that are not included in this table are available in all the derivatives

1.2 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code "XMC1<DDD>-<Z><PPP><T><FFFF>" identifies:

- <DDD> the derivatives function set
- <Z> the package variant
 - T: TSSOP
 - Q: VQFN
 - F: LQFP
- <PPP> package pin count
- <T> the temperature range:
 - F: -40°C to 85°C
 - X: -40°C to 105°C
- <FFFF> the Flash memory size in Kbytes.

For ordering codes for the XMC1400 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1400 series, some descriptions may not apply to a specific product. Please see [Table 2](#).

For simplicity the term **XMC1400** is used for all derivatives throughout this document.

Table 3 XMC1400 Chip Identification Number (cont'd)

Derivative	Value	Marking
XMC1403-Q064X0200	00014093 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00033000 10204083 _H	AA
XMC1404-Q048X0064	00014083 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00011000 10204083 _H	AA
XMC1404-Q048X0128	00014083 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00021000 10204083 _H	AA
XMC1404-Q048X0200	00014083 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00033000 10204083 _H	AA
XMC1404-Q064X0064	00014093 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00011000 10204083 _H	AA
XMC1404-Q064X0128	00014093 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00021000 10204083 _H	AA
XMC1404-Q064X0200	00014093 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00033000 10204083 _H	AA
XMC1404-F064X0064	000140A3 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00011000 10204083 _H	AA
XMC1404-F064X0128	000140A3 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00021000 10204083 _H	AA
XMC1404-F064X0200	000140A3 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00033000 10204083 _H	AA

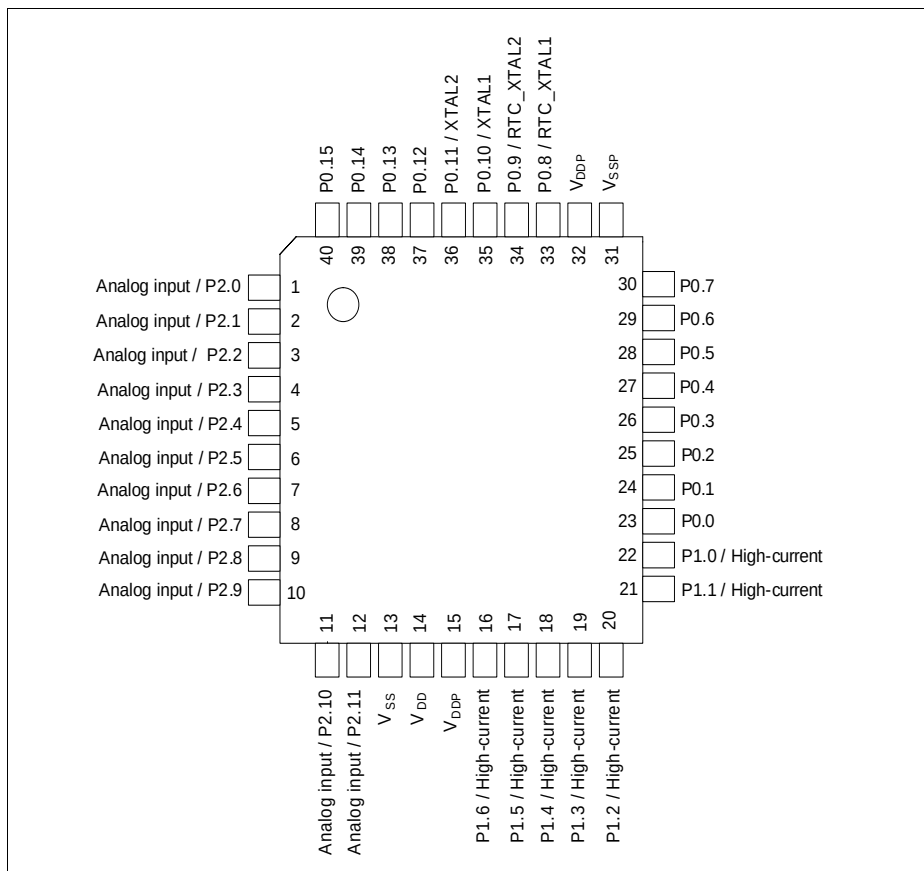


Figure 7 XMC1400 PG-VQFN-40-17 Pin Configuration (top view)

General Device Information

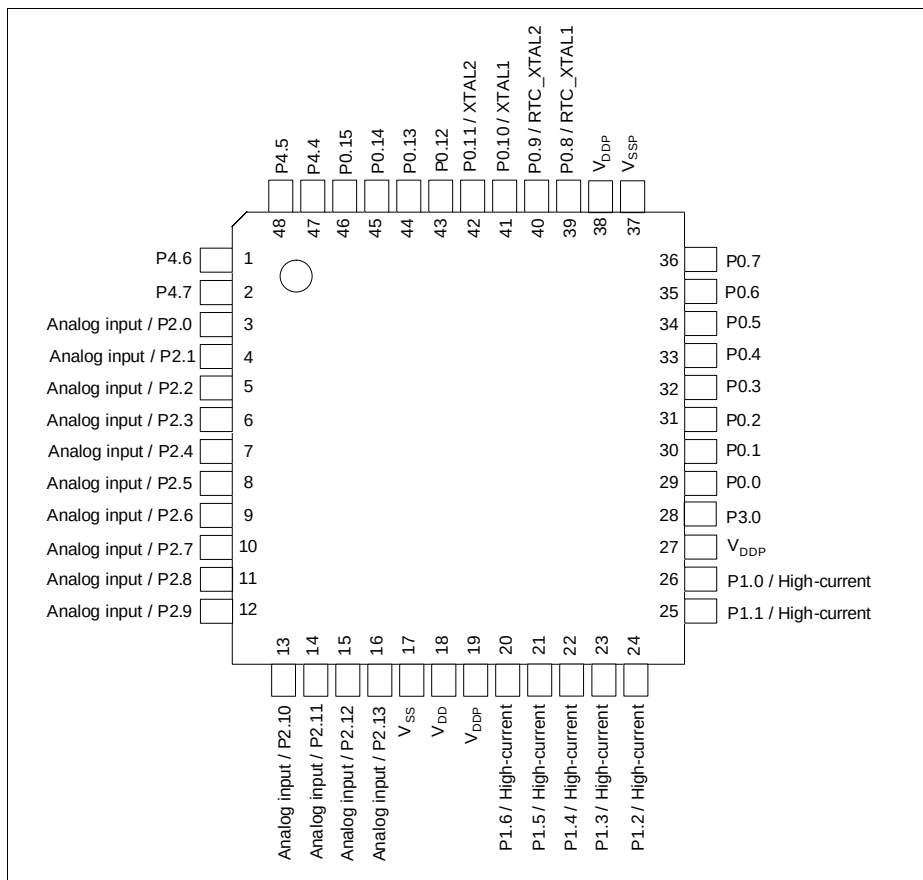


Figure 8 XMC1400 PG-VQFN-48-73 Pin Configuration (top view)

General Device Information

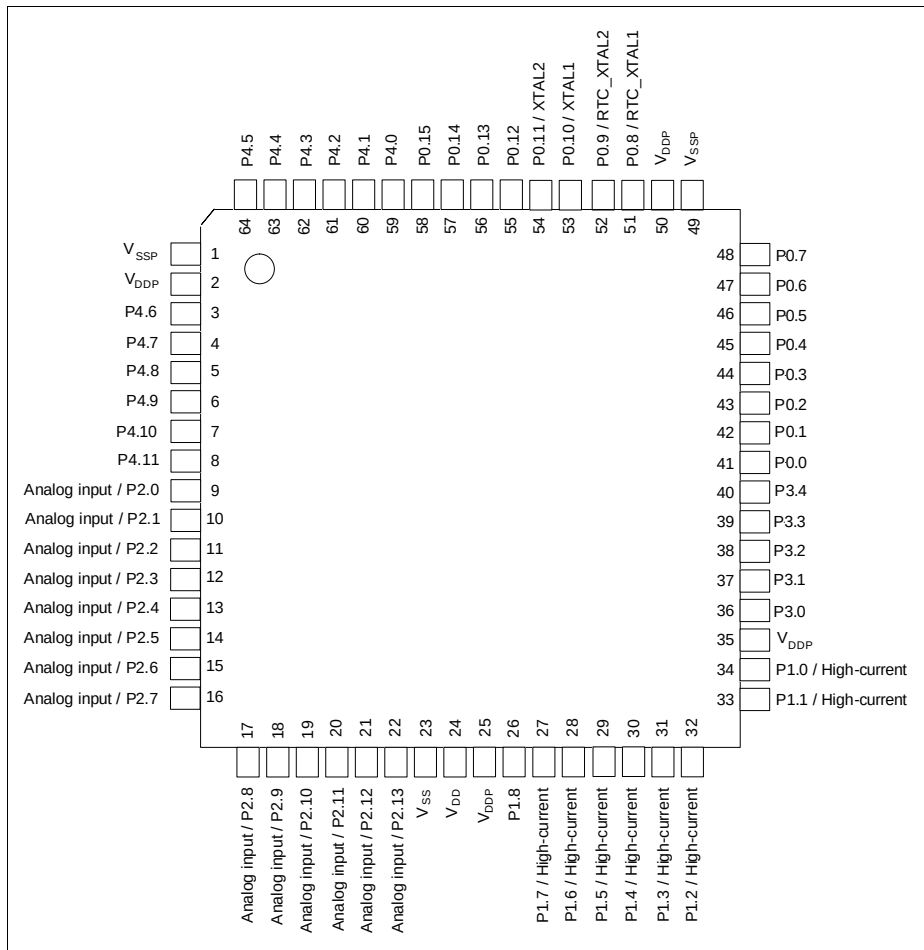


Figure 9 XMC1400 PG-LQFP-64-26 / PG-VQFN-64-6 Pin Configuration (top view)

Port I/O Function Table

Table 9 Port I/O Functions

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0.P DOUT0	LEDTS0 .LINE7	ERU0.G OUT0	CCU40. OUT0	CCU80. OUT00	USIC0_ CH0.SE LO0	USIC0_ CH1.SE LO0	CCU81. OUT00	USIC1_ CH1.DO UT0	BCCU0. TRAPIN B	CCU40.I N0AC					USIC1_ CH1.DX 0A	USIC0_ CH0.D X2A		USIC0_ CH1.DX 2A		
P0.1	ERU0.P DOUT1	LEDTS0 .LINE6	ERU0.G OUT1	CCU40. OUT1	CCU80. OUT01	BCCU0. OUT8	SCU.VD ROP	USIC1_ CH1.SC LKOUT	USIC1_ CH1.DO UT0		CCU40.I N1AC					USIC1_ CH1.DX 0B	USIC1_ CH1.D X1A				
P0.2	ERU0.P DOUT2	LEDTS0 .LINE5	ERU0.G OUT2	CCU40. OUT2	CCU80. OUT02	VADC0. EMUX02	CCU80. OUT10	USIC1_ CH0.SC LKOUT	USIC1_ CH0.DO UT0		CCU40.I N2AC					USIC1_ CH0.DX 0A	USIC1_ CH0.D X1A				
P0.3	ERU0.P DOUT3	LEDTS0 .LINE4	ERU0.G OUT3	CCU40. OUT3	CCU80. OUT03	VADC0. EMUX01	CCU80. OUT11	USIC1_ CH1.SC LKOUT	USIC1_ CH0.DO UT0		CCU40.I N3AC					USIC1_ CH0.DX 0B					
P0.4	BCCU0. OUT0	LEDTS0 .LINE3	LEDTS0 .COL3	CCU40. OUT1	CCU80. OUT13	VADC0. EMUX00	WWDT. SERVIC E_OUT	USIC1_ CH1.SE LO0	CAN.N0 _TXD			CCU41.I N0AB	CCU80.I N0AB							CAN.N0 _RXDA	
P0.5	BCCU0. OUT1	LEDTS0 .LINE2	LEDTS0 .COL2	CCU40. OUT0	CCU80. OUT12	ACMP2. OUT	CCU80. OUT01	VADC0. EMUX10	CAN.N0 _TXD			CCU41.I N1AB	CCU80.I N1AB							CAN.N0 _RXDB	
P0.6	BCCU0. OUT2	LEDTS0 .LINE1	LEDTS0 .COL1	CCU40. OUT0	CCU80. OUT11	USIC0_ CH1.MC LKOUT	USIC0_ CH1.DO UT0	VADC0. EMUX11	CCU41. OUT0		CCU40.I N0AB	CCU41.I N2AB					USIC0_ CH1.DX 0C				
P0.7	BCCU0. OUT3	LEDTS0 .LINE0	LEDTS0 .COL0	CCU40. OUT1	CCU80. OUT10	USIC0_ CH0.SC LKOUT	USIC0_ CH1.DO UT0	VADC0. EMUX12	CCU41. OUT1		CCU40.I N1AB	CCU41.I N3AB					USIC0_ CH0.D X1C	USIC0_ CH1.DX 0D	USIC0_ CH1.DX 1C		
P0.8/ RTC_XTAL1	BCCU0. OUT4	LEDTS1 .LINE0	LEDTS0 .COLA	CCU40. OUT2	CCU80. OUT20	USIC0_ CH0.SC LKOUT	USIC0_ CH1.SC LKOUT	CCU81. OUT20	CCU41. OUT2		CCU40.I N2AB					USIC0_ CH0.D X1B		USIC0_ CH1.DX 1B			
P0.9/ RTC_XTAL2	BCCU0. OUT5	LEDTS1 .LINE1	LEDTS0 .COL6	CCU40. OUT3	CCU80. OUT21	USIC0_ CH0.SE LO0	USIC0_ CH1.SE LO0	CCU81. OUT21	CCU41. OUT3		CCU40.I N3AB					USIC0_ CH0.D X2B		USIC0_ CH1.DX 2B			
P0.10/ XTAL1	BCCU0. OUT6	LEDTS1 .LINE2	LEDTS0 .COL5	ACMP0. OUT	CCU80. OUT22	USIC0_ CH0.SE LO1	USIC0_ CH1.SE LO1	CCU81. OUT22					CCU80.I N2AB	CCU81.I N2AB		USIC0_ CH0.D X2C		USIC0_ CH1.DX 2C			
P0.11/ XTAL2	BCCU0. OUT7	LEDTS1 .LINE3	LEDTS0 .COL4	USIC0_ CH0.MC LKOUT	CCU80. OUT23	USIC0_ CH0.SE LO2	USIC0_ CH1.SE LO2	CCU81. OUT23								USIC0_ CH0.D X2D		USIC0_ CH1.DX 2D			
P0.12	BCCU0. OUT6	LEDTS1 .LINE4	LEDTS0 .COL3	LEDTS1 .COL3	CCU80. OUT33	USIC0_ CH0.SE LO3	CCU80. OUT20		CAN.N1 _TXD	BCCU0. TRAPIN A	CCU40.I N0AA	CCU40.I N1AA	CCU40.I N2AA	CCU81.I N0AU	CCU40.I N3AA	CCU80.I N0AA	USIC0_ CH0.D X2E	CCU80.I N1AA	CCU80.I N2AA	CAN.N1 _RXDA	CCU80.I N3AA

Table 9 Port I/O Functions (cont'd)

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P2.2										ACMP2.I NN	VADC0. G0CH7		ORC0.A N	USIC1_ CH0.DX 5E		USIC0_ CH0.DX 3A	USIC0_ CH0.D X4A	USIC0_ CH1.DX 5A			ERU0.0 B1
P2.3												VADC0. G1CH5	ORC1.A N	USIC1_ CH0.DX 3E	USIC1_ CH0.DX 4E	USIC1_ CH0.DX 5C	USIC0_ CH0.D X5B	USIC0_ CH1.DX 3C	USIC0_ CH1.DX 4C		ERU0.1 B1
P2.4												VADC0. G1CH6	ORC2.A N	USIC1_ CH1.DX 3C	USIC1_ CH1.DX 4C	USIC0_ CH0.DX 3B	USIC0_ CH0.D X4B	USIC1_ CH0.DX 5F	USIC0_ CH1.DX 5B		ERU0.0 A1
P2.5												VADC0. G1CH7	ORC3.A N	USIC1_ CH1.DX 5D		USIC0_ CH0.DX 5D		USIC0_ CH1.DX 3E	USIC0_ CH1.DX 4E		ERU0.1 A1
P2.6										ACMP1.I NN	VADC0. G0CH0		ORC4.A N	USIC1_ CH1.DX 3E	USIC1_ CH1.DX 4E	USIC0_ CH0.DX 3E	USIC0_ CH0.D X4E	USIC0_ CH1.DX 5D			ERU0.2 A1
P2.7										ACMP1.I NP		VADC0. G1CH1	ORC5.A N	USIC1_ CH1.DX 5E		USIC0_ CH0.DX 5C		USIC0_ CH1.DX 3D	USIC0_ CH1.DX 4D		ERU0.3 A1
P2.8										ACMP0.I NN	VADC0. G0CH1	VADC0. G1CH0	ORC6.A N			USIC0_ CH0.DX 3D	USIC0_ CH0.D X4D	USIC0_ CH1.DX 5C			ERU0.3 B1
P2.9										ACMP0.I NP	VADC0. G0CH2	VADC0. G1CH4	ORC7.A N			USIC0_ CH0.DX 5A		USIC0_ CH1.DX 3B	USIC0_ CH1.DX 4B		ERU0.3 B0
P2.10	ERU0.P DOUT1	CCU40. OUT2	ERU0.G OUT1	LEDTS1 .COL4	CCU80. OUT30	ACMP0. OUT	USIC0_ CH1.DO UT0		CAN.N1 _TXD		VADC0. G0CH3	VADC0. G1CH2				USIC0_ CH0.DX 3C	USIC0_ CH0.D X4C	USIC0_ CH1.DX 0F		CAN.N1 _RXDE	ERU0.2 B0
P2.11	ERU0.P DOUT0	CCU40. OUT3	ERU0.G OUT0	LEDTS1 .COL3	CCU80. OUT31	USIC0_ CH1.SC LKOUT	USIC0_ CH1.DO UT0		CAN.N1 _TXD	ACMP.R EF	VADC0. G0CH4	VADC0. G1CH3						USIC0_ CH1.DX 0E	USIC0_ CH1.DX 1E	CAN.N1 _RXDF	ERU0.2 B1
P2.12	BCCU0. OUT3	VADC0. EMUX00	USIC1_ CH0.SC LKOUT	USIC1_ CH1.SC LKOUT		ACMP2. OUT	USIC1_ CH1.DO UT0	LEDTS2 .COL6		ACMP3.I NN						USIC1_ CH0.DX 3A	USIC0_ CH0.D X4A	USIC1_ CH1.DX 0C	USIC1_ CH1.DX 1B		ERU1.3 A2
P2.13	BCCU0. OUT4	CCU40. OUT3	USIC1_ CH0.MC LKOUT	CCU81. OUT31		VADC0. EMUX01	USIC1_ CH1.DO UT0	CCU81. OUT33	CCU41. OUT3	ACMP3.I NP						USIC1_ CH0.DX 5A		USIC1_ CH1.DX 0D			ERU1.3 A3
P3.0	BCCU0. OUT0	USIC1_ CH1.DO UT0	USIC1_ CH1.SC LKOUT	LEDTS2 .COLA	CCU80. OUT21	ACMP1. OUT	USIC1_ CH0.SE LO1	CCU81. OUT21	CCU41. OUT0	BCCU0. TRAPIN C	CCU41.I N0AA	CCU41.I N1AA	CCU41.I N2AA	CCU41.I N3AA	CCU81.I N0AA	CCU81.I N1AA	CCU81. IN2AA	USIC1_ CH1.DX 0E	USIC1_ CH1.DX 1D	CCU81.I N3AA	ERU1.0 A1
P3.1	BCCU0. OUT1	USIC1_ CH1.DO UT0		LEDTS2 .COL0	CCU80. OUT20	ACMP3. OUT	USIC1_ CH0.SE LO0	CCU81. OUT20	CCU41. OUT1								USIC1_ CH0.D X2F	USIC1_ CH1.DX 0F			ERU1.1 A1

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 12 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
 - pad supply levels (V_{DDP})
 - temperature

If a pin current is outside of the **Operating Conditions** but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 12 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	
Absolute sum of all input circuit currents during overload condition	I_{OVS} SR	–	–	25	mA	

Figure 11 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

Electrical Parameter
Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input low voltage on port pins (Large Hysteresis)	V_{ILPL}	SR	—	$0.08 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input high voltage on port pins (Large Hysteresis)	V_{IHPL}	SR	$0.85 \times V_{DDP}$	—	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Rise/fall time on High Current Pad ¹⁾	t_{HCPR} , t_{HCPF}	CC	—	9	ns	50 pF @ 5 V ²⁾
			—	12	ns	50 pF @ 3.3 V ³⁾
			—	25	ns	50 pF @ 1.8 V ⁴⁾
Rise/fall time on Standard Pad ¹⁾	t_R , t_F	CC	—	12	ns	50 pF @ 5 V ⁵⁾
			—	15	ns	50 pF @ 3.3 V ⁶⁾ .
			—	31	ns	50 pF @ 1.8 V ⁷⁾ .
Input Hysteresis on port pin except P2.3 - P2.9 ⁸⁾	HYS	CC	$0.08 \times V_{DDP}$	—	V	CMOS Mode (5 V), Standard Hysteresis
			$0.03 \times V_{DDP}$	—	V	CMOS Mode (3.3 V), Standard Hysteresis
			$0.02 \times V_{DDP}$	—	V	CMOS Mode (2.2 V), Standard Hysteresis
			$0.5 \times V_{DDP}$	$0.75 \times V_{DDP}$	V	CMOS Mode(5 V), Large Hysteresis
			$0.4 \times V_{DDP}$	$0.75 \times V_{DDP}$	V	CMOS Mode(3.3 V), Large Hysteresis
			$0.2 \times V_{DDP}$	$0.65 \times V_{DDP}$	V	CMOS Mode(2.2 V), Large Hysteresis

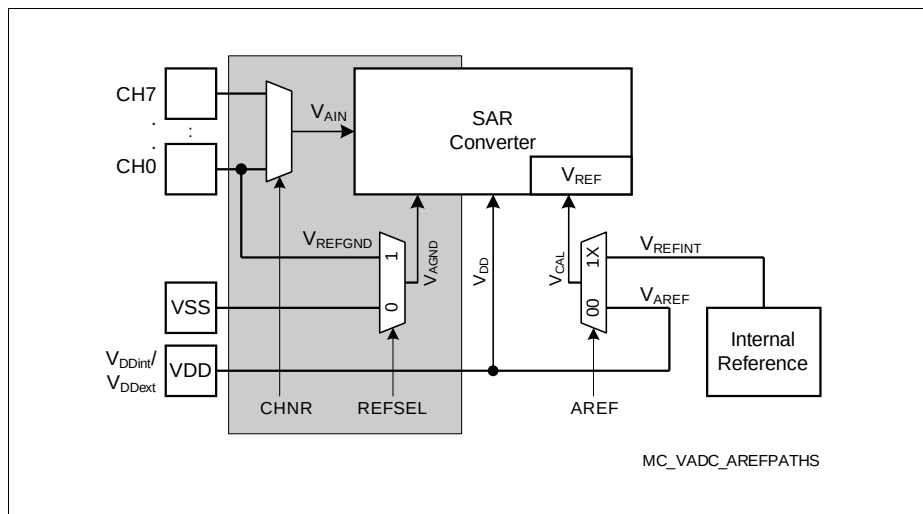


Figure 12 ADC Voltage Supply

3.2.4 Analog Comparator Characteristics

Table 19 below shows the Analog Comparator characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 19 Analog Comparator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Notes/ Test Conditions
			Min.	Typ.	Max.		
Input Voltage	V_{CMP}	SR	-0.05	—	$V_{DDP} + 0.05$	V	
Input Offset	V_{CMPOFF}	CC	—	+/-3	—	mV	High power mode $\Delta V_{CMP} < 200$ mV
Propagation Delay ¹⁾	t_{PDELAY}	CC	—	25	—	ns	High power mode, $\Delta V_{CMP} = 100$ mV
			—	80	—	ns	High power mode, $\Delta V_{CMP} = 25$ mV
			—	250	—	ns	Low power mode, $\Delta V_{CMP} = 100$ mV
			—	700	—	ns	Low power mode, $\Delta V_{CMP} = 25$ mV
Current Consumption	I_{ACMP}	CC	—	100	—	μA	First active ACMP in high power mode, $\Delta V_{CMP} > 30$ mV
			—	66	—	μA	Each additional ACMP in high power mode, $\Delta V_{CMP} > 30$ mV
			—	10	—	μA	First active ACMP in low power mode
			—	6	—	μA	Each additional ACMP in low power mode
Input Hysteresis	V_{HYS}	CC	—	+/-15	—	mV	
Filter Delay ¹⁾	t_{FDELAY}	CC	—	5	—	ns	

1) Total Analog Comparator Delay is the sum of Propagation Delay and Filter Delay.

Table 22 RTC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	–	32.768	–	kHz	
Oscillator start-up time ¹⁾²⁾	t_{OSCS} CC	–	–	5	s	
Input voltage at RTC_XTAL1	V_{IX} SR	-0.3	–	1.5	V	
Input amplitude (peak-to-peak) at RTC_XTAL1 ²⁾³⁾	V_{PPX} SR	0.2	–	1.2	V	

1) t_{OSCS} is defined from the moment the oscillator is enabled by the user with SCU_ANAOSCLPCTRL.MODE until the oscillations reach an amplitude at RTC_XTAL1 of $0.9 * V_{PPX}$.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) If the shaper unit is enabled and not bypassed.

3.3.2 Power-Up and Supply Threshold Characteristics

Table 26 provides the characteristics of the supply threshold in XMC1400.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DDP} is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 26 Power-Up and Supply Threshold Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} ramp-up time	t_{RAMPUP} SR	$V_{DDP}/S_{VDDPrise}$	–	10^7	μs	
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	$V/\mu s$	Slope during normal operation
	S_{VDDP10} SR	0	–	10	$V/\mu s$	Slope during fast transient within +/- 10% of V_{DDP}
	$S_{VDDPrise}$ SR	0	–	10	$V/\mu s$	Slope during power-on or restart after brownout event
	$S_{VDDPfall}^{1)}$ SR	0	–	0.25	$V/\mu s$	Slope during supply falling out of the +/- 10% limits ²⁾
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00 _B
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01 _B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10 _B

3.3.3 On-Chip Oscillator Characteristics

Table 27 provides the characteristics of the 96 MHz digital controlled oscillator DCO1.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 27 96 MHz DCO1 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ	Max.		
Nominal frequency	f_{NOM}	CC	–	96	–	MHz	under nominal conditions ¹⁾ after trimming
Accuracy with adjustment based on XTAL as reference	Δf_{LTX}	CC	-0.3	–	0.3	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature (-40 °C to 105 °C)
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature (0 °C to 85 °C)
			-3.9	–	4.0	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature (-40 °C to 105 °C)

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and $T_{\text{A}} = + 25\text{ °C}$.

Table 28 provides the characteristics of the 32 kHz digital controlled oscillator DCO2.

Table 28 32 kHz DCO2 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	–	32.75	–	kHz	under nominal conditions ¹⁾ after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature (0 °C to 85 °C)
			-3.9	–	4.0	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature (-40 °C to 105 °C) ¹⁾

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and $T_{\text{A}} = + 25\text{ °C}$.

3.3.4 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 29 SWD Interface Timing Parameters(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SWDCLK high time	t_1 SR	50	—	500000	ns	—
SWDCLK low time	t_2 SR	50	—	500000	ns	—
SWDIO input setup to SWDCLK rising edge	t_3 SR	10	—	—	ns	—
SWDIO input hold after SWDCLK rising edge	t_4 SR	10	—	—	ns	—
SWDIO output valid time after SWDCLK rising edge	t_5 CC	—	—	68	ns	$C_L = 50$ pF
		—	—	62	ns	$C_L = 30$ pF
SWDIO output hold time from SWDCLK rising edge	t_6 CC	4	—	—	ns	

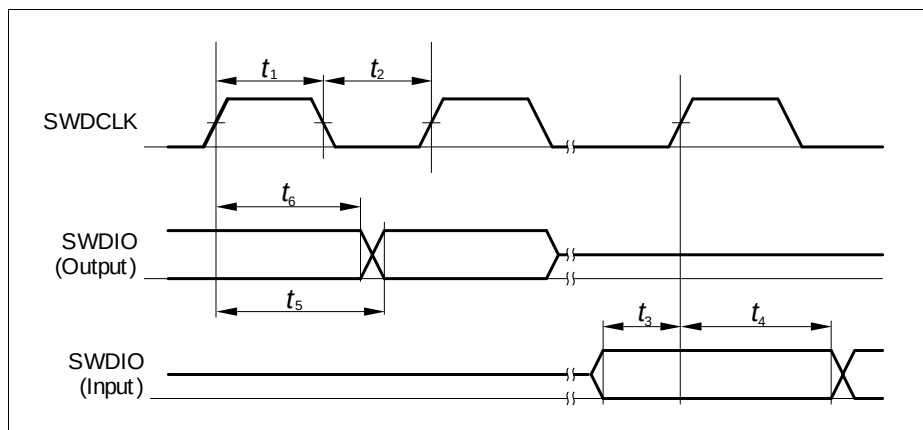


Figure 24 SWD Timing

3.3.6.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 33 USIC IIC Standard Mode Timing¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	μs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	μs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	μs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	μs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	μs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	μs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	μs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

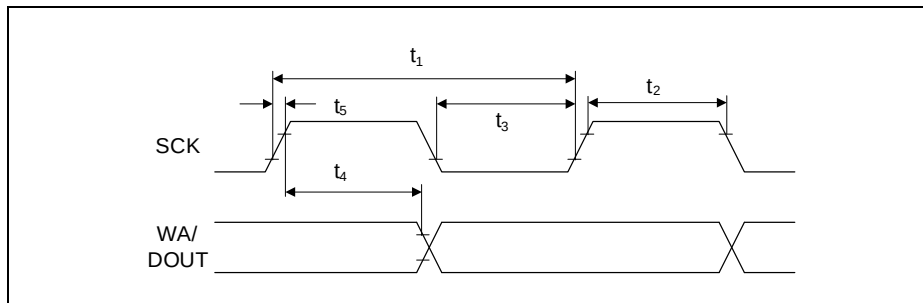


Figure 27 USIC IIS Master Transmitter Timing

Table 36 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	t_7 SR	$0.35 \times t_{6min}$	-	-	ns	
Clock Low	t_8 SR	$0.35 \times t_{6min}$	-	-	ns	
Set-up time	t_9 SR	$0.3 \times t_{6min}$	-	-	ns	
Hold time	t_{10} SR	15	-	-	ns	

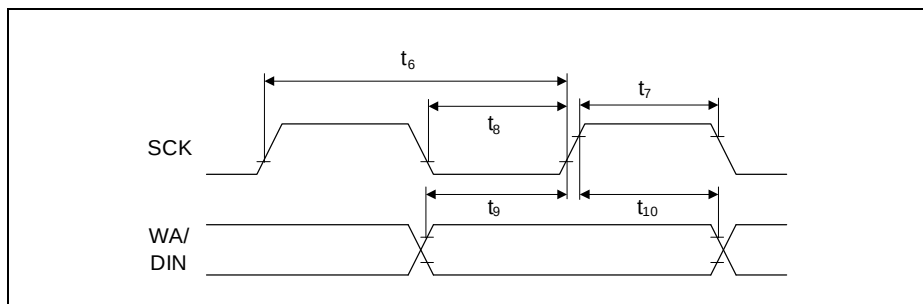


Figure 28 USIC IIS Slave Receiver Timing

4.2 Package Outlines

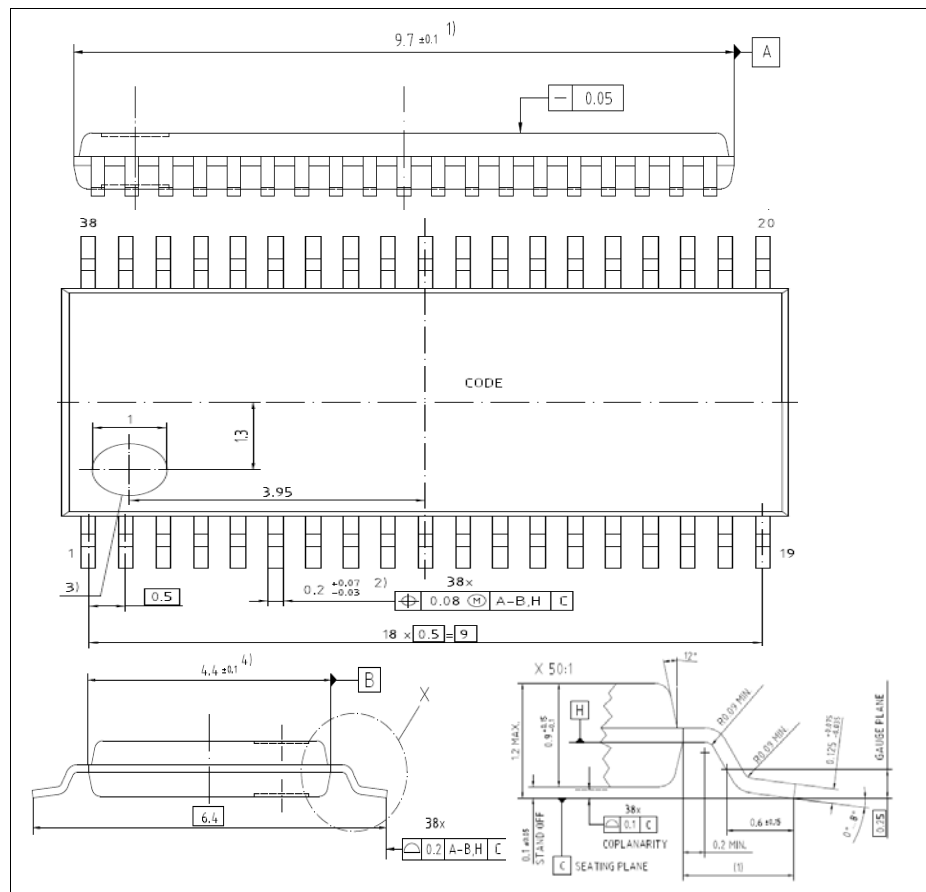


Figure 29 PG-TSSOP-38-9

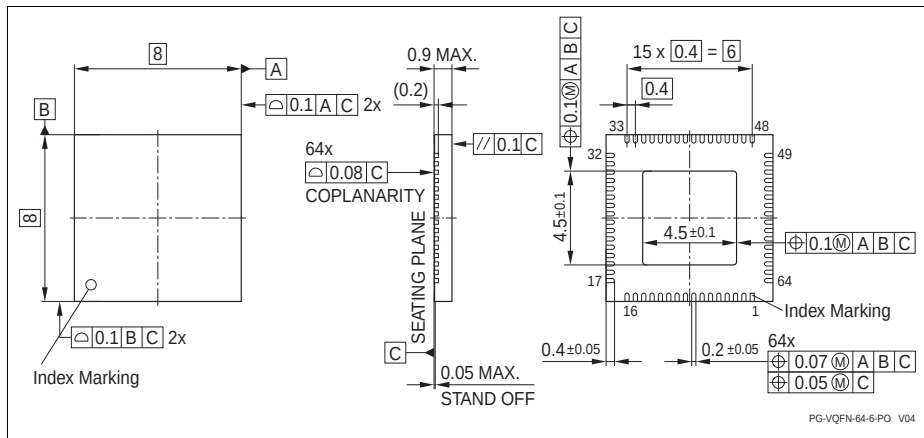


Figure 33 PG-VQFN-64-6

All dimensions in mm.

5 Quality Declaration

Table 38 shows the characteristics of the quality parameters in the XMC1400.

Table 38 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	-	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	-	3	-	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	-	260	°C	Profile according to JEDEC J-STD-020D