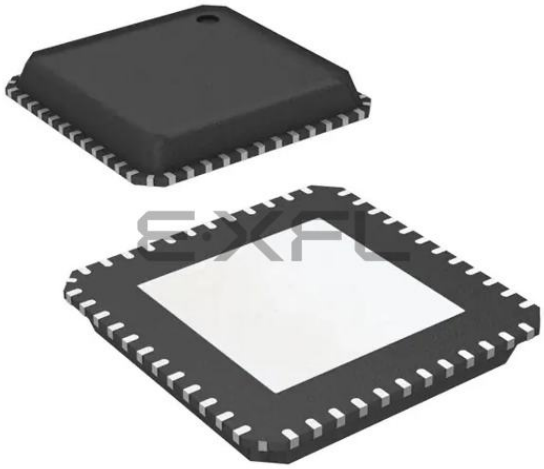
Infineon Technologies - XMC1402Q048X0064AAXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-73
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1402q048x0064aaxuma1

XMC1400 AA-Step

Microcontroller Series
for Industrial Applications

XMC1000 Family

ARM® Cortex®-M0
32-bit processor core

Data Sheet

V1.3 2016-10

Microcontrollers

Table of Contents

1.3 Device Types

These device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 2 Synopsis of XMC1400 Device Types

Derivative	Package	Flash Kbytes
XMC1401-Q048F0064	PG-VQFN-48	64
XMC1401-Q048F0128	PG-VQFN-48	128
XMC1401-F064F0064	PG-LQFP-64	64
XMC1401-F064F0128	PG-LQFP-64	128
XMC1402-T038X0032	PG-TSSOP-38	32
XMC1402-T038X0064	PG-TSSOP-38	64
XMC1402-T038X0128	PG-TSSOP-38	128
XMC1402-T038X0200	PG-TSSOP-38	200
XMC1402-Q040X0032	PG-VQFN-40	32
XMC1402-Q040X0064	PG-VQFN-40	64
XMC1402-Q040X0128	PG-VQFN-40	128
XMC1402-Q040X0200	PG-VQFN-40	200
XMC1402-Q048X0032	PG-VQFN-48	32
XMC1402-Q048X0064	PG-VQFN-48	64
XMC1402-Q048X0128	PG-VQFN-48	128
XMC1402-Q048X0200	PG-VQFN-48	200
XMC1402-Q064X0064	PG-VQFN-64	64
XMC1402-Q064X0128	PG-VQFN-64	128
XMC1402-Q064X0200	PG-VQFN-64	200
XMC1402-F064X0064	PG-LQFP-64	64
XMC1402-F064X0128	PG-LQFP-64	128
XMC1402-F064X0200	PG-LQFP-64	200
XMC1403-Q040X0064	PG-VQFN-40	64
XMC1403-Q040X0128	PG-VQFN-40	128
XMC1403-Q040X0200	PG-VQFN-40	200
XMC1403-Q048X0064	PG-VQFN-48	64
XMC1403-Q048X0128	PG-VQFN-48	128

1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is an 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location : 1000 $0F00_H$ (MSB) - 1000 $0F1B_H$ (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

Table 3 XMC1400 Chip Identification Number

Derivative	Value	Marking
XMC1401-Q048F0064	00014082 07CF00FF 1E071FF7 20006000 00000D00 00001000 00011000 10204083_H	AA
XMC1401-Q048F0128	00014082 07CF00FF 1E071FF7 20006000 00000D00 00001000 00021000 10204083_H	AA
XMC1401-F064F0064	000140A2 07CF00FF 1E071FF7 20006000 00000D00 00001000 00011000 10204083_H	AA
XMC1401-F064F0128	000140A2 07CF00FF 1E071FF7 20006000 00000D00 00001000 00021000 10204083_H	AA
XMC1402-T038X0032	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00009000 10204083_H	AA
XMC1402-T038X0064	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00011000 10204083_H	AA
XMC1402-T038X0128	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00021000 10204083_H	AA
XMC1402-T038X0200	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00033000 10204083_H	AA
XMC1402-Q040X0032	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00009000 10204083_H	AA
XMC1402-Q040X0064	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00011000 10204083_H	AA
XMC1402-Q040X0128	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00021000 10204083_H	AA
XMC1402-Q040X0200	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00033000 10204083_H	AA
XMC1402-Q048X0032	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00009000 10204083_H	AA

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

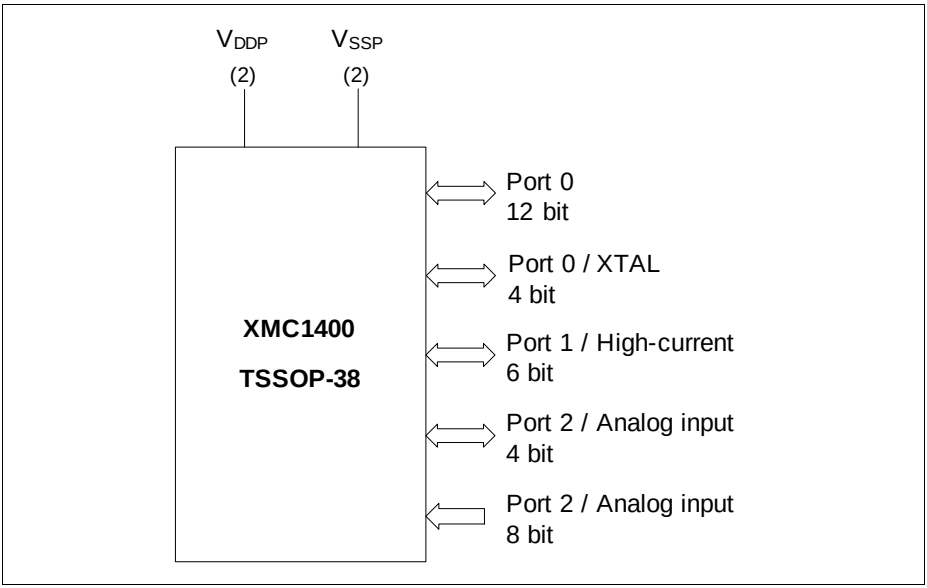

Figure 2 XMC1400 Logic Symbol for TSSOP-38-9

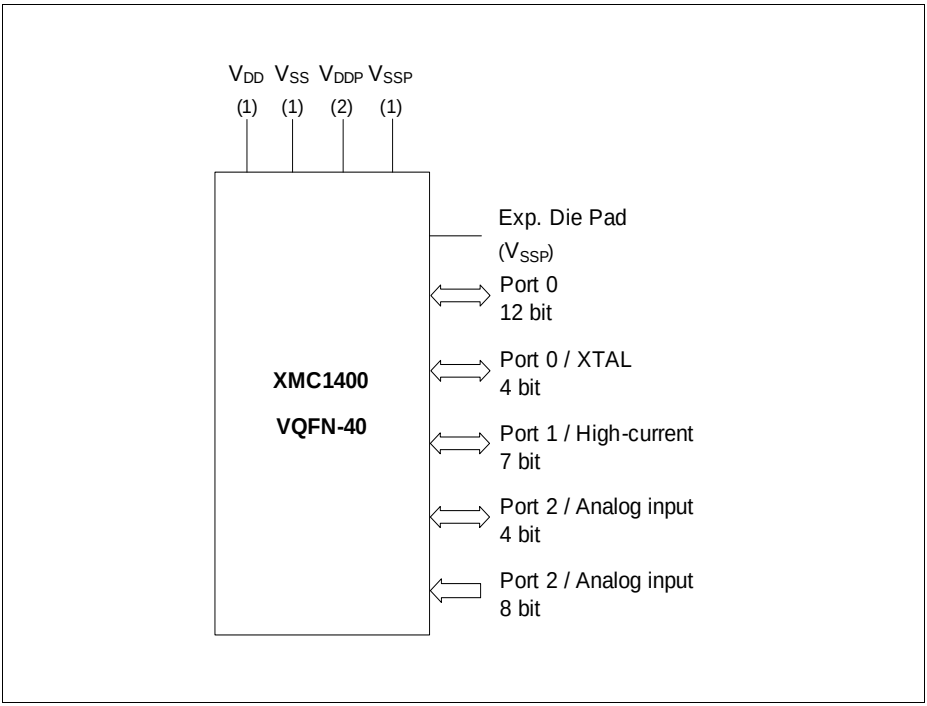

Figure 3 XMC1400 Logic Symbol for PG-VQFN-40-17

2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

Table 4 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type
Px.y	N	N		Pad Class

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type:

- STD_INOUT (standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- STD_INOUT/clock (standard bi-directional pads with oscillator function)
- High Current (high current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameter chapter.

Table 5 Package Pin Mapping

Function	LQFP 64, VQFN 64	VQFN 48	VQFN 40	TSSOP 38	Pad Type	Notes
P0.0	41	29	23	17	STD_INOUT	
P0.1	42	30	24	18	STD_INOUT	
P0.2	43	31	25	19	STD_INOUT	
P0.3	44	32	26	20	STD_INOUT	
P0.4	45	33	27	21	STD_INOUT	
P0.5	46	34	28	22	STD_INOUT	
P0.6	47	35	29	23	STD_INOUT	
P0.7	48	36	30	24	STD_INOUT	
P0.8/ RTC_ XTAL1	51	39	33	27	STD_INOUT /clock_IN	

2.2.3 Port I/O Function Description

The following general building block is used to describe the I/O functions of each PORT pin:

Table 7 Port I/O Function Description

Function	Outputs		Inputs	
	ALT1	ALTn	Input	Input
P0.0		MODA.OUT	MODC.INA	
Pn.y	MODA.OUT		MODA.INA	MODC.INB

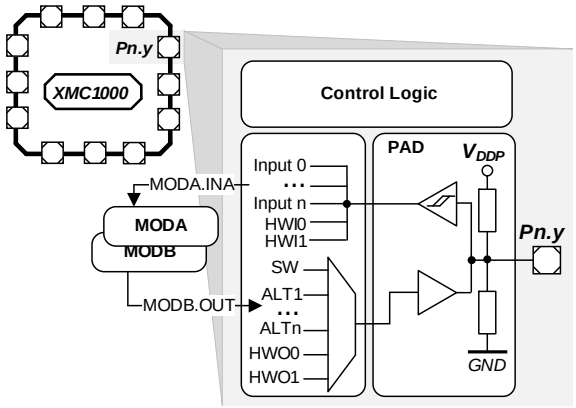

Figure 10 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to nine alternate output functions (ALT1 to ALT9) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

Please refer to the **Port I/O Functions** table for the complete Port I/O function mapping.

2.2.4 Hardware Controlled I/O Function Description

The following general building block is used to describe the hardware I/O and pull control functions of each PORT pin:

Table 8 Hardware Controlled I/O Function Description

Function	Outputs	Inputs	Pull Control	
	HWO0	**HWI0**	**HW0_PD**	**HW0_PU**
P0.0	MODB.OUT	MODB.INA		
Pn.y			$\overline{\text{MODC.OUT}}$	MODC.OUT

By Pn_HWSEL, it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers. Additional hardware signals HW0_PD/HW1_PD and HW0_PU/HW1_PU controlled by the peripherals can be used to control the pull devices of the pin.

Please refer to the **Hardware Controlled I/O Functions** table for the complete hardware I/O and pull control function mapping.

Table 9 Port I/O Functions (cont'd)

Function	Outputs									Inputs										
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P3.2	BCCU0.OUT2	USIC1_CH1.SCLKOUT		LEDTS2.COL1	CCU80.OUT11	ACMP2.OUT	USIC1_CH0.SCLKOUT	CCU81.OUT11	CCU41.OUT2							USIC1_CH0.DX3C	USIC1_CH0.DX4C	USIC1_CH1.DX3D	USIC1_CH1.DX4D		ERU1.2A1
P3.3	BCCU0.OUT5	USIC1_CH0.DOUT0		LEDTS2.COL2	CCU80.OUT10	ACMP0.OUT	USIC1_CH1.SELO0	CCU81.OUT10	CCU41.OUT3							USIC1_CH0.DX0E			USIC1_CH1.DX2A		ERU1.1A3
P3.4	BCCU0.OUT6	USIC1_CH0.DOUT0	USIC1_CH0.SCLKOUT	LEDTS2.COL3	CCU80.OUT01	USIC1_CH1.MCLKOUT	USIC1_CH1.SELO1	CCU81.OUT01								USIC1_CH0.DX0F	USIC1_CH0.DX1E		USIC1_CH1.DX2B		ERU1.2A3
P4.0	BCCU0.OUT0	ERU1.PDOUT0	LEDTS2.COL5	ERU1.GOUT0	CCU40.OUT0	ACMP1.OUT	USIC1_CH1.SELO1	CCU81.OUT10	CCU41.OUT0		CCU40.IN0BA	CCU41.IN0AC	CCU80.IN0AU			USIC1_CH0.DX3D	USIC1_CH0.DX4D				
P4.1	BCCU0.OUT8	ERU1.PDOUT1	LEDTS2.COL4	ERU1.GOUT1	CCU40.OUT1	ACMP3.OUT	USIC1_CH1.SELO2	CCU81.OUT11	CCU41.OUT1		CCU40.IN1BA	CCU41.IN1AC	CCU80.IN1AU		POSIF1.IN0B	USIC1_CH0.DX5C					
P4.2	BCCU0.OUT4	ERU1.PDOUT2	CCU81.OUT20	ERU1.GOUT2	CCU40.OUT2	ACMP2.OUT	USIC1_CH1.SELO3	CCU81.OUT12	CCU41.OUT2		CCU40.IN2BA	CCU41.IN2AC	CCU80.IN2AU	CCU81.IN1AB	POSIF1.IN1B	USIC1_CH0.DX5D					
P4.3	BCCU0.OUT5	ERU1.PDOUT3	CCU81.OUT21	ERU1.GOUT3	CCU40.OUT3	ACMP0.OUT	USIC1_CH0.SCLKOUT	CCU81.OUT13	CCU41.OUT3		CCU40.IN3BA	CCU41.IN3AC	CCU80.IN3AU		POSIF1.IN2B		USIC1_CH0.DX1B				
P4.4	BCCU0.OUT0	LEDTS2.LINE0		LEDTS1.COLA	CCU80.OUT00	USIC1_CH0.DOUT0		CCU81.OUT00	CCU41.OUT0			CCU41.IN0AV				USIC1_CH0.DX0C		USIC1_CH1.DX5F			ERU1.0A2
P4.5	BCCU0.OUT8	LEDTS2.LINE1		LEDTS1.COL6	CCU80.OUT01	USIC1_CH0.DOUT0	USIC1_CH0.SCLKOUT	CCU81.OUT01	CCU41.OUT1			CCU41.IN1AV				USIC1_CH0.DX0D	USIC1_CH0.DX1C				ERU1.1A2
P4.6	BCCU0.OUT2	LEDTS2.LINE2	CCU81.OUT10	LEDTS1.COL5	CCU80.OUT10		USIC1_CH0.SCLKOUT	CCU81.OUT02	CCU41.OUT2			CCU41.IN2AV		CCU81.IN0AB			USIC1_CH0.DX1D				ERU1.2A2
P4.7	BCCU0.OUT5	LEDTS2.LINE3	CCU81.OUT11	LEDTS1.COL4	CCU80.OUT11		USIC1_CH0.SELO0	CCU81.OUT03	CCU41.OUT3			CCU41.IN3AV					USIC1_CH0.DX2A				ERU1.0A3
P4.8	BCCU0.OUT7	LEDTS2.LINE4	LEDTS2.COL3	LEDTS1.COL3	CCU80.OUT30	CCU40.OUT0	USIC1_CH0.SELO1	CCU81.OUT30	CAN.N1_TXD		CCU40.IN0AV	CCU41.IN0BA					USIC1_CH0.DX2B			CAN.N1_RXDC	
P4.9	BCCU0.OUT3	LEDTS2.LINE5	LEDTS2.COL2	LEDTS1.COL2	CCU80.OUT31	CCU40.OUT1	USIC1_CH0.SELO2	CCU81.OUT31	CAN.N1_TXD		CCU40.IN1AV	CCU41.IN1BA					USIC1_CH0.DX2C			CAN.N1_RXDD	

Table 10 Hardware I/O Controlled Functions

Function	Outputs	Outputs	Inputs	Inputs	Pull Control	Pull Control	Pull Control	Pull Control
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P4.4	LEDTS2. EXTENDED0		LEDTS2.TSIN0	LEDTS2.TSIN0	Reserved for LEDTS Scheme A: pull-down disabled always	Reserved for LEDTS Scheme A: pull-down enabled always	Reserved for LEDTS Scheme B: pull-up enabled and pull-down disabled, and vice versa	
P4.5	LEDTS2. EXTENDED1		LEDTS2.TSIN1	LEDTS2.TSIN1				
P4.6	LEDTS2. EXTENDED2		LEDTS2.TSIN2	LEDTS2.TSIN2				
P4.7	LEDTS2. EXTENDED3		LEDTS2.TSIN3	LEDTS2.TSIN3				
P4.8	LEDTS2. EXTENDED4		LEDTS2.TSIN4	LEDTS2.TSIN4				
P4.9	LEDTS2. EXTENDED5		LEDTS2.TSIN5	LEDTS2.TSIN5				
P4.10	LEDTS2. EXTENDED6		LEDTS2.TSIN6	LEDTS2.TSIN6				
P4.11	LEDTS2. EXTENDED7		LEDTS2.TSIN7	LEDTS2.TSIN7				

Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input Hysteresis on port pin P2.3 - P2.9[8]	HYS_P2	CC	0.08 × V_{DDP}	–	V	CMOS Mode (5 V), Standard Hysteresis
			0.03 × V_{DDP}	–	V	CMOS Mode (3.3 V), Standard Hysteresis
			0.02 × V_{DDP}	–	V	CMOS Mode (2.2 V), Standard Hysteresis
			0.35 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode(5 V), Large Hysteresis
			0.25 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode(3.3 V), Large Hysteresis
			0.15 × V_{DDP}	0.65 × V_{DDP}	V	CMOS Mode(2.2 V), Large Hysteresis
Pin capacitance (digital inputs/outputs)	C_{IO}	CC	–	10	pF	
Pull-up current on port pins	I_{PUP}	CC	–	-80	µA	$V_{IH,min}$ (5 V)
			-95	–	µA	$V_{IL,max}$ (5 V)
			–	-50	µA	$V_{IH,min}$ (3.3 V)
			-65	–	µA	$V_{IL,max}$ (3.3 V)
Pull-down current on port pins	I_{PDP}	CC	–	40	µA	$V_{IL,max}$ (5 V)
			95	–	µA	$V_{IH,min}$ (5 V)
			–	30	µA	$V_{IL,max}$ (3.3 V)
			60	–	µA	$V_{IH,min}$ (3.3 V)
Input leakage current except P0.11[9]	I_{OZP}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105$ °C
Input leakage current for P0.11[9]	I_{OZP1}	CC	-10	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105$ °C
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	[10]
Maximum current per pin (excluding P1, V_{DDP} and V_{SS})	I_{MP}	SR	-10	11	mA	–
Maximum current per high currrent pins	I_{MP1A}	SR	-10	50	mA	–

Table 17 ADC Characteristics (Operating Conditions apply)[1)] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain settings	G_{IN} CC		1		–	GNCTRxz.GAINy = 00_B (unity gain)
			3		–	GNCTRxz.GAINy = 01_B (gain g1)
			6		–	GNCTRxz.GAINy = 10_B (gain g2)
			12		–	GNCTRxz.GAINy = 11_B (gain g3)
Sample Time	t_{sample} CC	5	–	–	1 / f_{ADC}	V_{DD} = 5.0 V, f_{ADCI} = 48 MHz
		3	–	–	1 / f_{ADC}	V_{DD} = 5.0 V, f_{ADCI} = 32 MHz
		3	–	–	1 / f_{ADC}	V_{DD} = 3.3 V, f_{ADCI} = 32 MHz
		30	–	–	1 / f_{ADC}	V_{DD} = 2.0 V, f_{ADCI} = 32 MHz
Conversion time in fast compare mode	t_{CF} CC		9		1 / f_{ADC}	3)
Conversion time in 12-bit mode	t_{C12} CC		20		1 / f_{ADC}	3)
Maximum sample rate in 12-bit mode[4)]	f_{C12} CC	–	–	f_{ADC} / 42.5	–	1 sample pending
		–	–	f_{ADC} / 62.5	–	2 samples pending
Conversion time in 10-bit mode	t_{C10} CC		18		1 / f_{ADC}	3)
Maximum sample rate in 10-bit mode[4)]	f_{C10} CC	–	–	f_{ADC} / 40.5	–	1 sample pending
		–	–	f_{ADC} / 58.5	–	2 samples pending
Conversion time in 8-bit mode	t_{C8} CC		16		1 / f_{ADC}	3)

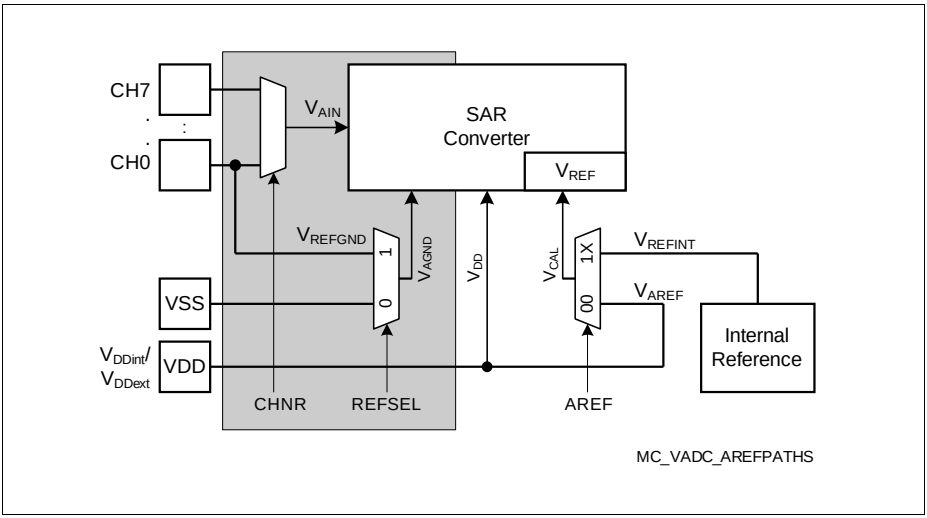

Figure 12 ADC Voltage Supply

3.2.6 Oscillator Pins

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The oscillator pins can be operated with an external crystal/resonator (see **Figure 15**) or in direct input mode (see **Figure 16**).

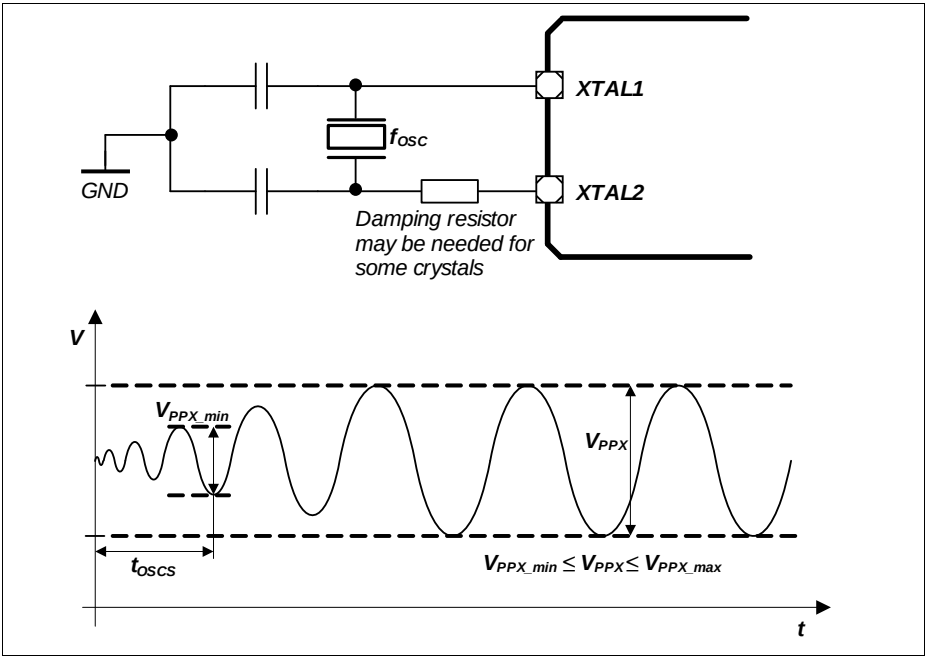

Figure 15 Oscillator in Crystal Mode

Table 23 Power Supply parameter table; V_{DDP} = 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.[1]	Max.		
Sleep mode current Peripherals clock disabled Flash active f_{MCLK} / f_{PCLK} in MHz[5]	I_{DDPSD} CC	–	2.8	–	mA	48 / 96
		–	2.2	–	mA	24 / 48
		–	2.0	–	mA	16 / 32
		–	1.9	–	mA	8 / 16
		–	1.7	–	mA	1 / 1
Sleep mode current Peripherals clock disabled Flash powered down f_{MCLK} / f_{PCLK} in MHz[6]	I_{DDPSR} CC	–	2.2	–	mA	48 / 96
		–	1.7	–	mA	24 / 48
		–	1.4	–	mA	16 / 32
		–	1.2	–	mA	8 / 16
		–	1.1	–	mA	1 / 1
Deep Sleep mode current[7]	I_{DDPDS} CC	–	0.27	–	mA	
Wake-up time from Sleep to Active mode[8]	t_{SSA} CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode[9]	t_{DSA} CC	–	290	–	µsec	

1) The typical values are measured at T_A = + 25 °C and V_{DDP} = 5 V.
2) CPU and all peripherals clock enabled, Flash is in active mode.
3) CPU enabled, all peripherals clock disabled, Flash is in active mode.
4) CPU in sleep, all peripherals clock enabled and Flash is in active mode.
5) CPU in sleep, Flash is in active mode.
6) CPU in sleep, Flash is powered down and code executed from RAM after wake-up.
7) CPU in sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.
8) CPU in sleep, Flash is in active mode during sleep mode.
9) CPU in sleep, Flash is in powered down mode during deep sleep mode.

3.3.2 Power-Up and Supply Threshold Characteristics

Table 26 provides the characteristics of the supply threshold in XMC1400.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DDP} is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 26 Power-Up and Supply Threshold Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} ramp-up time	t_{RAMPUP} SR	V_{DDP}/ $S_{VDDPrise}$	–	10^7	µs	
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	V/µs	Slope during normal operation
	S_{VDDP10} SR	0	–	10	V/µs	Slope during fast transient within +/-10% of V_{DDP}
	$S_{VDDPrise}$ SR	0	–	10	V/µs	Slope during power-on or restart after brownout event
	$S_{VDDPfall}$[1] SR	0	–	0.25	V/µs	Slope during supply falling out of the +/-10% limits[2]
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00_B
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01_B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10_B

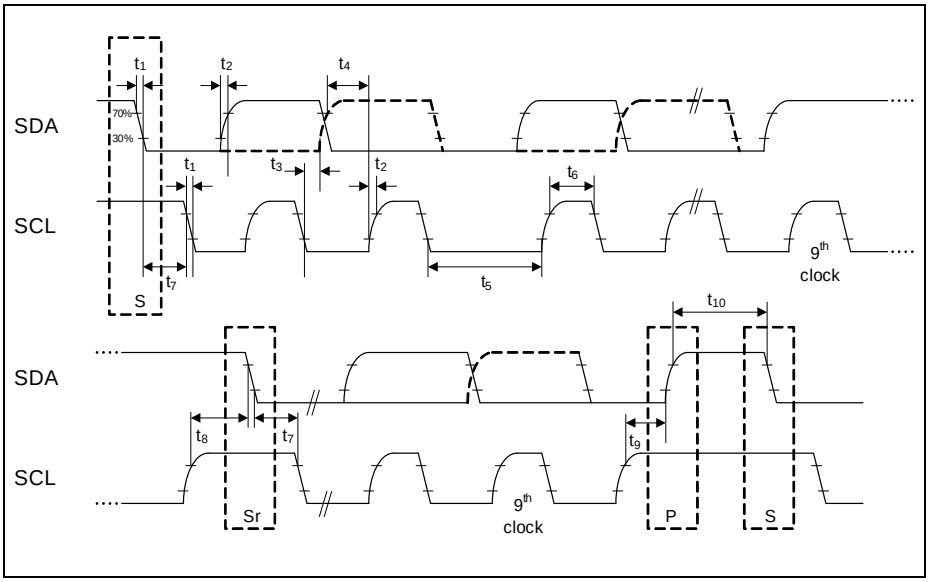

Figure 26 USIC IIC Timing

3.3.6.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: Operating Conditions apply.

Table 35 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	t_2 CC	0.35 x t_{1min}	-	-	ns	
Clock Low	t_3 CC	0.35 x t_{1min}	-	-	ns	
Hold time	t_4 CC	0	-	-	ns	
Clock rise time	t_5 CC	-	-	0.15 x t_{1min}	ns	

4 Package and Reliability

The XMC1400 is a member of the XMC1000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 37 provides the thermal characteristics of the packages used in XMC1400.

Table 37 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	3.7 × 3.7	mm	PG-VQFN-40-17
		-	4.2 × 4.2	mm	PG-VQFN-48-73
		-	4.6 × 4.6	mm	PG-VQFN-64-6
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	86.0	K/W	PG-TSSOP-38-9[1)]
		-	45.3	K/W	PG-VQFN-40-17[1)]
		-	44.9	K/W	PG-VQFN-48-73[1)]
		-	66.7	K/W	PG-LQFP-64-26[1)]
		-	44.7	K/W	PG-VQFN-64-6[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SSP}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC1400 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.