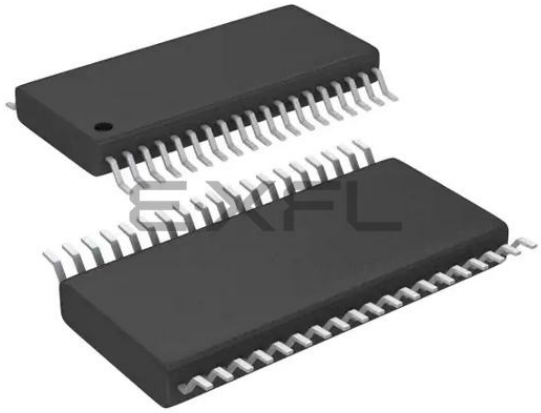
Infineon Technologies - XMC1402T038X0064AAXUMA1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38-9
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1402t038x0064aaxuma1

XMC1400 AA-Step

Microcontroller Series
for Industrial Applications

XMC1000 Family

ARM® Cortex®-M0
32-bit processor core

Data Sheet

V1.3 2016-10

Microcontrollers

Features

CPU subsystem

- 32-bit ARM Cortex-M0 CPU Core
  - 0.84 DMIPS/MHz (Dhrystone 2.1) at 48 MHz
- Nested Vectored Interrupt Controller
- 64 interrupt nodes
- MATH coprocessor
  - 24-bit trigonometric calculation (CORDIC)
  - 32-bit divide operation
- 2x4 channels ERU for event interconnections

On-Chip Memories

- 8 Kbyte ROM
- 16 Kbyte SRAM (with parity)
- up to 200 Kbyte Flash (with ECC)

Supply, Reset and Clock

- 1.8 V to 5.5 V supply with power on reset and brownout detector
- On-chip clock monitor
- External crystal oscillator support (32 kHz and 4 to 20 MHz)
- Internal slow and fast oscillators without the need of PLL

System Control

- Window watchdog
- Real time clock module
- Pseudo random number generator

Communication Peripherals

- Four USIC channels, usable as
  - UART (up to 12 Mb/s)
  - single-SPI (up to 12 Mb/s)
  - double-SPI (up to 2 × 12 Mb/s)
  - quad-SPI (up to 4 × 12 Mb/s)
  - IIC (up to 400 kb/s)
  - IIS (up to 12 Mb/s)
  - LIN interfaces (20kb/s)
- LEDTS in Human-Machine interface
  - up to 24 touch pads
  - drive up to 144 LEDs
- MultiCAN+, Full-CAN/Basic-CAN with 2 nodes, 32 message objects (up to 1 MBaud)

Analog Frontend Peripherals

- A/D Converters (up to 12 analog inputs)
  - 2 sample and hold stages
  - fast 12-bit ADC (up to 1.1 MS/s), adjustable gain
  - 0 V to 5.5 V input range
- Up to 8 channels out of range comparators
- Up to 4 fast analog comparators
- Temperature Sensor

Industrial Control Peripherals

- 2x4 16-bit 96 MHz CCU4 timers for signal monitoring and PWM
- 2x4 16-bit 96 MHz CCU8 timers for complex PWM, complementary high/low side switches and multi phase control
- 2x POSIF for hall and quadrature encoders, motor positioning
- 9 channel BCCU (brightness and color control) for LED lighting applications

Up to 56 Input/Output Ports

- 1.8 V to 5.5 V capable
- up to 8 high current pads (50 mA sink)

On-Chip Debug Support

- 4 breakpoints, 2 watchpoints
- ARM serial wire debug, single-pin debug interfaces

Programming Support

- Single-pin bootloader
- Secure bootstrap loader SBSL (optional)

Packages

- TSSOP-38 (9.7 × 6.4 mm^2)
- VQFN-40/48/64 (5×5/7×7/8×8 mm^2)
- LQFP-64 (12 × 12 mm^2)

Tools

- Free DAVE™ toolchain with low level drivers and apps

1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is an 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location : 1000 $0F00_H$ (MSB) - 1000 $0F1B_H$ (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

Table 3 XMC1400 Chip Identification Number

Derivative	Value	Marking
XMC1401-Q048F0064	00014082 07CF00FF 1E071FF7 20006000 00000D00 00001000 00011000 10204083_H	AA
XMC1401-Q048F0128	00014082 07CF00FF 1E071FF7 20006000 00000D00 00001000 00021000 10204083_H	AA
XMC1401-F064F0064	000140A2 07CF00FF 1E071FF7 20006000 00000D00 00001000 00011000 10204083_H	AA
XMC1401-F064F0128	000140A2 07CF00FF 1E071FF7 20006000 00000D00 00001000 00021000 10204083_H	AA
XMC1402-T038X0032	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00009000 10204083_H	AA
XMC1402-T038X0064	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00011000 10204083_H	AA
XMC1402-T038X0128	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00021000 10204083_H	AA
XMC1402-T038X0200	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00033000 10204083_H	AA
XMC1402-Q040X0032	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00009000 10204083_H	AA
XMC1402-Q040X0064	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00011000 10204083_H	AA
XMC1402-Q040X0128	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00021000 10204083_H	AA
XMC1402-Q040X0200	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00033000 10204083_H	AA
XMC1402-Q048X0032	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00009000 10204083_H	AA

2.2.3 Port I/O Function Description

The following general building block is used to describe the I/O functions of each PORT pin:

Table 7 Port I/O Function Description

Function	Outputs		Inputs	
	ALT1	ALTn	Input	Input
P0.0		MODA.OUT	MODC.INA	
Pn.y	MODA.OUT		MODA.INA	MODC.INB

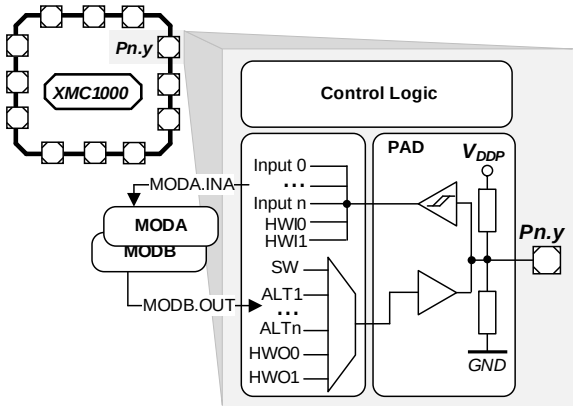


Figure 10 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to nine alternate output functions (ALT1 to ALT9) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

Please refer to the **Port I/O Functions** table for the complete Port I/O function mapping.

2.2.4 Hardware Controlled I/O Function Description

The following general building block is used to describe the hardware I/O and pull control functions of each PORT pin:

Table 8 Hardware Controlled I/O Function Description

Function	Outputs	Inputs	Pull Control	
	HWO0	**HWI0**	**HW0_PD**	**HW0_PU**
P0.0	MODB.OUT	MODB.INA		
Pn.y			$\overline{\text{MODC.OUT}}$	MODC.OUT

By Pn_HWSEL, it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers. Additional hardware signals HW0_PD/HW1_PD and HW0_PU/HW1_PU controlled by the peripherals can be used to control the pull devices of the pin.

Please refer to the **Hardware Controlled I/O Functions** table for the complete hardware I/O and pull control function mapping.

Port I/O Function Table

Table 9 Port I/O Functions

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0.PDOUT0	LEDTS0.LINE7	ERU0.GOUT0	CCU40.OUT0	CCU80.OUT00	USIC0_CH0.SELO0	USIC0_CH1.SELO0	CCU81.OUT00	USIC1_CH1.DOUT0	BCCU0.TRAPINB	CCU40.IN0AC					USIC1_CH1.DX0A	USIC0_CH0.DX2A		USIC0_CH1.DX2A		
P0.1	ERU0.PDOUT1	LEDTS0.LINE6	ERU0.GOUT1	CCU40.OUT1	CCU80.OUT01	BCCU0.OUT8	SCU.VDROP	USIC1_CH1.SCLKOUT	USIC1_CH1.DOUT0		CCU40.IN1AC					USIC1_CH1.DX0B	USIC1_CH1.DX1A				
P0.2	ERU0.PDOUT2	LEDTS0.LINE5	ERU0.GOUT2	CCU40.OUT2	CCU80.OUT02	VADC0.EMUX02	CCU80.OUT10	USIC1_CH0.SCLKOUT	USIC1_CH0.DOUT0		CCU40.IN2AC					USIC1_CH0.DX0A	USIC1_CH0.DX1A				
P0.3	ERU0.PDOUT3	LEDTS0.LINE4	ERU0.GOUT3	CCU40.OUT3	CCU80.OUT03	VADC0.EMUX01	CCU80.OUT11	USIC1_CH1.SCLKOUT	USIC1_CH0.DOUT0		CCU40.IN3AC					USIC1_CH0.DX0B					
P0.4	BCCU0.OUT0	LEDTS0.LINE3	LEDTS0.COL3	CCU40.OUT1	CCU80.OUT13	VADC0.EMUX00	WWDT.SERVICE_OUT	USIC1_CH1.SELO0	CAN.N0_TXD			CCU41.IN0AB	CCU80.IN0AB							CAN.N0_RXDA	
P0.5	BCCU0.OUT1	LEDTS0.LINE2	LEDTS0.COL2	CCU40.OUT0	CCU80.OUT12	ACMP2.OUT	CCU80.OUT01	VADC0.EMUX10	CAN.N0_TXD			CCU41.IN1AB	CCU80.IN1AB							CAN.N0_RXDB	
P0.6	BCCU0.OUT2	LEDTS0.LINE1	LEDTS0.COL1	CCU40.OUT0	CCU80.OUT11	USIC0_CH1.MCLKOUT	USIC0_CH1.DOUT0	VADC0.EMUX11	CCU41.OUT0		CCU40.IN0AB	CCU41.IN2AB						USIC0_CH1.DX0C			
P0.7	BCCU0.OUT3	LEDTS0.LINE0	LEDTS0.COL0	CCU40.OUT1	CCU80.OUT10	USIC0_CH0.SCLKOUT	USIC0_CH1.DOUT0	VADC0.EMUX12	CCU41.OUT1		CCU40.IN1AB	CCU41.IN3AB					USIC0_CH0.DX1C	USIC0_CH1.DX0D	USIC0_CH1.DX1C		
P0.8/ RTC_XTAL1	BCCU0.OUT4	LEDTS1.LINE0	LEDTS0.COLA	CCU40.OUT2	CCU80.OUT20	USIC0_CH0.SCLKOUT	USIC0_CH1.SCLKOUT	CCU81.OUT20	CCU41.OUT2		CCU40.IN2AB						USIC0_CH0.DX1B		USIC0_CH1.DX1B		
P0.9/ RTC_XTAL2	BCCU0.OUT5	LEDTS1.LINE1	LEDTS0.COL6	CCU40.OUT3	CCU80.OUT21	USIC0_CH0.SELO0	USIC0_CH1.SELO0	CCU81.OUT21	CCU41.OUT3		CCU40.IN3AB						USIC0_CH0.DX2B		USIC0_CH1.DX2B		
P0.10/ XTAL1	BCCU0.OUT6	LEDTS1.LINE2	LEDTS0.COL5	ACMP0.OUT	CCU80.OUT22	USIC0_CH0.SELO1	USIC0_CH1.SELO1	CCU81.OUT22					CCU80.IN2AB	CCU81.IN2AB			USIC0_CH0.DX2C		USIC0_CH1.DX2C		
P0.11/ XTAL2	BCCU0.OUT7	LEDTS1.LINE3	LEDTS0.COL4	USIC0_CH0.MCLKOUT	CCU80.OUT23	USIC0_CH0.SELO2	USIC0_CH1.SELO2	CCU81.OUT23									USIC0_CH0.DX2D		USIC0_CH1.DX2D		
P0.12	BCCU0.OUT6	LEDTS1.LINE4	LEDTS0.COL3	LEDTS1.COL3	CCU80.OUT33	USIC0_CH0.SELO3	CCU80.OUT20		CAN.N1_TXD	BCCU0.TRAPINA	CCU40.IN0AA	CCU40.IN1AA	CCU40.IN2AA	CCU81.IN0AU	CCU40.IN3AA	CCU80.IN0AA	USIC0_CH0.DX2E	CCU80.IN1AA	CCU80.IN2AA	CAN.N1_RXDA	CCU80.IN3AA

Table 9 Port I/O Functions (cont'd)

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P0.13	WWDT.SERVICE_OUT	LEDTS1.LINE5	LEDTS0.COL2	LEDTS1.COL2	CCU80.OUT32	USIC0_CH0.SELO4	CCU80.OUT21		CAN.N1_TXD				CCU80.IN3AB	CCU81.IN1AU	POSIF0.IN0B		USIC0_CH0.DX2F			CAN.N1_RXDB	
P0.14	BCCU0.OUT7	LEDTS1.LINE6	LEDTS0.COL1	LEDTS1.COL1	CCU80.OUT31	USIC0_CH0.DOUT0	USIC0_CH0.SCLKOUT		CAN.N0_TXD					CCU81.IN2AU	POSIF0.IN1B	USIC0_CH0.DX0A	USIC0_CH0.DX1A	USIC1_CH1.DX5B		CAN.N0_RXDC	
P0.15	BCCU0.OUT8	LEDTS1.LINE7	LEDTS0.COL0	LEDTS1.COL0	CCU80.OUT30	USIC0_CH0.DOUT0	USIC0_CH1.MCLKOUT		CAN.N0_TXD					CCU81.IN3AU	POSIF0.IN2B	USIC0_CH0.DX0B		USIC1_CH1.DX3B	USIC1_CH1.DX4B	CAN.N0_RXDD	
P1.0	BCCU0.OUT0	CCU40.OUT0	LEDTS0.COL0	LEDTS1.COLA	CCU80.OUT00	ACMP1.OUT	USIC0_CH0.DOUT0	CCU81.OUT00	CAN.N0_TXD						POSIF0.IN2A	USIC0_CH0.DX0C				CAN.N0_RXDG	
P1.1	ERU1.PDOUT1	CCU40.OUT1	LEDTS0.COL1	LEDTS1.COL0	CCU80.OUT01	USIC0_CH0.DOUT0	USIC0_CH1.SELO0	CCU81.OUT01	CAN.N0_TXD						POSIF0.IN1A	USIC0_CH0.DX0D	USIC0_CH0.DX1D		USIC0_CH1.DX2E	CAN.N0_RXDH	
P1.2	ERU1.PDOUT2	CCU40.OUT2	LEDTS0.COL2	LEDTS1.COL1	CCU80.OUT10	ACMP2.OUT	USIC0_CH1.DOUT0	CCU81.OUT10	CAN.N1_TXD						POSIF0.IN0A			USIC0_CH1.DX0B		CAN.N1_RXDG	
P1.3	ERU1.PDOUT3	CCU40.OUT3	LEDTS0.COL3	LEDTS1.COL2	CCU80.OUT11	USIC0_CH1.SCLKOUT	USIC0_CH1.DOUT0	CCU81.OUT11	CAN.N1_TXD									USIC0_CH1.DX0A	USIC0_CH1.DX1A	CAN.N1_RXDH	
P1.4	ERU1.PDOUT0	USIC0_CH1.SCLKOUT	LEDTS0.COL4	LEDTS1.COL3	CCU80.OUT20	USIC0_CH0.SELO0	USIC0_CH1.SELO1	CCU81.OUT20	CCU41.OUT0							USIC0_CH0.DX5E		USIC0_CH1.DX5E			
P1.5	ERU1.PDOUT1	USIC0_CH0.DOUT0	LEDTS0.COLA	BCCU0.OUT1	CCU80.OUT21	USIC0_CH0.SELO1	USIC0_CH1.SELO2	CCU81.OUT21	CCU41.OUT1									USIC0_CH1.DX5F			
P1.6	ERU1.PDOUT2	USIC0_CH1.DOUT0	LEDTS0.COL5	USIC0_CH0.SCLKOUT	BCCU0.OUT2	USIC0_CH0.SELO2	USIC0_CH1.SELO3	CCU81.OUT30	CCU41.OUT2						POSIF1.IN2A	USIC0_CH0.DX5F					
P1.7	BCCU0.OUT8	CCU40.OUT3	LEDTS0.COL6	LEDTS1.COL4		ACMP3.OUT	ERU1.PDOUT3	CCU81.OUT31	CCU41.OUT3						POSIF1.IN1A	USIC1_CH0.DX5B			USIC1_CH1.DX2C		
P1.8	BCCU0.OUT0	CCU40.OUT0	USIC1_CH1.SCLKOUT	VADC0.EMUX02		ACMP1.OUT	ERU1.PDOUT0	CCU81.OUT32							POSIF1.IN0A	USIC1_CH0.DX3B	USIC1_CH0.DX4B		USIC1_CH1.DX1C		
P2.0	ERU0.PDOUT3	CCU40.OUT0	ERU0.GOUT3	LEDTS1.COL5	CCU80.OUT20	USIC0_CH0.DOUT0	USIC0_CH0.SCLKOUT	CCU81.OUT20	CAN.N0_TXD		VADC0.G0CH5					USIC0_CH0.DX0E	USIC0_CH0.DX1E		USIC0_CH1.DX2F	CAN.N0_RXDE	ERU0.0B0
P2.1	ERU0.PDOUT2	CCU40.OUT1	ERU0.GOUT2	LEDTS1.COL6	CCU80.OUT21	USIC0_CH0.DOUT0	USIC0_CH1.SCLKOUT	CCU81.OUT21	CAN.N0_TXD	ACMP2.INP	VADC0.G0CH6					USIC0_CH0.DX0F		USIC0_CH1.DX3A	USIC0_CH1.DX4A	CAN.N0_RXDF	ERU0.1B0

Table 9 Port I/O Functions (cont'd)

Function	Outputs									Inputs										
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P4.10		LEDTS2.LINE6	LEDTS2.COL1	LEDTS1.COL1	CCU80.OUT00	CCU40.OUT2	USIC1_CH0.SELO3	CCU81.OUT32	CCU81.OUT00	BCCU0.TRAPIND	CCU40.IN2AV	CCU41.IN2BA		CCU81.IN3AB			USIC1_CH0.DX2D	USIC1_CH1.DX5A			
P4.11		LEDTS2.LINE7	LEDTS2.COL0	LEDTS1.COL0	CCU80.OUT01	CCU40.OUT3	USIC1_CH0.SELO4	CCU81.OUT33	CCU81.OUT01		CCU40.IN3AV	CCU41.IN3BA					USIC1_CH0.DX2E	USIC1_CH1.DX3A	USIC1_CH1.DX4A		

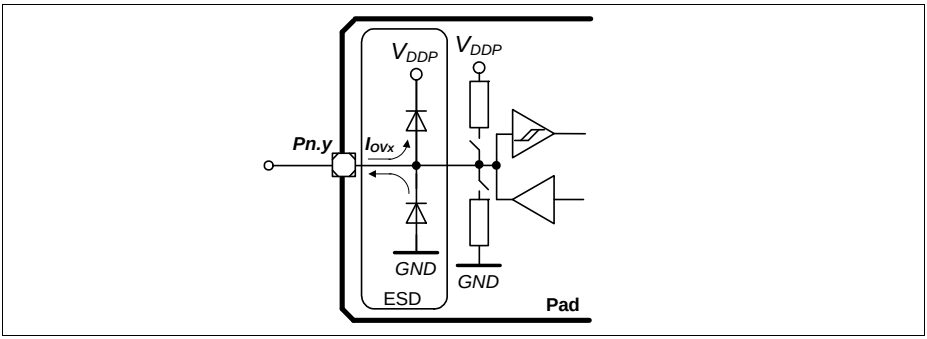


Figure 11 Input Overload Current via ESD structures

Table 13 and **Table 14** list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the **Absolute Maximum Ratings** must not be exceeded during overload.

Table 13 PN-Junction Characterisitics for positive Overload

Pad Type	I_{OV} = 5 mA
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{DDP} + 0.5$ V $V_{AIN} = V_{DDP} + 0.5$ V $V_{AREF} = V_{DDP} + 0.5$ V
P2.[1,2,6:9,11]	$V_{INP2} = V_{DDP} + 0.3$ V

Table 14 PN-Junction Characterisitics for negative Overload

Pad Type	I_{OV} = 5 mA
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{SS} - 0.5$ V $V_{AIN} = V_{SS} - 0.5$ V $V_{AREF} = V_{SS} - 0.5$ V
P2.[1,2,6:9,11]	$V_{INP2} = V_{SS} - 0.3$ V

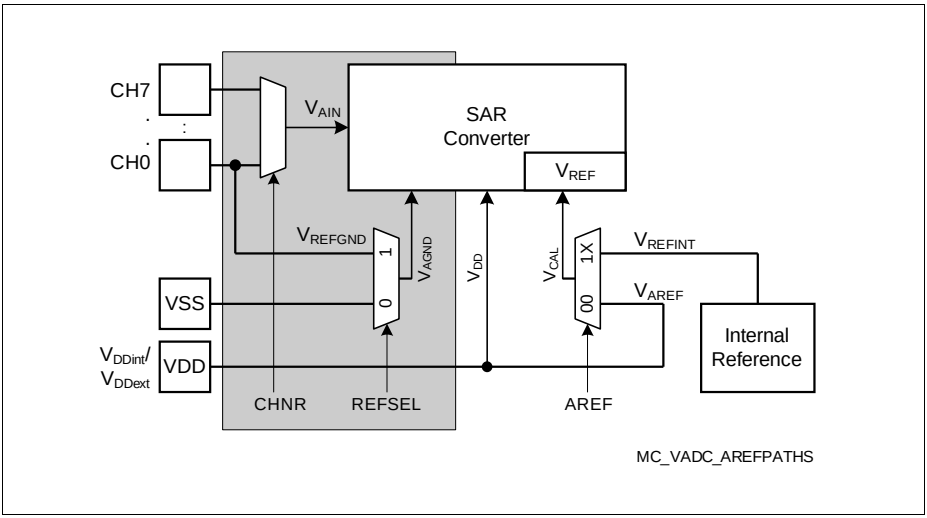


Figure 12 ADC Voltage Supply

Table 22 RTC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	–	32.768	–	kHz	
Oscillator start-up time[1)2)]	t_{OSCS} CC	–	–	5	s	
Input voltage at RTC_XTAL1	V_{IX} SR	-0.3	–	1.5	V	
Input amplitude (peak-to-peak) at RTC_XTAL1[2)3)]	V_{PPX} SR	0.2	–	1.2	V	

1) t_{OSCS} is defined from the moment the oscillator is enabled by the user with SCU_ANAOSCLPCTRL.MODE until the oscillations reach an amplitude at RTC_XTAL1 of 0.9 * V_{PPX}.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) If the shaper unit is enabled and not bypassed.

3.2.7 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 23 Power Supply parameter table; V_{DDP} = 5V

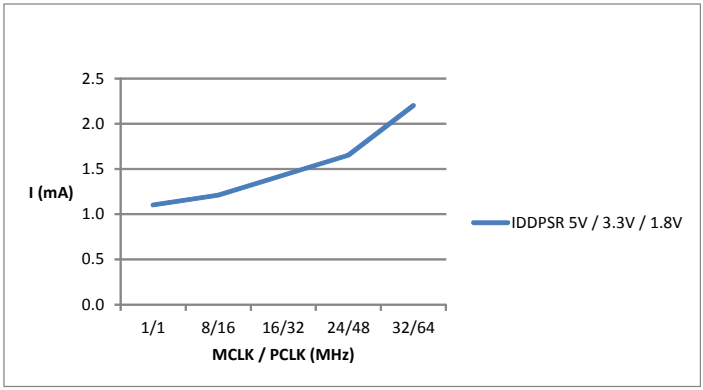
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.[1]	Max.		
Active mode current Peripherals enabled f_{MCLK} / f_{PCLK} in MHz[2]	I_{DDPAE} CC	–	14.1	20	mA	48 / 96
		–	9.8	–	mA	24 / 48
		–	7.8	–	mA	16 / 32
		–	6.4	–	mA	8 / 16
		–	4.4	–	mA	1 / 1
Active mode current Peripherals disabled f_{MCLK} / f_{PCLK} in MHz[3]	I_{DDPAD} CC	–	6.2		mA	48 / 96
		–	4.6	–	mA	24 / 48
		–	3.6	–	mA	16 / 32
		–	3.1	–	mA	8 / 16
		–	1.8	–	mA	1 / 1
Active mode current Code execution from RAM Flash is powered down f_{MCLK} / f_{PCLK} in MHz	I_{DDPAR} CC	–	9.6	–	mA	48 / 96
Sleep mode current Peripherals clock enabled f_{MCLK} / f_{PCLK} in MHz[4]	I_{DDPSE} CC	–	11.0	–	mA	48 / 96
		–	7.6	–	mA	24 / 48
		–	6.4	–	mA	16 / 32
		–	5.3	–	mA	8 / 16
		–	4.2	–	mA	1 / 1

Table 23 Power Supply parameter table; V_{DDP} = 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.[1]	Max.		
Sleep mode current Peripherals clock disabled Flash active f_{MCLK} / f_{PCLK} in MHz[5]	I_{DDPSD} CC	–	2.8	–	mA	48 / 96
		–	2.2	–	mA	24 / 48
		–	2.0	–	mA	16 / 32
		–	1.9	–	mA	8 / 16
		–	1.7	–	mA	1 / 1
Sleep mode current Peripherals clock disabled Flash powered down f_{MCLK} / f_{PCLK} in MHz[6]	I_{DDPSR} CC	–	2.2	–	mA	48 / 96
		–	1.7	–	mA	24 / 48
		–	1.4	–	mA	16 / 32
		–	1.2	–	mA	8 / 16
		–	1.1	–	mA	1 / 1
Deep Sleep mode current[7]	I_{DDPDS} CC	–	0.27	–	mA	
Wake-up time from Sleep to Active mode[8]	t_{SSA} CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode[9]	t_{DSA} CC	–	290	–	µsec	

1) The typical values are measured at T_A = + 25 °C and V_{DDP} = 5 V.
2) CPU and all peripherals clock enabled, Flash is in active mode.
3) CPU enabled, all peripherals clock disabled, Flash is in active mode.
4) CPU in sleep, all peripherals clock enabled and Flash is in active mode.
5) CPU in sleep, Flash is in active mode.
6) CPU in sleep, Flash is powered down and code executed from RAM after wake-up.
7) CPU in sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.
8) CPU in sleep, Flash is in active mode during sleep mode.
9) CPU in sleep, Flash is in powered down mode during deep sleep mode.

Figure 18 shows typical graphs for sleep mode current for V_{DDP} = 5 V, V_{DDP} = 3.3 V, V_{DDP} = 1.8 V across different clock frequencies.



Condition:
1. TA = +25° C

Figure 18 Sleep mode, peripherals clocks disabled, Flash powered down: Supply current I_{DDPSD} over supply voltage V_{DDP} for different clock frequencies

3.3.2 Power-Up and Supply Threshold Characteristics

Table 26 provides the characteristics of the supply threshold in XMC1400.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DDP} is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 26 Power-Up and Supply Threshold Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} ramp-up time	t_{RAMPUP} SR	V_{DDP}/ $S_{VDDPrise}$	–	10^7	µs	
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	V/µs	Slope during normal operation
	S_{VDDP10} SR	0	–	10	V/µs	Slope during fast transient within +/-10% of V_{DDP}
	$S_{VDDPrise}$ SR	0	–	10	V/µs	Slope during power-on or restart after brownout event
	$S_{VDDPfall}$[1] SR	0	–	0.25	V/µs	Slope during supply falling out of the +/-10% limits[2]
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00_B
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01_B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10_B

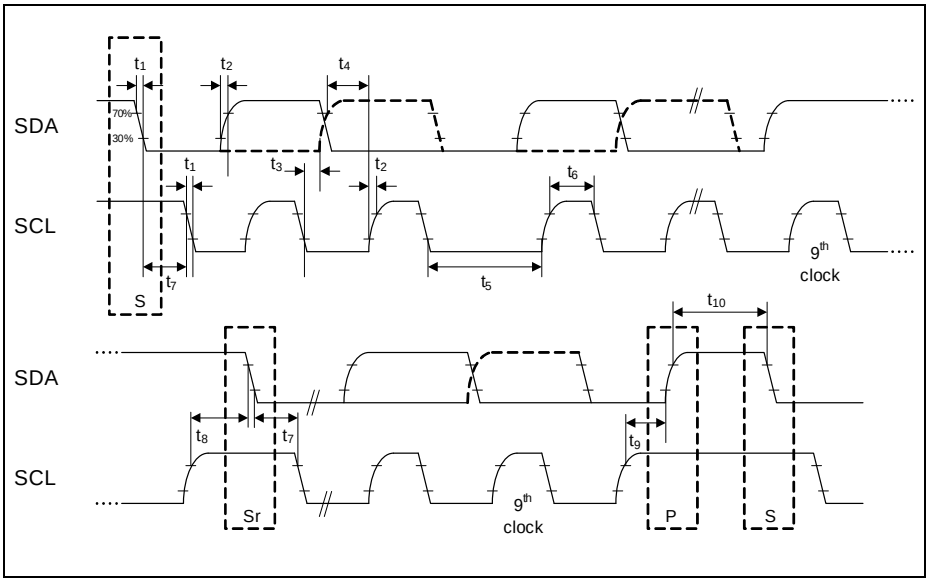


Figure 26 USIC IIC Timing

3.3.6.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: Operating Conditions apply.

Table 35 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	t_2 CC	0.35 x t_{1min}	-	-	ns	
Clock Low	t_3 CC	0.35 x t_{1min}	-	-	ns	
Hold time	t_4 CC	0	-	-	ns	
Clock rise time	t_5 CC	-	-	0.15 x t_{1min}	ns	

4 Package and Reliability

The XMC1400 is a member of the XMC1000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 37 provides the thermal characteristics of the packages used in XMC1400.

Table 37 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	3.7 × 3.7	mm	PG-VQFN-40-17
		-	4.2 × 4.2	mm	PG-VQFN-48-73
		-	4.6 × 4.6	mm	PG-VQFN-64-6
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	86.0	K/W	PG-TSSOP-38-9[1)]
		-	45.3	K/W	PG-VQFN-40-17[1)]
		-	44.9	K/W	PG-VQFN-48-73[1)]
		-	66.7	K/W	PG-LQFP-64-26[1)]
		-	44.7	K/W	PG-VQFN-64-6[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SSP}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC1400 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

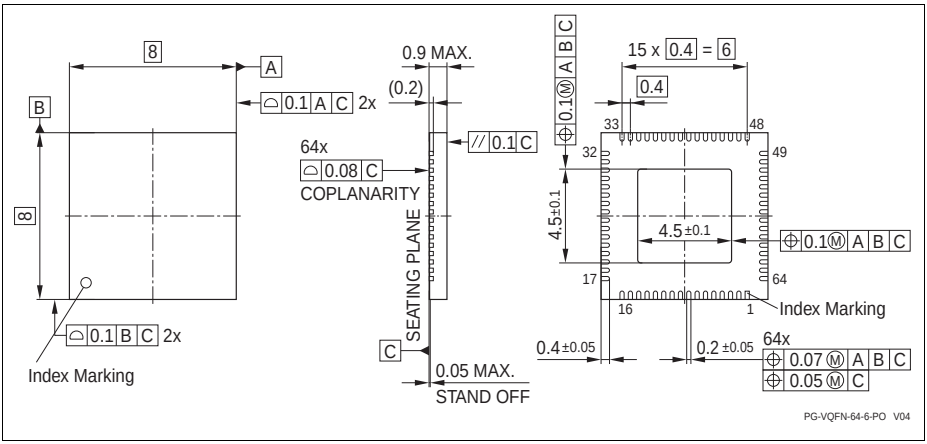


Figure 33 PG-VQFN-64-6

All dimensions in mm.

5 Quality Declaration

Table 38 shows the characteristics of the quality parameters in the XMC1400.

Table 38 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	-	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	*MSL* CC	-	3	-	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	-	260	°C	Profile according to JEDEC J-STD-020D

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