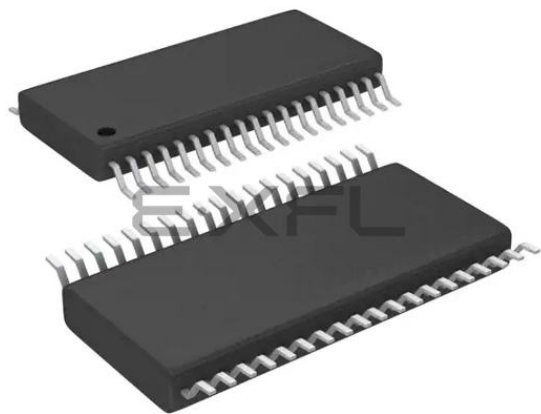




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	200KB (200K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38-9
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1402t038x0200aaxuma1

1 Summary of Features

The XMC1400 devices are members of the XMC1000 Family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1400 series addresses the real-time control needs of motor control and digital power conversion. It also features peripherals for LED Lighting applications and Human-Machine Interface (HMI).

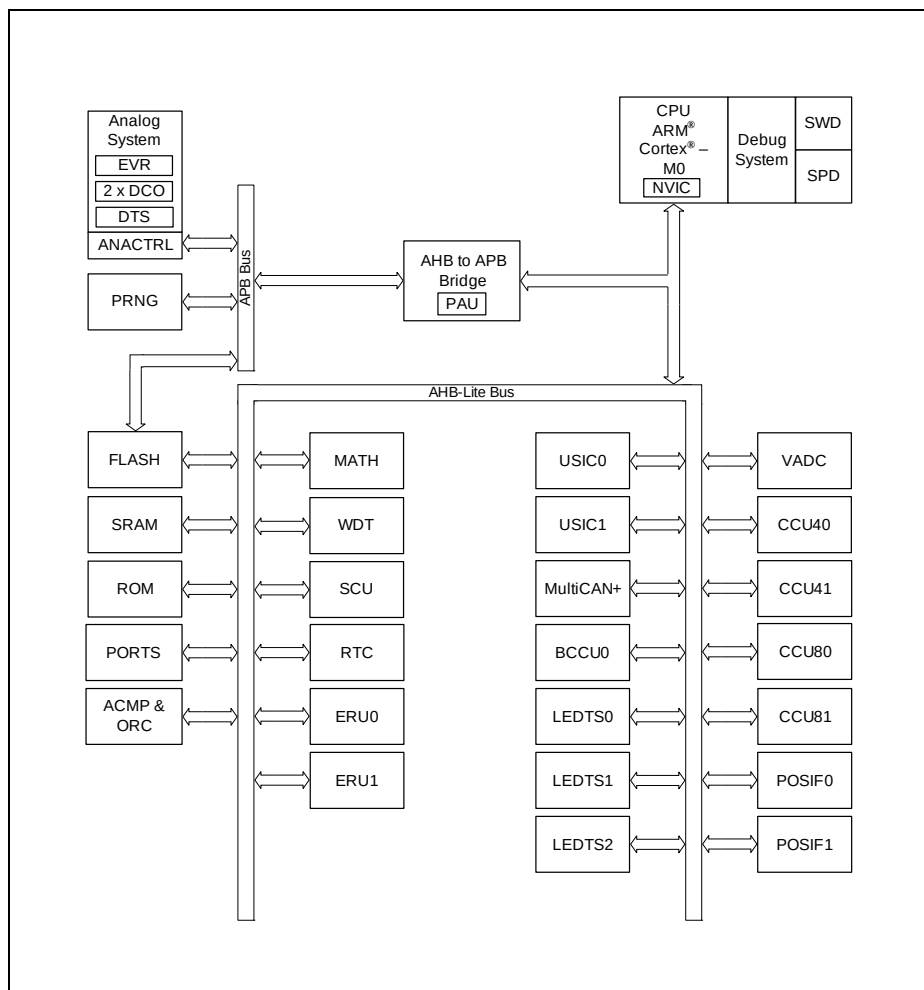


Figure 1 Block Diagram

1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is an 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location : 1000 0F00_H (MSB) - 1000 0F1B_H (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

Table 3 XMC1400 Chip Identification Number

Derivative	Value	Marking
XMC1401-Q048F0064	00014082 07CF00FF 1E071FF7 20006000 00000D00 00001000 00011000 10204083 _H	AA
XMC1401-Q048F0128	00014082 07CF00FF 1E071FF7 20006000 00000D00 00001000 00021000 10204083 _H	AA
XMC1401-F064F0064	000140A2 07CF00FF 1E071FF7 20006000 00000D00 00001000 00011000 10204083 _H	AA
XMC1401-F064F0128	000140A2 07CF00FF 1E071FF7 20006000 00000D00 00001000 00021000 10204083 _H	AA
XMC1402-T038X0032	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00009000 10204083 _H	AA
XMC1402-T038X0064	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00011000 10204083 _H	AA
XMC1402-T038X0128	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00021000 10204083 _H	AA
XMC1402-T038X0200	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00033000 10204083 _H	AA
XMC1402-Q040X0032	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00009000 10204083 _H	AA
XMC1402-Q040X0064	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00011000 10204083 _H	AA
XMC1402-Q040X0128	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00021000 10204083 _H	AA
XMC1402-Q040X0200	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00033000 10204083 _H	AA
XMC1402-Q048X0032	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00009000 10204083 _H	AA

Table 3 XMC1400 Chip Identification Number (cont'd)

Derivative	Value	Marking
XMC1403-Q064X0200	00014093 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00033000 10204083 _H	AA
XMC1404-Q048X0064	00014083 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00011000 10204083 _H	AA
XMC1404-Q048X0128	00014083 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00021000 10204083 _H	AA
XMC1404-Q048X0200	00014083 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00033000 10204083 _H	AA
XMC1404-Q064X0064	00014093 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00011000 10204083 _H	AA
XMC1404-Q064X0128	00014093 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00021000 10204083 _H	AA
XMC1404-Q064X0200	00014093 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00033000 10204083 _H	AA
XMC1404-F064X0064	000140A3 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00011000 10204083 _H	AA
XMC1404-F064X0128	000140A3 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00021000 10204083 _H	AA
XMC1404-F064X0200	000140A3 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00033000 10204083 _H	AA

General Device Information

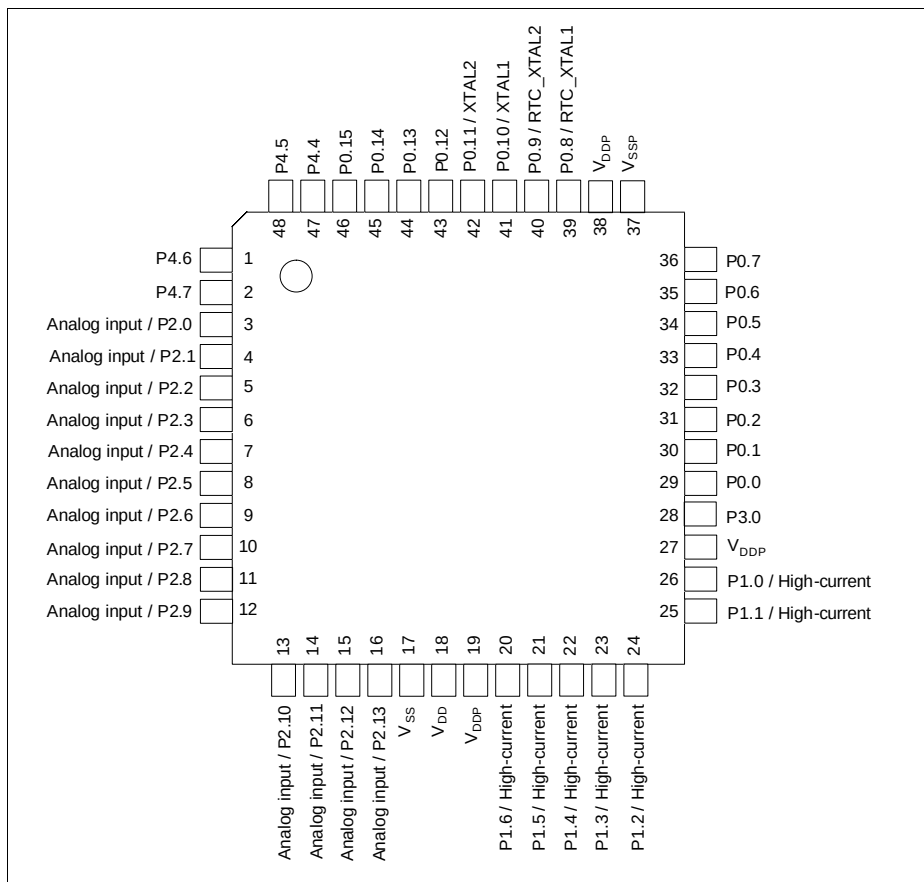


Figure 8 XMC1400 PG-VQFN-48-73 Pin Configuration (top view)

2.2.2 Port Pin for Boot Modes

Port functions can be overruled by the boot mode selected. The type of boot mode is selected via BMI. [Table 6](#) shows the port pins used for the various boot modes.

Table 6 Port Pin for Boot Modes

Pin	Boot	Boot Description
P0.13	CS(O)	SSC BSL mode
P0.14	SWDIO_0	Debug mode (SWD)
	SPD_0	Debug mode (SPD)
	RX/TX	ASC BSL half-duplex mode
	RX	ASC BSL full-duplex mode
	RX	CAN BSL mode
	SCLK(O)	SSC BSL mode
P0.15	SWDCLK_0	Debug mode (SWD)
	TX	ASC BSL full-duplex mode
	TX	CAN BSL mode
	DATA(I/O)	SSC BSL mode
P1.2	SWDCLK_1	Debug mode (SWD)
	TX	ASC BSL full-duplex mode
	TX	CAN BSL mode
P1.3	SWDIO_1	Debug mode (SWD)
	SPD_1	Debug mode (SPD)
	RX/TX	ASC BSL half-duplex mode
	RX	ASC BSL full-duplex mode
	RX	CAN BSL mode
P4.6	HWCON0	Boot Pins
P4.7	HWCON1	(Boot from pins mode must be selected)

Port I/O Function Table

Table 9 Port I/O Functions

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0.P DOUT0	LEDTS0 .LINE7	ERU0.G OUT0	CCU40. OUT0	CCU80. OUT00	USIC0_ CH0.SE LO0	USIC0_ CH1.SE LO0	CCU81. OUT00	USIC1_ CH1.DO UT0	BCCU0. TRAPIN B	CCU40.I N0AC					USIC1_ CH1.DX 0A	USIC0_ CH0.D X2A		USIC0_ CH1.DX 2A		
P0.1	ERU0.P DOUT1	LEDTS0 .LINE6	ERU0.G OUT1	CCU40. OUT1	CCU80. OUT01	BCCU0. OUT8	SCU.VD ROP	USIC1_ CH1.SC LKOUT	USIC1_ CH1.DO UT0		CCU40.I N1AC					USIC1_ CH1.DX 0B	USIC1_ CH1.D X1A				
P0.2	ERU0.P DOUT2	LEDTS0 .LINE5	ERU0.G OUT2	CCU40. OUT2	CCU80. OUT02	VADC0. EMUX02	CCU80. OUT10	USIC1_ CH0.SC LKOUT	USIC1_ CH0.DO UT0		CCU40.I N2AC					USIC1_ CH0.DX 0A	USIC1_ CH0.D X1A				
P0.3	ERU0.P DOUT3	LEDTS0 .LINE4	ERU0.G OUT3	CCU40. OUT3	CCU80. OUT03	VADC0. EMUX01	CCU80. OUT11	USIC1_ CH1.SC LKOUT	USIC1_ CH0.DO UT0		CCU40.I N3AC					USIC1_ CH0.DX 0B					
P0.4	BCCU0. OUT0	LEDTS0 .LINE3	LEDTS0 .COL3	CCU40. OUT1	CCU80. OUT13	VADC0. EMUX00	WWDT. SERVIC E_OUT	USIC1_ CH1.SE LO0	CAN.N0 _TXD			CCU41.I N0AB	CCU80.I N0AB							CAN.N0 _RXDA	
P0.5	BCCU0. OUT1	LEDTS0 .LINE2	LEDTS0 .COL2	CCU40. OUT0	CCU80. OUT12	ACMP2. OUT	CCU80. OUT01	VADC0. EMUX10	CAN.N0 _TXD			CCU41.I N1AB	CCU80.I N1AB							CAN.N0 _RXDB	
P0.6	BCCU0. OUT2	LEDTS0 .LINE1	LEDTS0 .COL1	CCU40. OUT0	CCU80. OUT11	USIC0_ CH1.MC LKOUT	USIC0_ CH1.DO UT0	VADC0. EMUX11	CCU41. OUT0		CCU40.I N0AB	CCU41.I N2AB						USIC0_ CH1.DX 0C			
P0.7	BCCU0. OUT3	LEDTS0 .LINE0	LEDTS0 .COL0	CCU40. OUT1	CCU80. OUT10	USIC0_ CH0.SC LKOUT	USIC0_ CH1.DO UT0	VADC0. EMUX12	CCU41. OUT1		CCU40.I N1AB	CCU41.I N3AB				USIC0_ CH0.D X1C	USIC0_ CH1.DX 0D	USIC0_ CH1.DX 1C			
P0.8/ RTC_XTAL1	BCCU0. OUT4	LEDTS1 .LINE0	LEDTS0 _OUT2	CCU40. OUT20	CCU80. OUT20	USIC0_ CH0.SC LKOUT	USIC0_ CH1.SC LKOUT	CCU81. OUT20	CCU41. OUT2		CCU40.I N2AB					USIC0_ CH0.D X1B		USIC0_ CH1.DX 1B			
P0.9/ RTC_XTAL2	BCCU0. OUT5	LEDTS1 .LINE1	LEDTS0 _OUT3	CCU40. OUT3	CCU80. OUT21	USIC0_ CH0.SE LO0	USIC0_ CH1.SE LO0	CCU81. OUT21	CCU41. OUT3		CCU40.I N3AB					USIC0_ CH0.D X2B		USIC0_ CH1.DX 2B			
P0.10/ XTAL1	BCCU0. OUT6	LEDTS1 .LINE2	LEDTS0 _COL5	ACMP0. OUT	CCU80. OUT22	USIC0_ CH0.SE LO1	USIC0_ CH1.SE LO1	CCU81. OUT22				CCU80.I N2AB	CCU81.I N2AB			USIC0_ CH0.D X2C		USIC0_ CH1.DX 2C			
P0.11/ XTAL2	BCCU0. OUT7	LEDTS1 .LINE3	LEDTS0 _COL4	USIC0_ CH0.MC LKOUT	CCU80. OUT23	USIC0_ CH0.SE LO2	USIC0_ CH1.SE LO2	CCU81. OUT23								USIC0_ CH0.D X2D		USIC0_ CH1.DX 2D			
P0.12	BCCU0. OUT6	LEDTS1 .LINE4	LEDTS0 _COL3	LEDTS1 _COL3	CCU80. OUT33	USIC0_ CH0.SE LO3	CCU80. OUT20		CAN.N1 _TXD	BCCU0. TRAPIN A	CCU40.I N0AA	CCU40.I N1AA	CCU40.I N2AA	CCU81.I N0AU	CCU40.I N3AA	CCU80.I N0AA	USIC0_ CH0.D X2E	CCU80.I N1AA	CCU80.I N2AA	CAN.N1 _RXDA	CCU80.I N3AA

Table 10 Hardware I/O Controlled Functions

Function	Outputs	Outputs	Inputs	Inputs	Pull Control	Pull Control	Pull Control	Pull Control
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P0.0	LEDTS0. EXTENDED7		LEDTS0.TSIN7	LEDTS0.TSIN7	Reserved for LEDTS Scheme A: pull-down disabled always	Reserved for LEDTS Scheme A: pull-down enabled always	Reserved for LEDTS Scheme B: pull-up enabled and pull-down disabled, and vice versa	
P0.1	LEDTS0. EXTENDED6		LEDTS0.TSIN6	LEDTS0.TSIN6				
P0.2	LEDTS0. EXTENDED5		LEDTS0.TSIN5	LEDTS0.TSIN5				
P0.3	LEDTS0. EXTENDED4		LEDTS0.TSIN4	LEDTS0.TSIN4				
P0.4	LEDTS0. EXTENDED3		LEDTS0.TSIN3	LEDTS0.TSIN3				
P0.5	LEDTS0. EXTENDED2		LEDTS0.TSIN2	LEDTS0.TSIN2				
P0.6	LEDTS0. EXTENDED1		LEDTS0.TSIN1	LEDTS0.TSIN1				
P0.7	LEDTS0. EXTENDED0		LEDTS0.TSIN0	LEDTS0.TSIN0				
P0.8	LEDTS1. EXTENDED0		LEDTS1.TSIN0	LEDTS1.TSIN0				
P0.9	LEDTS1. EXTENDED1		LEDTS1.TSIN1	LEDTS1.TSIN1				
P0.10	LEDTS1. EXTENDED2		LEDTS1.TSIN2	LEDTS1.TSIN2				
P0.11	LEDTS1. EXTENDED3		LEDTS1.TSIN3	LEDTS1.TSIN3				
P0.12	LEDTS1. EXTENDED4		LEDTS1.TSIN4	LEDTS1.TSIN4				
P0.13	LEDTS1. EXTENDED5		LEDTS1.TSIN5	LEDTS1.TSIN5				
P0.14	LEDTS1. EXTENDED6		LEDTS1.TSIN6	LEDTS1.TSIN6				
P0.15	LEDTS1. EXTENDED7		LEDTS1.TSIN7	LEDTS1.TSIN7				
P1.0		USIC0_CH0.DOUT0		USIC0_CH0.HWIN0	BCCU0.OUT2	BCCU0.OUT2		
P1.1		USIC0_CH0.DOUT1		USIC0_CH0.HWIN1	BCCU0.OUT3	BCCU0.OUT3		
P1.2		USIC0_CH0.DOUT2		USIC0_CH0.HWIN2	BCCU0.OUT4	BCCU0.OUT4		

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 12 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
 - pad supply levels (V_{DDP})
 - temperature

If a pin current is outside of the **Operating Conditions** but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 12 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	
Absolute sum of all input circuit currents during overload condition	I_{OVS} SR	–	–	25	mA	

Figure 11 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

3.2 DC Parameters

3.2.1 Input/Output Characteristics

Table 16 provides the characteristics of the input/output pins of the XMC1400.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.

Table 16 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Output low voltage on port pins (with standard pads)	V_{OLP}	CC	–	1.0	V	$I_{OL} = 11 \text{ mA}$ (5 V) $I_{OL} = 7 \text{ mA}$ (3.3 V)
			–	0.4	V	$I_{OL} = 5 \text{ mA}$ (5 V) $I_{OL} = 3.5 \text{ mA}$ (3.3 V)
Output low voltage on high current pads	V_{OLP1}	CC	–	1.0	V	$I_{OL} = 50 \text{ mA}$ (5 V) $I_{OL} = 25 \text{ mA}$ (3.3 V)
			–	0.32	V	$I_{OL} = 10 \text{ mA}$ (5 V)
			–	0.4	V	$I_{OL} = 5 \text{ mA}$ (3.3 V)
Output high voltage on port pins (with standard pads)	V_{OHP}	CC	$V_{DDP} - 1.0$	–	V	$I_{OH} = -10 \text{ mA}$ (5 V) $I_{OH} = -7 \text{ mA}$ (3.3 V)
			$V_{DDP} - 0.4$	–	V	$I_{OH} = -4.5 \text{ mA}$ (5 V) $I_{OH} = -2.5 \text{ mA}$ (3.3 V)
Output high voltage on high current pads	V_{OHP1}	CC	$V_{DDP} - 0.32$	–	V	$I_{OH} = -6 \text{ mA}$ (5 V)
			$V_{DDP} - 1.0$	–	V	$I_{OH} = -8 \text{ mA}$ (3.3 V)
			$V_{DDP} - 0.4$	–	V	$I_{OH} = -4 \text{ mA}$ (3.3 V)
Input low voltage on port pins (Standard Hysteresis)	V_{ILPS}	SR	–	$0.19 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input high voltage on port pins (Standard Hysteresis)	V_{IHPS}	SR	$0.7 \times V_{DDP}$	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)

Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input Hysteresis on port pin P2.3 - P2.9 ⁸⁾	HYS_ CC P2		$0.08 \times V_{DDP}$	—	V	CMOS Mode (5 V), Standard Hysteresis
			$0.03 \times V_{DDP}$	—	V	CMOS Mode (3.3 V), Standard Hysteresis
			$0.02 \times V_{DDP}$	—	V	CMOS Mode (2.2 V), Standard Hysteresis
			$0.35 \times V_{DDP}$	$0.75 \times V_{DDP}$	V	CMOS Mode(5 V), Large Hysteresis
			$0.25 \times V_{DDP}$	$0.75 \times V_{DDP}$	V	CMOS Mode(3.3 V), Large Hysteresis
			$0.15 \times V_{DDP}$	$0.65 \times V_{DDP}$	V	CMOS Mode(2.2 V), Large Hysteresis
Pin capacitance (digital inputs/outputs)	C _{IO}	CC	—	10	pF	
Pull-up current on port pins	I _{PUP}	CC	—	-80	μA	V _{IH,min} (5 V)
			-95	—	μA	V _{IL,max} (5 V)
			—	-50	μA	V _{IH,min} (3.3 V)
			-65	—	μA	V _{IL,max} (3.3 V)
Pull-down current on port pins	I _{PDP}	CC	—	40	μA	V _{IL,max} (5 V)
			95	—	μA	V _{IH,min} (5 V)
			—	30	μA	V _{IL,max} (3.3 V)
			60	—	μA	V _{IH,min} (3.3 V)
Input leakage current except P0.11 ⁹⁾	I _{OZP}	CC	-1	1	μA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105^\circ\text{C}$
Input leakage current for P0.11 ⁹⁾	I _{OZP1}	CC	-10	1	μA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105^\circ\text{C}$
Voltage on any pin during V _{DDP} power off	V _{PO}	SR	—	0.3	V	¹⁰⁾
Maximum current per pin (excluding P1, V _{DDP} and V _{SS})	I _{MP}	SR	-10	11	mA	—
Maximum current per high current pins	I _{MP1A}	SR	-10	50	mA	—

Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Maximum current into V_{DDP} (VQFN64, LQFP64)	I_{MVDD1}	SR	–	520	mA	
Maximum current into V_{DDP} (VQFN48)	I_{MVDD2}	SR	–	390	mA	
Maximum current into V_{DDP} (VQFN40)	I_{MVDD3}	SR	–	260	mA	
Maximum current out of V_{SS} (VQFN64, LQFP64)	I_{MVSS1}	SR	–	390	mA	
Maximum current out of V_{SS} (VQFN48)	I_{MVSS2}	SR	–	260	mA	
Maximum current out of V_{SS} (VQFN40)	I_{MVSS3}	SR	–	260	mA	

- 1) Rise/Fall time parameters are taken with 10% - 90% of supply.
- 2) Additional rise/fall time valid for $C_L = 50$ pF - $C_L = 100$ pF @ 0.150 ns/pF at 5 V supply voltage.
- 3) Additional rise/fall time valid for $C_L = 50$ pF - $C_L = 100$ pF @ 0.205 ns/pF at 3.3 V supply voltage.
- 4) Additional rise/fall time valid for $C_L = 50$ pF - $C_L = 100$ pF @ 0.445 ns/pF at 1.8 V supply voltage.
- 5) Additional rise/fall time valid for $C_L = 50$ pF - $C_L = 100$ pF @ 0.225 ns/pF at 5 V supply voltage.
- 6) Additional rise/fall time valid for $C_L = 50$ pF - $C_L = 100$ pF @ 0.288 ns/pF at 3.3 V supply voltage.
- 7) Additional rise/fall time valid for $C_L = 50$ pF - $C_L = 100$ pF @ 0.588 ns/pF at 1.8 V supply voltage.
- 8) Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
- 9) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.
- 10) However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

Electrical Parameter
Table 17 ADC Characteristics (Operating Conditions apply)¹⁾ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain settings	G_{IN} CC	1			–	GNCTRxz.GAINy = 00 _B (unity gain)
		3			–	GNCTRxz.GAINy = 01 _B (gain g1)
		6			–	GNCTRxz.GAINy = 10 _B (gain g2)
		12			–	GNCTRxz.GAINy = 11 _B (gain g3)
Sample Time	t_{sample} CC	5	–	–	1 / f_{ADC}	$V_{DD} = 5.0$ V, $f_{ADCI} = 48$ MHz
		3	–	–	1 / f_{ADC}	$V_{DD} = 5.0$ V, $f_{ADCI} = 32$ MHz
		3	–	–	1 / f_{ADC}	$V_{DD} = 3.3$ V, $f_{ADCI} = 32$ MHz
		30	–	–	1 / f_{ADC}	$V_{DD} = 2.0$ V, $f_{ADCI} = 32$ MHz
Conversion time in fast compare mode	t_{CF} CC	9			1 / f_{ADC}	³⁾
Conversion time in 12-bit mode	t_{C12} CC	20			1 / f_{ADC}	³⁾
Maximum sample rate in 12-bit mode ⁴⁾	f_{C12} CC	–	–	$f_{ADC} / 42.5$	–	1 sample pending
		–	–	$f_{ADC} / 62.5$	–	2 samples pending
Conversion time in 10-bit mode	t_{C10} CC	18			1 / f_{ADC}	³⁾
Maximum sample rate in 10-bit mode ⁴⁾	f_{C10} CC	–	–	$f_{ADC} / 40.5$	–	1 sample pending
		–	–	$f_{ADC} / 58.5$	–	2 samples pending
Conversion time in 8-bit mode	t_{C8} CC	16			1 / f_{ADC}	³⁾

Table 17 ADC Characteristics (Operating Conditions apply)¹⁾ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum sample rate in 8-bit mode ⁴⁾	f_{C8} CC	–	–	$f_{ADC} / 38.5$	–	1 sample pending
		–	–	$f_{ADC} / 54.5$	–	2 samples pending
RMS noise ⁵⁾	EN_{RMS} CC	–	1.5	–	LSB 12	DC input, SHSCFG.AREF = 00 _B , GNCTRxz.GAINy = 00 _B (unity gain), $V_{DD} = 5.0$ V, $V_{AIN} = 2.5$ V, 25°C
DNL error	EA_{DNL} CC	–	±2.0	–	LSB 12	
INL error	EA_{INL} CC	–	±4.0	–	LSB 12	
Gain error with external reference	EA_{GAIN} CC	–	±0.5	–	%	SHSCFG.AREF = 00 _B (calibrated)
Gain error with internal reference ⁶⁾	EA_{GAIN} CC	–	±3.6	–	%	SHSCFG.AREF = 1X _B (calibrated), -40°C - 110°C
		–	±2.0	–	%	SHSCFG.AREF = 1X _B (calibrated), 0°C - 85°C
Offset error	EA_{OFF} CC	–	±8.0	–	mV	Calibrated, $V_{DD} = 5.0$ V

1) The parameters are defined for ADC clock frequencies $f_{SH} = 32$ MHz for the full supply range, and $f_{SH} = 48$ MHz at $V_{DD_int} , V_{DD_ext} = 5$ V. Usage of any other frequencies may affect the ADC performance.

2) The alternate reference ground connection is separate for each converter. This mode, therefore, provides the lowest noise impact.

3) No pending samples assumed, excluding sampling time and calibration.

4) Includes synchronization and calibration (average of gain and offset calibration).

5) This parameter can also be defined as an SNR value: $SNR[dB] = 20 \times \log(A_{MAXeff} / N_{RMS})$.

With $A_{MAXeff} = 2^N / 2$, $SNR[dB] = 20 \times \log(2048 / N_{RMS})$ [$N = 12$].

$N_{RMS} = 1.5$ LSB12, therefore, equals $SNR = 20 \times \log(2048 / 1.5) = 62.7$ dB.

6) Includes error from the reference voltage.

3.2.4 Analog Comparator Characteristics

Table 19 below shows the Analog Comparator characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 19 Analog Comparator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Notes/ Test Conditions
			Min.	Typ.	Max.		
Input Voltage	V_{CMP}	SR	-0.05	—	$V_{DDP} + 0.05$	V	
Input Offset	V_{CMPOFF}	CC	—	+/-3	—	mV	High power mode $\Delta V_{CMP} < 200$ mV
Propagation Delay ¹⁾	t_{PDELAY}	CC	—	25	—	ns	High power mode, $\Delta V_{CMP} = 100$ mV
			—	80	—	ns	High power mode, $\Delta V_{CMP} = 25$ mV
			—	250	—	ns	Low power mode, $\Delta V_{CMP} = 100$ mV
			—	700	—	ns	Low power mode, $\Delta V_{CMP} = 25$ mV
Current Consumption	I_{ACMP}	CC	—	100	—	μA	First active ACMP in high power mode, $\Delta V_{CMP} > 30$ mV
			—	66	—	μA	Each additional ACMP in high power mode, $\Delta V_{CMP} > 30$ mV
			—	10	—	μA	First active ACMP in low power mode
			—	6	—	μA	Each additional ACMP in low power mode
Input Hysteresis	V_{HYS}	CC	—	+/-15	—	mV	
Filter Delay ¹⁾	t_{FDELAY}	CC	—	5	—	ns	

1) Total Analog Comparator Delay is the sum of Propagation Delay and Filter Delay.

3.3.3 On-Chip Oscillator Characteristics

Table 27 provides the characteristics of the 96 MHz digital controlled oscillator DCO1.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 27 96 MHz DCO1 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ	Max.		
Nominal frequency	f_{NOM}	CC	–	96	–	MHz	under nominal conditions ¹⁾ after trimming
Accuracy with adjustment based on XTAL as reference	Δf_{LTX}	CC	-0.3	–	0.3	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature (-40 °C to 105 °C)
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature (0 °C to 85 °C)
			-3.9	–	4.0	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature (-40 °C to 105 °C)

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and $T_{\text{A}} = + 25\text{ °C}$.

Table 28 provides the characteristics of the 32 kHz digital controlled oscillator DCO2.

Table 28 32 kHz DCO2 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	–	32.75	–	kHz	under nominal conditions ¹⁾ after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature (0 °C to 85 °C)
			-3.9	–	4.0	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature (-40 °C to 105 °C) ¹⁾

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and $T_{\text{A}} = + 25\text{ °C}$.

Table 32 USIC SSC Slave Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 hold after last clock input DX1 receive edge ¹⁾	t_{11} SR	17	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge ¹⁾	t_{12} SR	21	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge ¹⁾	t_{13} SR	15	–	–	ns	
Data output DOUT[3:0] valid time	t_{14} CC	-	–	71	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

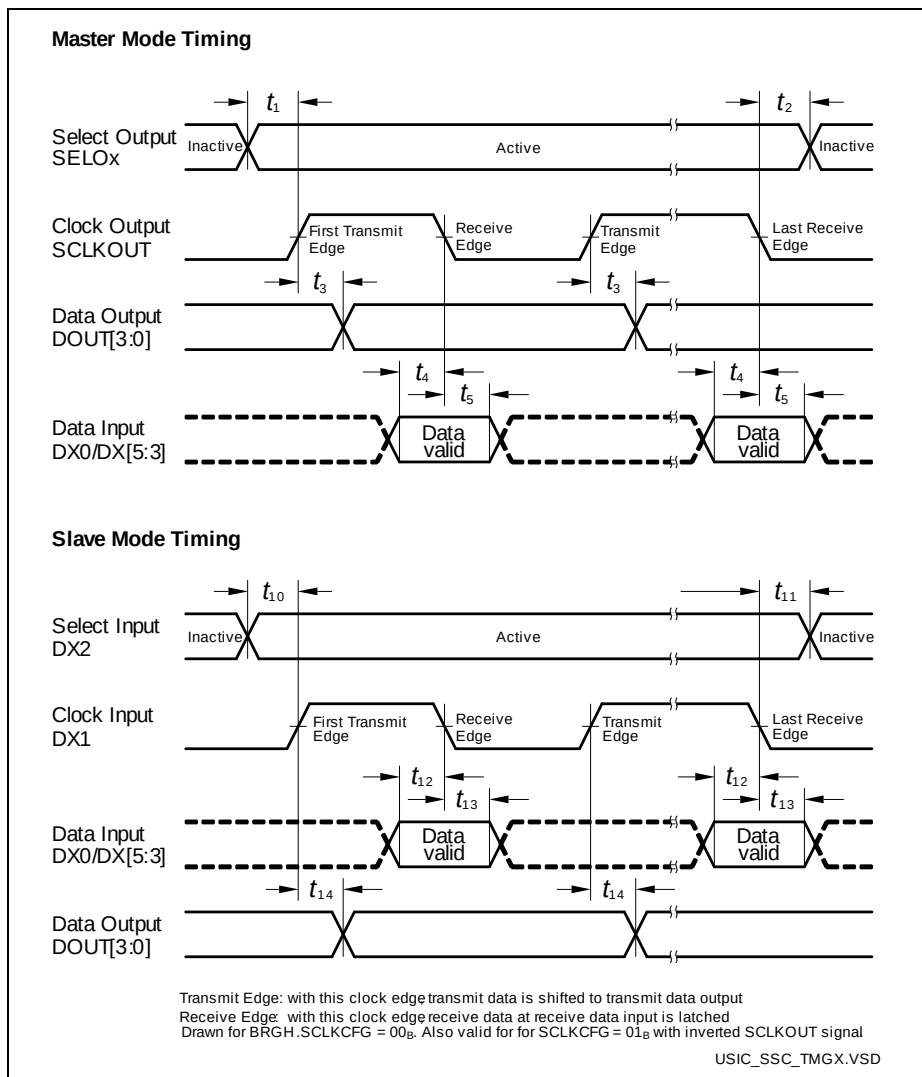


Figure 25 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

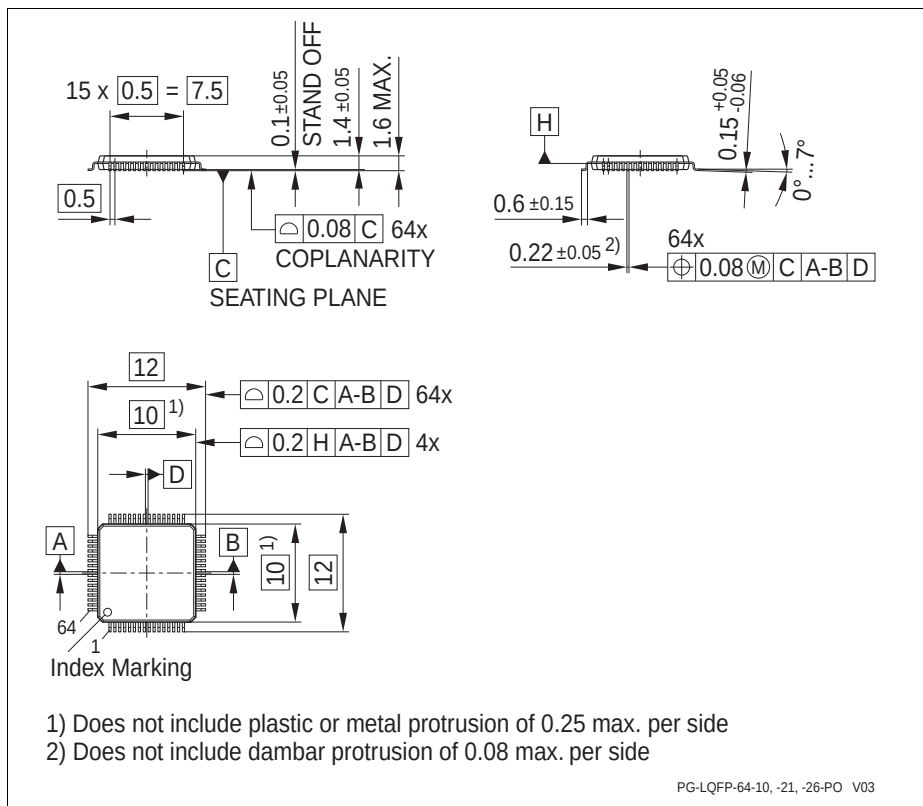


Figure 32 PG-LQFP-64-26

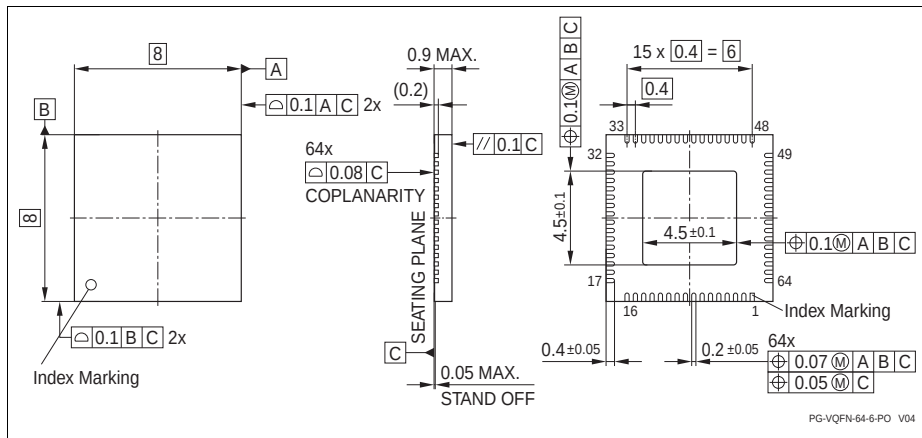


Figure 33 PG-VQFN-64-6

All dimensions in mm.

5 Quality Declaration

Table 38 shows the characteristics of the quality parameters in the XMC1400.

Table 38 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	-	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	-	3	-	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	-	260	°C	Profile according to JEDEC J-STD-020D

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