Infineon Technologies - XMC1403Q064X0200AAXUMA1 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	48
Program Memory Size	200KB (200K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-64-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1403q064x0200aaxuma1

Edition 2016-10

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Trademarks

C166™, TriCore™, XMC™ and DAVE™ are trademarks of Infineon Technologies AG.

ARM®, ARM Powered®, Cortex®, Thumb® and AMBA® are registered trademarks of ARM, Limited.

CoreSight™, ETM™, Embedded Trace Macrocell™ and Embedded Trace Buffer™ are trademarks of ARM, Limited.

We Listen to Your Comments

Is there any information in this document that you feel is wrong, unclear or missing? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

mcdocu.comments@infineon.com

Features

CPU subsystem

- 32-bit ARM Cortex-M0 CPU Core
  - 0.84 DMIPS/MHz (Dhrystone 2.1) at 48 MHz
- Nested Vectored Interrupt Controller
- 64 interrupt nodes
- MATH coprocessor
  - 24-bit trigonometric calculation (CORDIC)
  - 32-bit divide operation
- 2x4 channels ERU for event interconnections

On-Chip Memories

- 8 Kbyte ROM
- 16 Kbyte SRAM (with parity)
- up to 200 Kbyte Flash (with ECC)

Supply, Reset and Clock

- 1.8 V to 5.5 V supply with power on reset and brownout detector
- On-chip clock monitor
- External crystal oscillator support (32 kHz and 4 to 20 MHz)
- Internal slow and fast oscillators without the need of PLL

System Control

- Window watchdog
- Real time clock module
- Pseudo random number generator

Communication Peripherals

- Four USIC channels, usable as
  - UART (up to 12 Mb/s)
  - single-SPI (up to 12 Mb/s)
  - double-SPI (up to 2 × 12 Mb/s)
  - quad-SPI (up to 4 × 12 Mb/s)
  - IIC (up to 400 kb/s)
  - IIS (up to 12 Mb/s)
  - LIN interfaces (20kb/s)
- LEDTS in Human-Machine interface
  - up to 24 touch pads
  - drive up to 144 LEDs
- MultiCAN+, Full-CAN/Basic-CAN with 2 nodes, 32 message objects (up to 1 MBaud)

Analog Frontend Peripherals

- A/D Converters (up to 12 analog inputs)
  - 2 sample and hold stages
  - fast 12-bit ADC (up to 1.1 MS/s), adjustable gain
  - 0 V to 5.5 V input range
- Up to 8 channels out of range comparators
- Up to 4 fast analog comparators
- Temperature Sensor

Industrial Control Peripherals

- 2x4 16-bit 96 MHz CCU4 timers for signal monitoring and PWM
- 2x4 16-bit 96 MHz CCU8 timers for complex PWM, complementary high/low side switches and multi phase control
- 2x POSIF for hall and quadrature encoders, motor positioning
- 9 channel BCCU (brightness and color control) for LED lighting applications

Up to 56 Input/Output Ports

- 1.8 V to 5.5 V capable
- up to 8 high current pads (50 mA sink)

On-Chip Debug Support

- 4 breakpoints, 2 watchpoints
- ARM serial wire debug, single-pin debug interfaces

Programming Support

- Single-pin bootloader
- Secure bootstrap loader SBSL (optional)

Packages

- TSSOP-38 (9.7 × 6.4 mm^2)
- VQFN-40/48/64 (5×5/7×7/8×8 mm^2)
- LQFP-64 (12 × 12 mm^2)

Tools

- Free DAVE™ toolchain with low level drivers and apps

1.1 Device Overview

The following table lists the available features per device type for the XMC1400 series.

Table 1 Features of XMC1400 Device Types[1)]

Features		XMC1401-Q048	XMC1401-F064	XMC1402-T038	XMC1402-Q040	XMC1402-Q048	XMC1402-Q064	XMC1402-F064	XMC1403-Q040	XMC1403-Q048	XMC1403-Q064	XMC1404-Q048	XMC1404-Q064	XMC1404-F064
CPU frequency		48 MHz												
Operating temperature (ambient)		-40 to 85 °C		-40 to 105 °C										
Operating voltage		1.8 V to 5.5 V												
Flash options (Kbytes)		64, 128	64, 128	32, 64, 128 200	32, 64, 128 200	32, 64, 128 200	64, 128 200	64, 128 200	64, 128 200	64, 128 200	64, 128 200	64, 128 200	64, 128 200	64, 128 200
SRAM (Kbytes)		16	16	16	16	16	16	16	16	16	16	16	16	16
MATH		-	-	1	1	1	1	1	-	-	-	1	1	1
Industrial Control	CCU4	2	2	2	2	2	2	2	2	2	2	2	2	2
	CCU8	-	-	2	2	2	2	2	-	-	-	2	2	2
	POSIF	-	-	1	1	2	2	2	-	-	-	2	2	2
	BCCU	-	-	1	1	1	1	1	-	-	-	1	1	1
Communication	USIC (modules / channels)	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 2
	LEDTS	3	3	-	-	-	-	-	-	-	-	3	3	3
	MultiCAN+ (nodes / MOs)	-	-	-	-	-	-	-	2 / 32	2 / 32	2 / 32	2 / 32	2 / 32	2 / 32

1.3 Device Types

These device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 2 Synopsis of XMC1400 Device Types

Derivative	Package	Flash Kbytes
XMC1401-Q048F0064	PG-VQFN-48	64
XMC1401-Q048F0128	PG-VQFN-48	128
XMC1401-F064F0064	PG-LQFP-64	64
XMC1401-F064F0128	PG-LQFP-64	128
XMC1402-T038X0032	PG-TSSOP-38	32
XMC1402-T038X0064	PG-TSSOP-38	64
XMC1402-T038X0128	PG-TSSOP-38	128
XMC1402-T038X0200	PG-TSSOP-38	200
XMC1402-Q040X0032	PG-VQFN-40	32
XMC1402-Q040X0064	PG-VQFN-40	64
XMC1402-Q040X0128	PG-VQFN-40	128
XMC1402-Q040X0200	PG-VQFN-40	200
XMC1402-Q048X0032	PG-VQFN-48	32
XMC1402-Q048X0064	PG-VQFN-48	64
XMC1402-Q048X0128	PG-VQFN-48	128
XMC1402-Q048X0200	PG-VQFN-48	200
XMC1402-Q064X0064	PG-VQFN-64	64
XMC1402-Q064X0128	PG-VQFN-64	128
XMC1402-Q064X0200	PG-VQFN-64	200
XMC1402-F064X0064	PG-LQFP-64	64
XMC1402-F064X0128	PG-LQFP-64	128
XMC1402-F064X0200	PG-LQFP-64	200
XMC1403-Q040X0064	PG-VQFN-40	64
XMC1403-Q040X0128	PG-VQFN-40	128
XMC1403-Q040X0200	PG-VQFN-40	200
XMC1403-Q048X0064	PG-VQFN-48	64
XMC1403-Q048X0128	PG-VQFN-48	128

1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is an 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location : 1000 $0F00_H$ (MSB) - 1000 $0F1B_H$ (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

Table 3 XMC1400 Chip Identification Number

Derivative	Value	Marking
XMC1401-Q048F0064	00014082 07CF00FF 1E071FF7 20006000 00000D00 00001000 00011000 10204083_H	AA
XMC1401-Q048F0128	00014082 07CF00FF 1E071FF7 20006000 00000D00 00001000 00021000 10204083_H	AA
XMC1401-F064F0064	000140A2 07CF00FF 1E071FF7 20006000 00000D00 00001000 00011000 10204083_H	AA
XMC1401-F064F0128	000140A2 07CF00FF 1E071FF7 20006000 00000D00 00001000 00021000 10204083_H	AA
XMC1402-T038X0032	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00009000 10204083_H	AA
XMC1402-T038X0064	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00011000 10204083_H	AA
XMC1402-T038X0128	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00021000 10204083_H	AA
XMC1402-T038X0200	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00033000 10204083_H	AA
XMC1402-Q040X0032	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00009000 10204083_H	AA
XMC1402-Q040X0064	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00011000 10204083_H	AA
XMC1402-Q040X0128	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00021000 10204083_H	AA
XMC1402-Q040X0200	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00033000 10204083_H	AA
XMC1402-Q048X0032	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00009000 10204083_H	AA

Table 3 XMC1400 Chip Identification Number (cont'd)

Derivative	Value	Marking
XMC1402-Q048X0064	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00011000 10204083_H	AA
XMC1402-Q048X0128	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00021000 10204083_H	AA
XMC1402-Q048X0200	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00033000 10204083_H	AA
XMC1402-Q064X0064	00014093 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00011000 10204083_H	AA
XMC1402-Q064X0128	00014093 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00021000 10204083_H	AA
XMC1402-Q064X0200	00014093 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00033000 10204083_H	AA
XMC1402-F064X0064	000140A3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00011000 10204083_H	AA
XMC1402-F064X0128	000140A3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00021000 10204083_H	AA
XMC1402-F064X0200	000140A3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00033000 10204083_H	AA
XMC1403-Q040X0064	00014043 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00011000 10204083_H	AA
XMC1403-Q040X0128	00014043 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00021000 10204083_H	AA
XMC1403-Q040X0200	00014043 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00033000 10204083_H	AA
XMC1403-Q048X0064	00014083 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00011000 10204083_H	AA
XMC1403-Q048X0128	00014083 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00021000 10204083_H	AA
XMC1403-Q048X0200	00014083 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00033000 10204083_H	AA
XMC1403-Q064X0064	00014093 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00011000 10204083_H	AA
XMC1403-Q064X0128	00014093 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00021000 10204083_H	AA

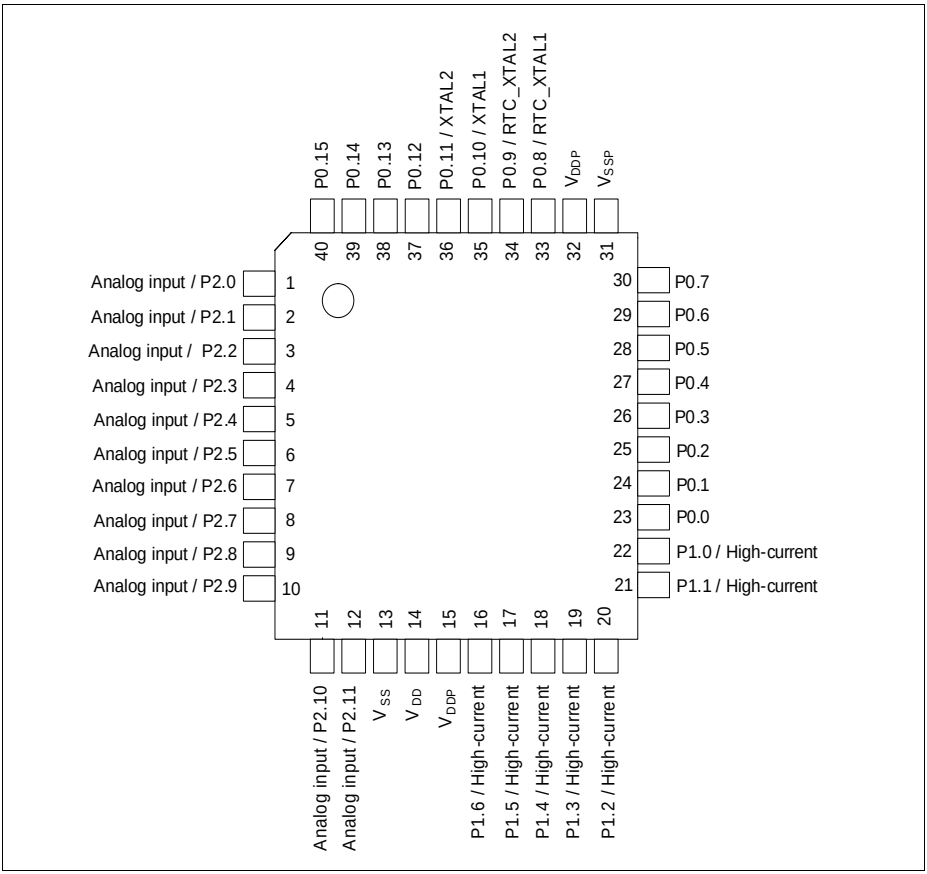


Figure 7 XMC1400 PG-VQFN-40-17 Pin Configuration (top view)

Table 10 Hardware I/O Controlled Functions

Function	Outputs	Outputs	Inputs	Inputs	Pull Control	Pull Control	Pull Control	Pull Control
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P1.3		USIC0_CH0.DOUT3		USIC0_CH0.HWIN3	$\overline{\text{BCCU0.OUT5}}$	BCCU0.OUT5		
P1.4					$\overline{\text{BCCU0.OUT6}}$	BCCU0.OUT6		
P1.5					$\overline{\text{BCCU0.OUT7}}$	BCCU0.OUT7		
P1.6					$\overline{\text{BCCU0.OUT8}}$	BCCU0.OUT8		
P1.7								
P1.8								
P2.0					$\overline{\text{BCCU0.OUT1}}$	BCCU0.OUT1		
P2.1					$\overline{\text{BCCU0.OUT6}}$	BCCU0.OUT6		
P2.2					$\overline{\text{BCCU0.OUT0}}$	BCCU0.OUT0	$\overline{\text{CCU40.OUT3}}$	CCU40.OUT3
P2.3					$\overline{\text{ACMP2.OUT}}$	ACMP2.OUT		
P2.4					$\overline{\text{BCCU0.OUT8}}$	BCCU0.OUT8		
P2.5					$\overline{\text{ACMP1.OUT}}$	ACMP1.OUT		
P2.6					$\overline{\text{BCCU0.OUT2}}$	BCCU0.OUT2	$\overline{\text{CCU40.OUT3}}$	CCU40.OUT3
P2.7					$\overline{\text{BCCU0.OUT8}}$	BCCU0.OUT8	$\overline{\text{CCU40.OUT3}}$	CCU40.OUT3
P2.8					$\overline{\text{BCCU0.OUT1}}$	BCCU0.OUT1	$\overline{\text{CCU40.OUT2}}$	CCU40.OUT2
P2.9					$\overline{\text{BCCU0.OUT7}}$	BCCU0.OUT7	$\overline{\text{CCU40.OUT2}}$	CCU40.OUT2
P2.10					$\overline{\text{BCCU0.OUT4}}$	BCCU0.OUT4		
P2.11					$\overline{\text{BCCU0.OUT5}}$	BCCU0.OUT5		
P2.12					$\overline{\text{BCCU0.OUT3}}$	BCCU0.OUT3	$\overline{\text{CCU41.OUT0}}$	CCU41.OUT0
P2.13					$\overline{\text{BCCU0.OUT4}}$	BCCU0.OUT4	$\overline{\text{CCU41.OUT2}}$	CCU41.OUT2
P3.0								
P3.1		USIC1_CH0.DOUT3		USIC1_CH0.HWIN3				
P3.2		USIC1_CH0.DOUT2		USIC1_CH0.HWIN2				
P3.3		USIC1_CH0.DOUT1		USIC1_CH0.HWIN1				
P3.4		USIC1_CH0.DOUT0		USIC1_CH0.HWIN0				
P4.0								
P4.1								
P4.2								
P4.3								

Table 10 Hardware I/O Controlled Functions

Function	Outputs	Outputs	Inputs	Inputs	Pull Control	Pull Control	Pull Control	Pull Control
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P4.4	LEDTS2. EXTENDED0		LEDTS2.TSIN0	LEDTS2.TSIN0	Reserved for LEDTS Scheme A: pull-down disabled always	Reserved for LEDTS Scheme A: pull-down enabled always	Reserved for LEDTS Scheme B: pull-up enabled and pull-down disabled, and vice versa	
P4.5	LEDTS2. EXTENDED1		LEDTS2.TSIN1	LEDTS2.TSIN1				
P4.6	LEDTS2. EXTENDED2		LEDTS2.TSIN2	LEDTS2.TSIN2				
P4.7	LEDTS2. EXTENDED3		LEDTS2.TSIN3	LEDTS2.TSIN3				
P4.8	LEDTS2. EXTENDED4		LEDTS2.TSIN4	LEDTS2.TSIN4				
P4.9	LEDTS2. EXTENDED5		LEDTS2.TSIN5	LEDTS2.TSIN5				
P4.10	LEDTS2. EXTENDED6		LEDTS2.TSIN6	LEDTS2.TSIN6				
P4.11	LEDTS2. EXTENDED7		LEDTS2.TSIN7	LEDTS2.TSIN7				

3 Electrical Parameter

This section provides the electrical parameter which are implementation-specific for the XMC1400.

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XMC1400 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the XMC1400 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC1400 is designed in.

3.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC1400. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 15 Operating Conditions Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Ambient Temperature	T_A	SR	-40	–	85	°C	Temp. Range F
			-40	–	105	°C	Temp. Range X
Digital supply voltage[1)]	V_{DDP}	SR	1.8	–	5.5	V	
Short circuit current of digital outputs	I_{SC}	SR	-5	–	5	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D}	SR	–	–	25	mA	

1) See also the Supply Monitoring thresholds, **Chapter 3.3.2**.

Table 23 Power Supply parameter table; V_{DDP} = 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.[1]	Max.		
Sleep mode current Peripherals clock disabled Flash active f_{MCLK} / f_{PCLK} in MHz[5]	I_{DDPSD} CC	–	2.8	–	mA	48 / 96
		–	2.2	–	mA	24 / 48
		–	2.0	–	mA	16 / 32
		–	1.9	–	mA	8 / 16
		–	1.7	–	mA	1 / 1
Sleep mode current Peripherals clock disabled Flash powered down f_{MCLK} / f_{PCLK} in MHz[6]	I_{DDPSR} CC	–	2.2	–	mA	48 / 96
		–	1.7	–	mA	24 / 48
		–	1.4	–	mA	16 / 32
		–	1.2	–	mA	8 / 16
		–	1.1	–	mA	1 / 1
Deep Sleep mode current[7]	I_{DDPDS} CC	–	0.27	–	mA	
Wake-up time from Sleep to Active mode[8]	t_{SSA} CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode[9]	t_{DSA} CC	–	290	–	µsec	

1) The typical values are measured at T_A = + 25 °C and V_{DDP} = 5 V.
2) CPU and all peripherals clock enabled, Flash is in active mode.
3) CPU enabled, all peripherals clock disabled, Flash is in active mode.
4) CPU in sleep, all peripherals clock enabled and Flash is in active mode.
5) CPU in sleep, Flash is in active mode.
6) CPU in sleep, Flash is powered down and code executed from RAM after wake-up.
7) CPU in sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.
8) CPU in sleep, Flash is in active mode during sleep mode.
9) CPU in sleep, Flash is in powered down mode during deep sleep mode.

10) Active current is measured with: module enabled, MCLK=48 MHz, time-out mode; WLB = 0, WUB = 0x00008000; WDT serviced every 1 s

11) Active current is measured with: module enabled, MCLK=48 MHz, Periodic interrupt enabled

12) Active current is measured with: module enabled, MCLK=48 MHz, running at 20 MHz baudrate generator, 1 node activated, 1 transmit and 1 receive object active.

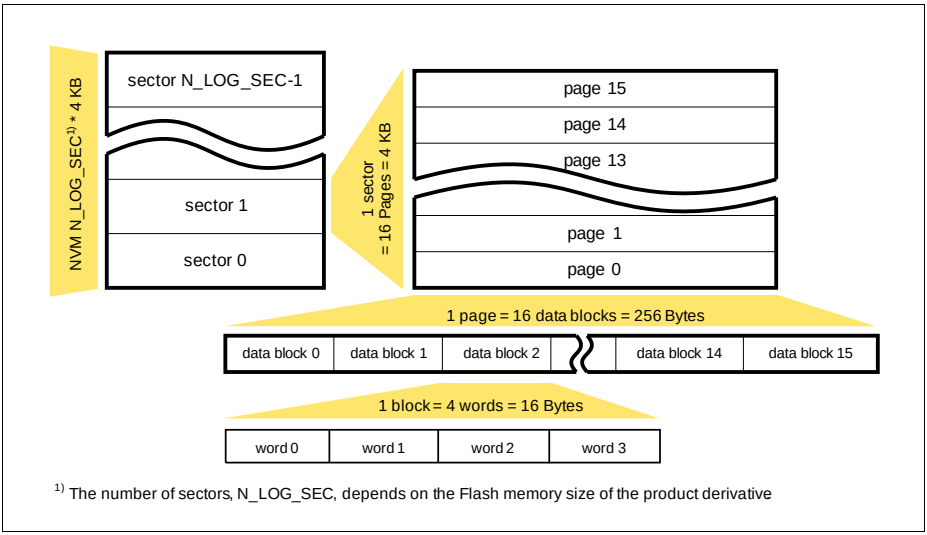
3.2.8 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase time per page / sector	t_{ERASE} CC	6.8	7.1	7.6	ms	
Program time per block	t_{PSER} CC	102	152	204	µs	
Wake-Up time	t_{WU} CC	–	32.2	–	µs	
Read time per word	t_a CC	–	50	–	ns	
Data Retention Time	t_{RET} CC	10	–	–	years	Max. 100 erase / program cycles
Flash Wait States [1]	$N_{WSFLASH}$ CC	0	0	0		f_{MCLK} = 8 MHz
		0	1	1		f_{MCLK} = 16 MHz
		1	2	2		f_{MCLK} = 32 MHz
		2	2	3		f_{MCLK} = 48 MHz
Erase Cycles	N_{ECYC} CC	–	–	$5*10^4$	cycles	Sum of page and sector erase cycles
Total Erase Cycles	N_{TECYC} CC	–	–	$2*10^6$	cycles	

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.



[1] The number of sectors, N_LOG_SEC, depends on the Flash memory size of the product derivative

Figure 19 Logical Structure of the Flash

3.3.2 Power-Up and Supply Threshold Characteristics

Table 26 provides the characteristics of the supply threshold in XMC1400.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DDP} is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 26 Power-Up and Supply Threshold Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} ramp-up time	t_{RAMPUP} SR	V_{DDP}/ $S_{VDDPrise}$	–	10^7	µs	
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	V/µs	Slope during normal operation
	S_{VDDP10} SR	0	–	10	V/µs	Slope during fast transient within +/-10% of V_{DDP}
	$S_{VDDPrise}$ SR	0	–	10	V/µs	Slope during power-on or restart after brownout event
	$S_{VDDPfall}$[1] SR	0	–	0.25	V/µs	Slope during supply falling out of the +/-10% limits[2]
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00_B
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01_B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10_B

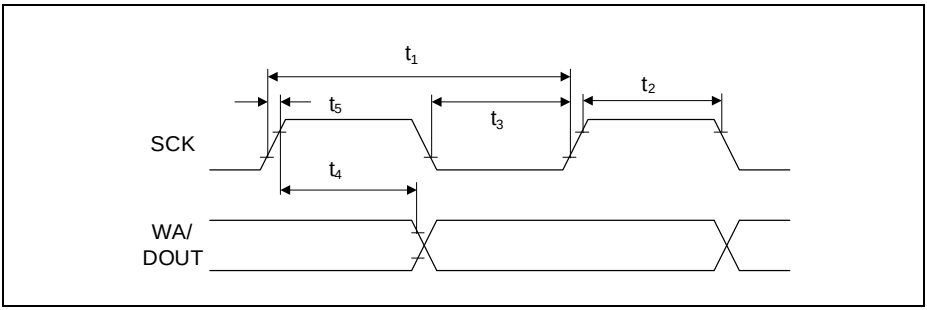


Figure 27 USIC IIS Master Transmitter Timing

Table 36 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	t_7 SR	0.35 x t_{6min}	-	-	ns	
Clock Low	t_8 SR	0.35 x t_{6min}	-	-	ns	
Set-up time	t_9 SR	0.3 x t_{6min}	-	-	ns	
Hold time	t_{10} SR	15	-	-	ns	

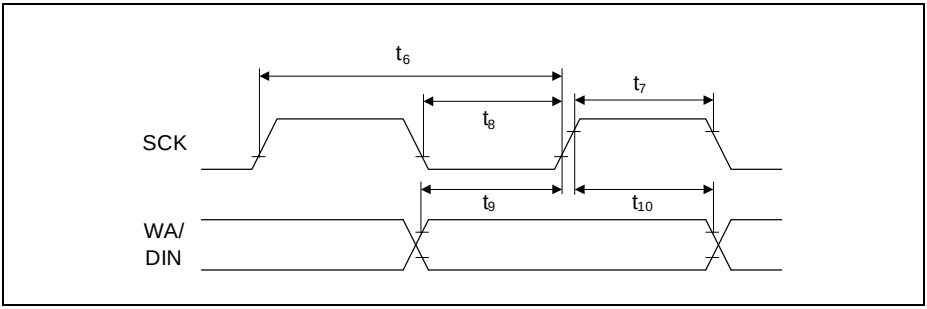


Figure 28 USIC IIS Slave Receiver Timing

4.2 Package Outlines

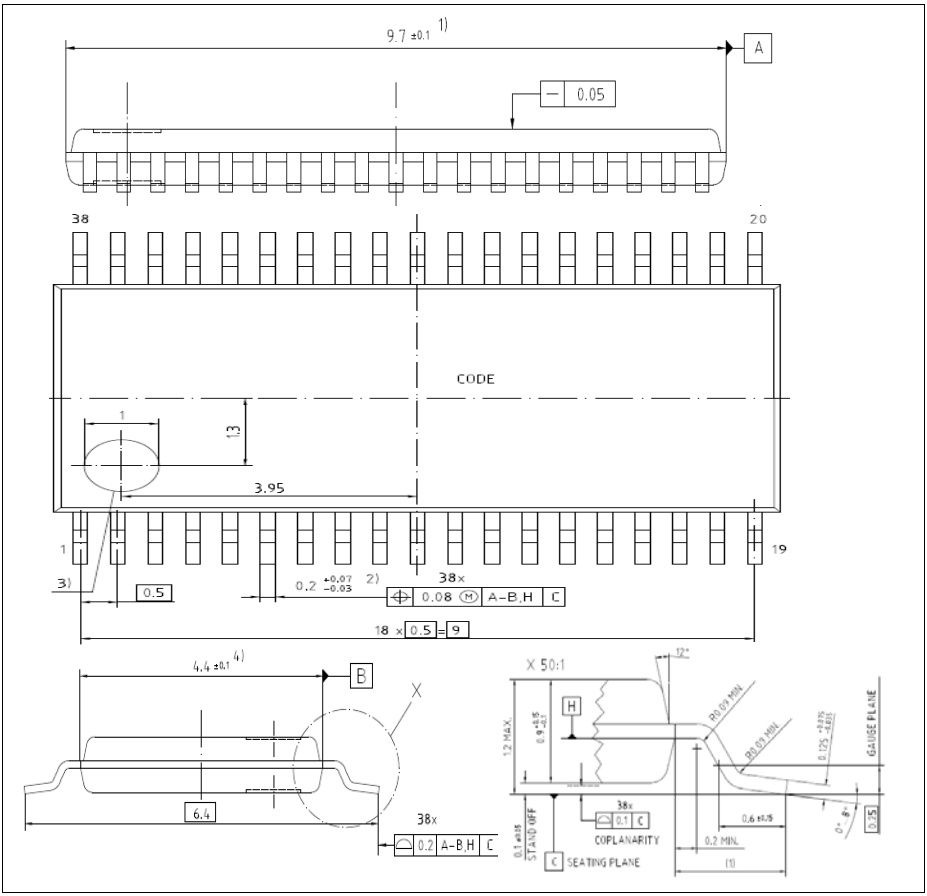


Figure 29 PG-TSSOP-38-9