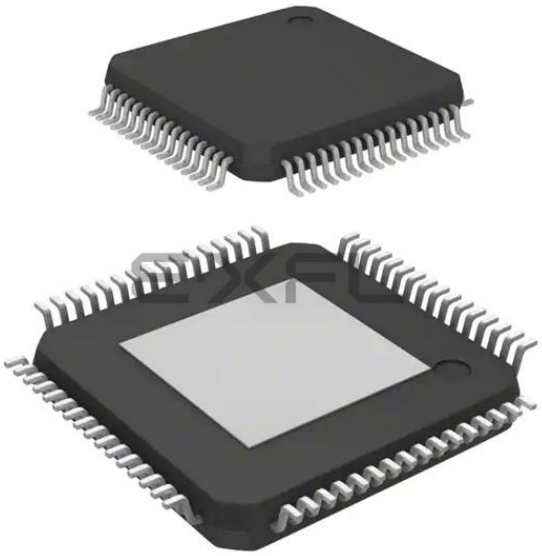
Infineon Technologies - XMC1404F064X0064AAXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, LED, POR, PWM, WDT
Number of I/O	48
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1404f064x0064aaxuma1

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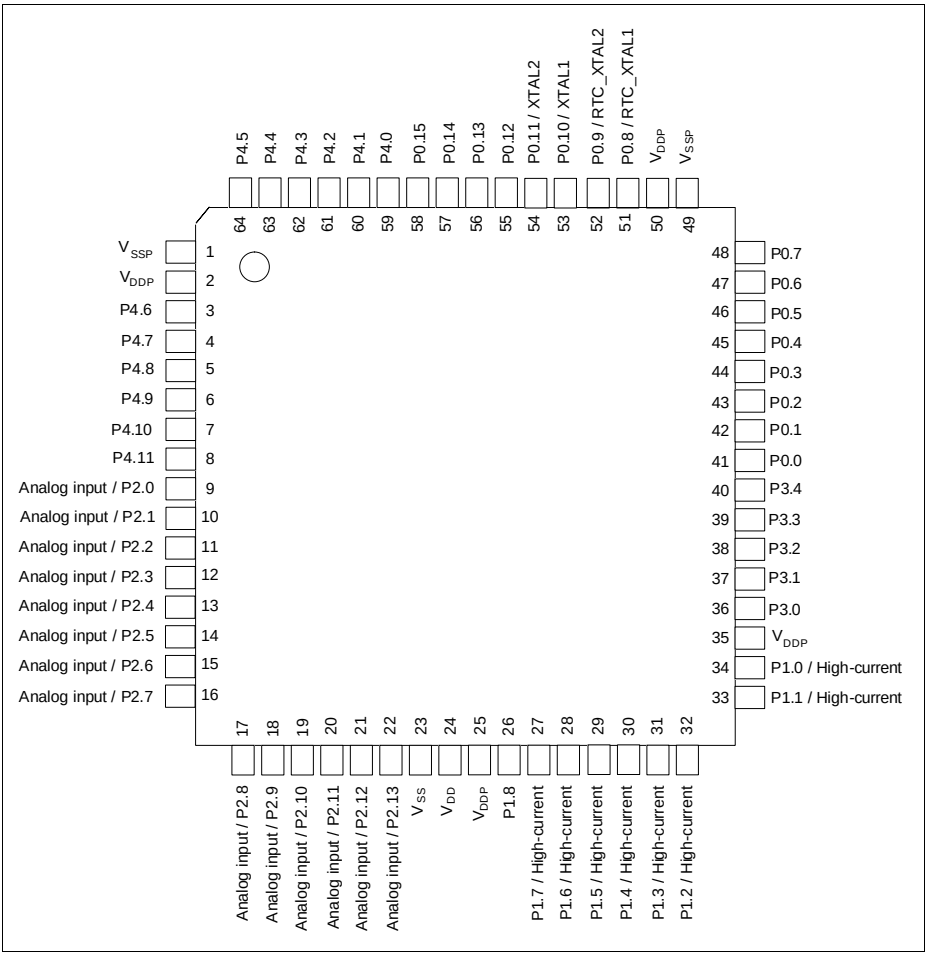


Figure 9 XMC1400 PG-LQFP-64-26 / PG-VQFN-64-6 Pin Configuration (top view)

Table 5 Package Pin Mapping (cont'd)

Function	LQFP 64, VQFN 64	VQFN 48	VQFN 40	TSSOP 38	Pad Type	Notes
VDD	24	18	14	10	Power	Supply VDD, ADC reference voltage/ ORC reference voltage
VDDP	25	19	15	10	Power	When VDD is supplied, VDDP has to be supplied with the same voltage.
VDDP	2	-	-	-	Power	I/O port supply
VDDP	35	27	-	-	Power	I/O port supply
VDDP	50	38	32	26	Power	I/O port supply
VSSP	1	-	-	-	Power	I/O port ground
VSSP	49	37	31	25	Power	I/O port ground
VSSP	Exp. Pad (in VQFN 64 only)	Exp. Pad	Exp. Pad	-	Power	**Exposed Die Pad** The exposed die pad is connected internally to VSSP. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, please refer to the Package and Reliability chapter.

Table 9 Port I/O Functions (cont'd)

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P0.13	WWDT.SERVICE_OUT	LEDTS1.LINE5	LEDTS0.COL2	LEDTS1.COL2	CCU80.OUT32	USIC0_CH0.SELO4	CCU80.OUT21		CAN.N1_TXD				CCU80.IN3AB	CCU81.IN1AU	POSIF0.IN0B		USIC0_CH0.DX2F			CAN.N1_RXDB	
P0.14	BCCU0.OUT7	LEDTS1.LINE6	LEDTS0.COL1	LEDTS1.COL1	CCU80.OUT31	USIC0_CH0.DOUT0	USIC0_CH0.SCLKOUT		CAN.N0_TXD					CCU81.IN2AU	POSIF0.IN1B	USIC0_CH0.DX0A	USIC0_CH0.DX1A	USIC1_CH1.DX5B		CAN.N0_RXDC	
P0.15	BCCU0.OUT8	LEDTS1.LINE7	LEDTS0.COL0	LEDTS1.COL0	CCU80.OUT30	USIC0_CH0.DOUT0	USIC0_CH1.MCLKOUT		CAN.N0_TXD					CCU81.IN3AU	POSIF0.IN2B	USIC0_CH0.DX0B		USIC1_CH1.DX3B	USIC1_CH1.DX4B	CAN.N0_RXDD	
P1.0	BCCU0.OUT0	CCU40.OUT0	LEDTS0.COL0	LEDTS1.COLA	CCU80.OUT00	ACMP1.OUT	USIC0_CH0.DOUT0	CCU81.OUT00	CAN.N0_TXD						POSIF0.IN2A	USIC0_CH0.DX0C				CAN.N0_RXDG	
P1.1	ERU1.PDOUT1	CCU40.OUT1	LEDTS0.COL1	LEDTS1.COL0	CCU80.OUT01	USIC0_CH0.DOUT0	USIC0_CH1.SELO0	CCU81.OUT01	CAN.N0_TXD						POSIF0.IN1A	USIC0_CH0.DX0D	USIC0_CH0.DX1D		USIC0_CH1.DX2E	CAN.N0_RXDH	
P1.2	ERU1.PDOUT2	CCU40.OUT2	LEDTS0.COL2	LEDTS1.COL1	CCU80.OUT10	ACMP2.OUT	USIC0_CH1.DOUT0	CCU81.OUT10	CAN.N1_TXD						POSIF0.IN0A			USIC0_CH1.DX0B		CAN.N1_RXDG	
P1.3	ERU1.PDOUT3	CCU40.OUT3	LEDTS0.COL3	LEDTS1.COL2	CCU80.OUT11	USIC0_CH1.SCLKOUT	USIC0_CH1.DOUT0	CCU81.OUT11	CAN.N1_TXD									USIC0_CH1.DX0A	USIC0_CH1.DX1A	CAN.N1_RXDH	
P1.4	ERU1.PDOUT0	USIC0_CH1.SCLKOUT	LEDTS0.COL4	LEDTS1.COL3	CCU80.OUT20	USIC0_CH0.SELO0	USIC0_CH1.SELO1	CCU81.OUT20	CCU41.OUT0							USIC0_CH0.DX5E		USIC0_CH1.DX5E			
P1.5	ERU1.PDOUT1	USIC0_CH0.DOUT0	LEDTS0.COLA	BCCU0.OUT1	CCU80.OUT21	USIC0_CH0.SELO1	USIC0_CH1.SELO2	CCU81.OUT21	CCU41.OUT1									USIC0_CH1.DX5F			
P1.6	ERU1.PDOUT2	USIC0_CH1.DOUT0	LEDTS0.COL5	USIC0_CH0.SCLKOUT	BCCU0.OUT2	USIC0_CH0.SELO2	USIC0_CH1.SELO3	CCU81.OUT30	CCU41.OUT2						POSIF1.IN2A	USIC0_CH0.DX5F					
P1.7	BCCU0.OUT8	CCU40.OUT3	LEDTS0.COL6	LEDTS1.COL4		ACMP3.OUT	ERU1.PDOUT3	CCU81.OUT31	CCU41.OUT3						POSIF1.IN1A	USIC1_CH0.DX5B			USIC1_CH1.DX2C		
P1.8	BCCU0.OUT0	CCU40.OUT0	USIC1_CH1.SCLKOUT	VADC0.EMUX02		ACMP1.OUT	ERU1.PDOUT0	CCU81.OUT32							POSIF1.IN0A	USIC1_CH0.DX3B	USIC1_CH0.DX4B		USIC1_CH1.DX1C		
P2.0	ERU0.PDOUT3	CCU40.OUT0	ERU0.GOUT3	LEDTS1.COL5	CCU80.OUT20	USIC0_CH0.DOUT0	USIC0_CH0.SCLKOUT	CCU81.OUT20	CAN.N0_TXD		VADC0.G0CH5					USIC0_CH0.DX0E	USIC0_CH0.DX1E		USIC0_CH1.DX2F	CAN.N0_RXDE	ERU0.0B0
P2.1	ERU0.PDOUT2	CCU40.OUT1	ERU0.GOUT2	LEDTS1.COL6	CCU80.OUT21	USIC0_CH0.DOUT0	USIC0_CH1.SCLKOUT	CCU81.OUT21	CAN.N0_TXD	ACMP2.INP	VADC0.G0CH6					USIC0_CH0.DX0F		USIC0_CH1.DX3A	USIC0_CH1.DX4A	CAN.N0_RXDF	ERU0.1B0

Table 9 Port I/O Functions (cont'd)

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P2.2										ACMP2.INN	VADC0.G0CH7		ORC0.AIN	USIC1_CH0.DX5E		USIC0_CH0.DX3A	USIC0_CH0.DX4A	USIC0_CH1.DX5A			ERU0.0B1
P2.3												VADC0.G1CH5	ORC1.AIN	USIC1_CH0.DX3E	USIC1_CH0.DX4E	USIC1_CH1.DX5C	USIC0_CH0.DX5B	USIC0_CH1.DX3C	USIC0_CH1.DX4C		ERU0.1B1
P2.4												VADC0.G1CH6	ORC2.AIN	USIC1_CH1.DX3C	USIC1_CH1.DX4C	USIC0_CH0.DX3B	USIC0_CH0.DX4B	USIC1_CH0.DX5F	USIC0_CH1.DX5B		ERU0.0A1
P2.5												VADC0.G1CH7	ORC3.AIN	USIC1_CH1.DX5D		USIC0_CH0.DX5D		USIC0_CH1.DX3E	USIC0_CH1.DX4E		ERU0.1A1
P2.6										ACMP1.INN	VADC0.G0CH0		ORC4.AIN	USIC1_CH1.DX3E	USIC1_CH1.DX4E	USIC0_CH0.DX3E	USIC0_CH0.DX4E	USIC0_CH1.DX5D			ERU0.2A1
P2.7										ACMP1.INP		VADC0.G1CH1	ORC5.AIN	USIC1_CH1.DX5E		USIC0_CH0.DX5C		USIC0_CH1.DX3D	USIC0_CH1.DX4D		ERU0.3A1
P2.8										ACMP0.INN	VADC0.G0CH1	VADC0.G1CH0	ORC6.AIN			USIC0_CH0.DX3D	USIC0_CH0.DX4D	USIC0_CH1.DX5C			ERU0.3B1
P2.9										ACMP0.INP	VADC0.G0CH2	VADC0.G1CH4	ORC7.AIN			USIC0_CH0.DX5A		USIC0_CH1.DX3B	USIC0_CH1.DX4B		ERU0.3B0
P2.10	ERU0.PDOUT1	CCU40.OUT2	ERU0.GOUT1	LEDTS1.COL4	CCU80.OUT30	ACMP0.OUT	USIC0_CH1.DOUT0		CAN.N1_TXD		VADC0.G0CH3	VADC0.G1CH2				USIC0_CH0.DX3C	USIC0_CH0.DX4C	USIC0_CH1.DX0F		CAN.N1_RXDE	ERU0.2B0
P2.11	ERU0.PDOUT0	CCU40.OUT3	ERU0.GOUT0	LEDTS1.COL3	CCU80.OUT31	USIC0_CH1.SCLKOUT	USIC0_CH1.DOUT0		CAN.N1_TXD	ACMP.REF	VADC0.G0CH4	VADC0.G1CH3						USIC0_CH1.DX0E	USIC0_CH1.DX1E	CAN.N1_RXDF	ERU0.2B1
P2.12	BCCU0.OUT3	VADC0.EMUX00	USIC1_CH0.SCLKOUT	USIC1_CH1.SCLKOUT		ACMP2.OUT	USIC1_CH1.DOUT0	LEDTS2.COL6		ACMP3.INN						USIC1_CH0.DX3A	USIC1_CH0.DX4A	USIC1_CH1.DX0C	USIC1_CH1.DX1B		ERU1.3A2
P2.13	BCCU0.OUT4	CCU40.OUT3	USIC1_CH0.MCLKOUT	CCU81.OUT31		VADC0.EMUX01	USIC1_CH1.DOUT0	CCU81.OUT33	CCU41.OUT3	ACMP3.INP						USIC1_CH0.DX5A		USIC1_CH1.DX0D			ERU1.3A3
P3.0	BCCU0.OUT0	USIC1_CH1.DOUT0	USIC1_CH1.SCLKOUT	LEDTS2.COLA	CCU80.OUT21	ACMP1.OUT	USIC1_CH0.SELO1	CCU81.OUT21	CCU41.OUT0	BCCU0.TRAPINC	CCU41.IN0AA	CCU41.IN1AA	CCU41.IN2AA	CCU41.IN3AA	CCU81.IN0AA	CCU81.IN1AA	CCU81.IN2AA	USIC1_CH1.DX0E	USIC1_CH1.DX1D	CCU81.IN3AA	ERU1.0A1
P3.1	BCCU0.OUT1	USIC1_CH1.DOUT0		LEDTS2.COL0	CCU80.OUT20	ACMP3.OUT	USIC1_CH0.SELO0	CCU81.OUT20	CCU41.OUT1								USIC1_CH0.DX2F	USIC1_CH1.DX0F			ERU1.1A1

Table 10 Hardware I/O Controlled Functions

Function	Outputs	Outputs	Inputs	Inputs	Pull Control	Pull Control	Pull Control	Pull Control
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P4.4	LEDTS2. EXTENDED0		LEDTS2.TSIN0	LEDTS2.TSIN0	Reserved for LEDTS Scheme A: pull-down disabled always	Reserved for LEDTS Scheme A: pull-down enabled always	Reserved for LEDTS Scheme B: pull-up enabled and pull-down disabled, and vice versa	
P4.5	LEDTS2. EXTENDED1		LEDTS2.TSIN1	LEDTS2.TSIN1				
P4.6	LEDTS2. EXTENDED2		LEDTS2.TSIN2	LEDTS2.TSIN2				
P4.7	LEDTS2. EXTENDED3		LEDTS2.TSIN3	LEDTS2.TSIN3				
P4.8	LEDTS2. EXTENDED4		LEDTS2.TSIN4	LEDTS2.TSIN4				
P4.9	LEDTS2. EXTENDED5		LEDTS2.TSIN5	LEDTS2.TSIN5				
P4.10	LEDTS2. EXTENDED6		LEDTS2.TSIN6	LEDTS2.TSIN6				
P4.11	LEDTS2. EXTENDED7		LEDTS2.TSIN7	LEDTS2.TSIN7				

Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Maximum current into V_{DDP} (VQFN64, LQFP64)	I_{MVDD1}	SR	–	520	mA	
Maximum current into V_{DDP} (VQFN48)	I_{MVDD2}	SR	–	390	mA	
Maximum current into V_{DDP} (VQFN40)	I_{MVDD3}	SR	–	260	mA	
Maximum current out of V_{SS} (VQFN64, LQFP64)	I_{MVSS1}	SR	–	390	mA	
Maximum current out of V_{SS} (VQFN48)	I_{MVSS2}	SR	–	260	mA	
Maximum current out of V_{SS} (VQFN40)	I_{MVSS3}	SR	–	260	mA	

1) Rise/Fall time parameters are taken with 10% - 90% of supply.
2) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.150 ns/pF at 5 V supply voltage.
3) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.205 ns/pF at 3.3 V supply voltage.
4) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.445 ns/pF at 1.8 V supply voltage.
5) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.225 ns/pF at 5 V supply voltage.
6) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.288 ns/pF at 3.3 V supply voltage.
7) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.588 ns/pF at 1.8 V supply voltage.
8) Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
9) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.
10) However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

3.2.2 Analog to Digital Converters (ADC)

Table 17 shows the Analog to Digital Converter (ADC) characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 17 ADC Characteristics (Operating Conditions apply)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	V_{DD_int} SR	2.0	–	3.0	V	SHSCFG.AREF = 11_B; CALCTR.CALGNSTC = $0C_H$ for f_{SH} = 32 MHz, 12_H for f_{SH} = 48 MHz
		3.0	–	5.5	V	SHSCFG.AREF = 10_B
Supply voltage range (external reference)	V_{DD_ext} SR	3.0	–	5.5	V	SHSCFG.AREF = 00_B
Analog input voltage range	V_{AIN} SR	V_{SSP} - 0.05	–	V_{DDP} + 0.05	V	
Auxiliary analog reference ground[2)]	V_{REFGND} SR	V_{SSP} - 0.05	–	1.0	V	G0CH0
		V_{SSP} - 0.05	–	0.2	V	G1CH0
Internal reference voltage (full scale value)	V_{REFINT} CC	5			V	
Switched capacitance of an analog input	C_{AINS} CC	–	1.2	2	pF	GNCTRxz.GAINy = 00_B (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01_B (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10_B (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11_B (gain g3)
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	

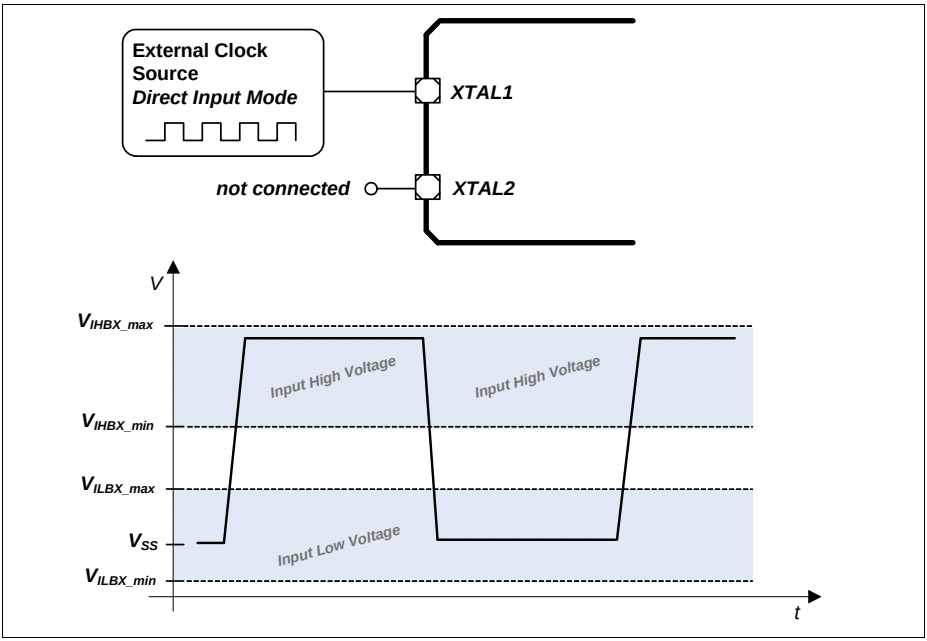


Figure 16 Oscillator in Direct Input Mode

Table 22 RTC_XTAL Parameters

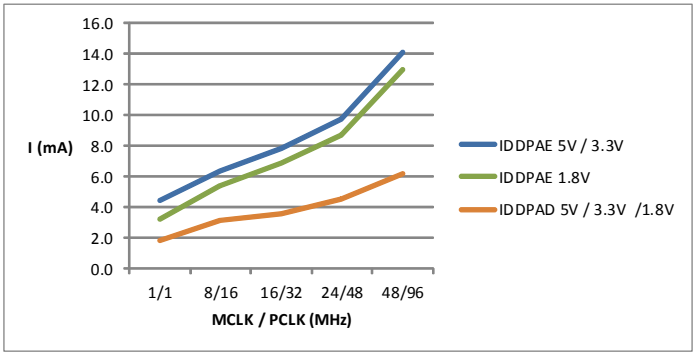
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	–	32.768	–	kHz	
Oscillator start-up time[1)2)]	t_{OSCS} CC	–	–	5	s	
Input voltage at RTC_XTAL1	V_{IX} SR	-0.3	–	1.5	V	
Input amplitude (peak-to-peak) at RTC_XTAL1[2)3)]	V_{PPX} SR	0.2	–	1.2	V	

1) t_{OSCS} is defined from the moment the oscillator is enabled by the user with SCU_ANAOSCLPCTRL.MODE until the oscillations reach an amplitude at RTC_XTAL1 of 0.9 * V_{PPX}.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) If the shaper unit is enabled and not bypassed.

Figure 17 shows typical graphs for active mode supply current for V_{DDP} = 5 V, V_{DDP} = 3.3 V, V_{DDP} = 1.8 V across different clock frequencies.



Condition:
1. TA = +25° C

Figure 17 Active mode, a) peripherals clocks enabled, b) peripherals clocks disabled: Supply current I_{DDPA} over supply voltage V_{DDP} for different clock frequencies

10) Active current is measured with: module enabled, MCLK=48 MHz, time-out mode; WLB = 0, WUB = 0x00008000; WDT serviced every 1 s

11) Active current is measured with: module enabled, MCLK=48 MHz, Periodic interrupt enabled

12) Active current is measured with: module enabled, MCLK=48 MHz, running at 20 MHz baudrate generator, 1 node activated, 1 transmit and 1 receive object active.

3.2.8 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase time per page / sector	t_{ERASE} CC	6.8	7.1	7.6	ms	
Program time per block	t_{PSER} CC	102	152	204	µs	
Wake-Up time	t_{WU} CC	–	32.2	–	µs	
Read time per word	t_a CC	–	50	–	ns	
Data Retention Time	t_{RET} CC	10	–	–	years	Max. 100 erase / program cycles
Flash Wait States [1]	$N_{WSFLASH}$ CC	0	0	0		f_{MCLK} = 8 MHz
		0	1	1		f_{MCLK} = 16 MHz
		1	2	2		f_{MCLK} = 32 MHz
		2	2	3		f_{MCLK} = 48 MHz
Erase Cycles	N_{ECYC} CC	–	–	$5*10^4$	cycles	Sum of page and sector erase cycles
Total Erase Cycles	N_{TECYC} CC	–	–	$2*10^6$	cycles	

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

3.3 AC Parameters

3.3.1 Testing Waveforms

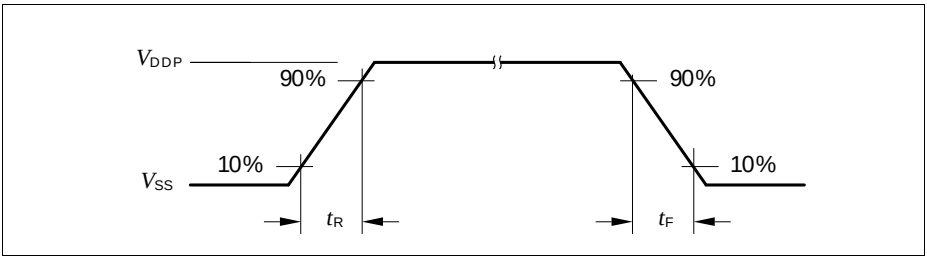


Figure 20 Rise/Fall Time Parameters

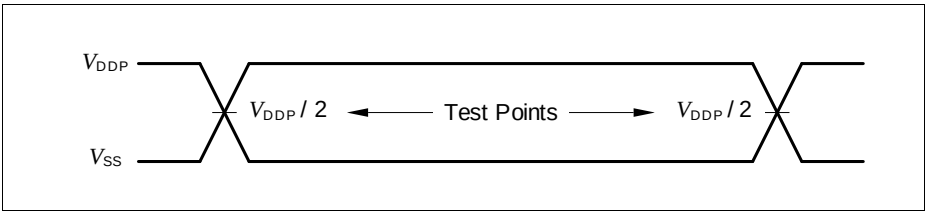


Figure 21 Testing Waveform, Output Delay

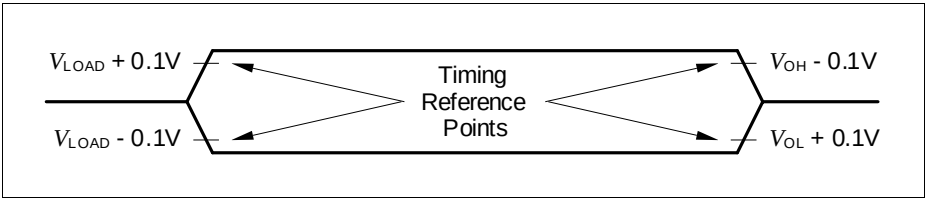


Figure 22 Testing Waveform, Output High Impedance

Table 26 Power-Up and Supply Threshold Parameters (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} brownout reset voltage	V_{DDPBO} CC	1.55	1.62	1.75	V	calibrated, before user code starts running
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	
Start-up time from power-on reset	t_{SSW} SR	–	260	–	µs	Time to the first user code instruction[3)]
BMI program time	t_{BMI} SR	–	8.25	–	ms	Time taken from a user-triggered system reset after BMI installation is is requested

1) A capacitor of at least 100 nF has to be added between V_{DDP} and V_{SSP} to fulfill the requirement as stated for this parameter.

2) Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.

3) This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 48 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

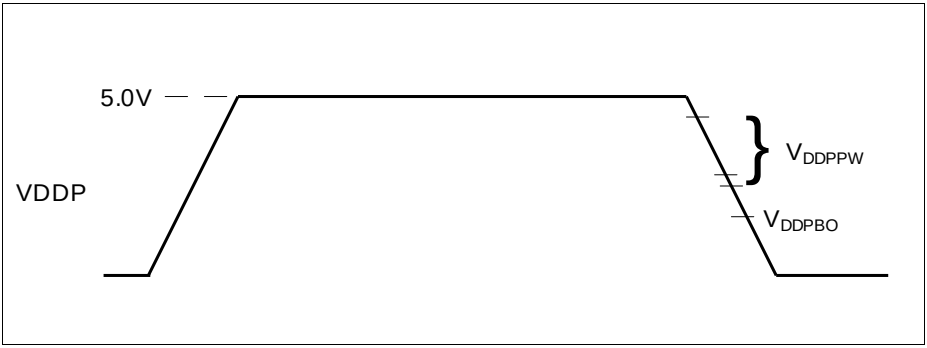


Figure 23 Supply Threshold Parameters

3.3.3 On-Chip Oscillator Characteristics

Table 27 provides the characteristics of the 96 MHz digital controlled oscillator DCO1.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 27 96 MHz DCO1 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	–	96	–	MHz	under nominal conditions[1] after trimming
Accuracy with adjustment based on XTAL as reference	Δf_{LTX}	CC	-0.3	–	0.3	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0 °C to 85 °C)
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

Table 28 provides the characteristics of the 32 kHz digital controlled oscillator DCO2.

Table 28 32 kHz DCO2 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	–	32.75	–	kHz	under nominal conditions[1] after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0 °C to 85 °C)
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)[1]

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

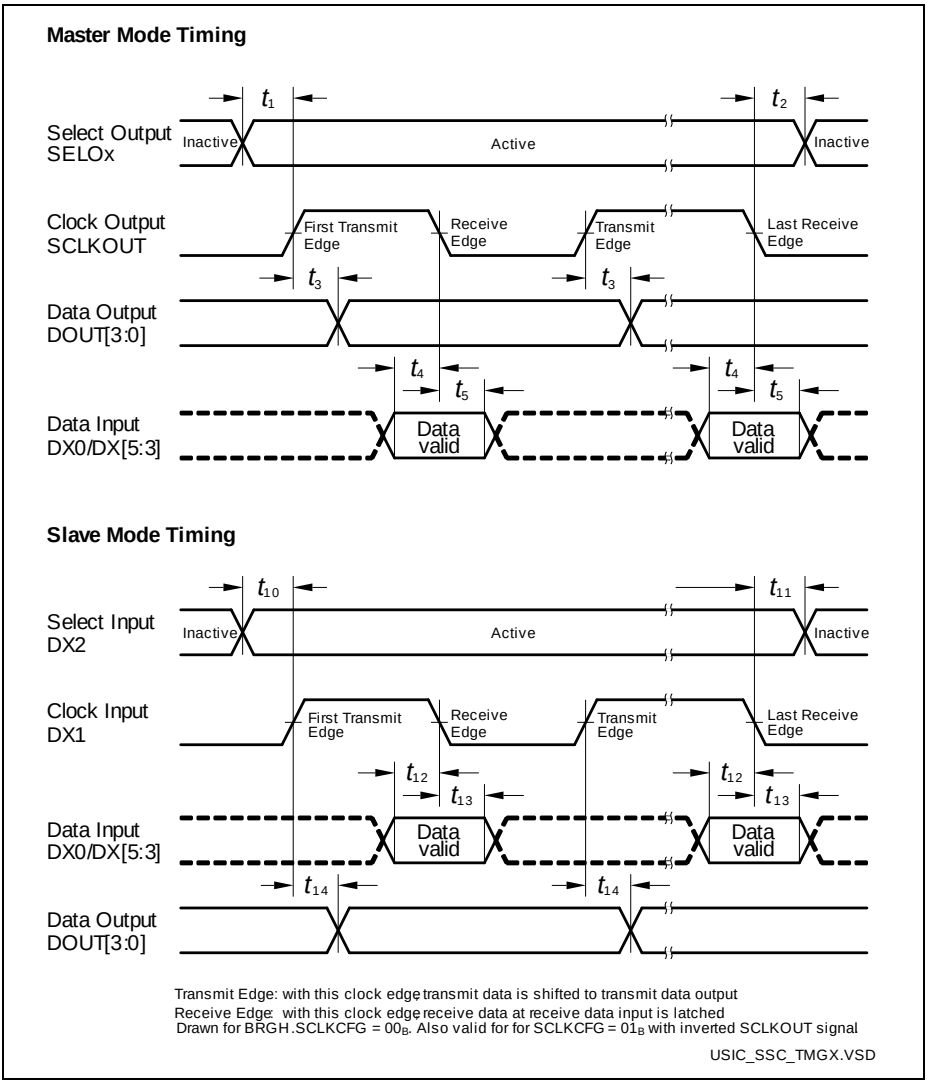


Figure 25 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

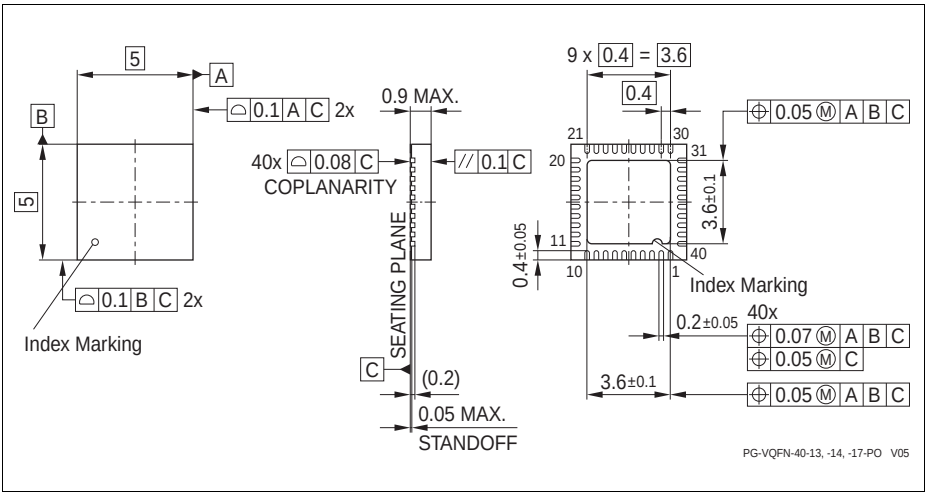


Figure 30 PG-VQFN-40-17

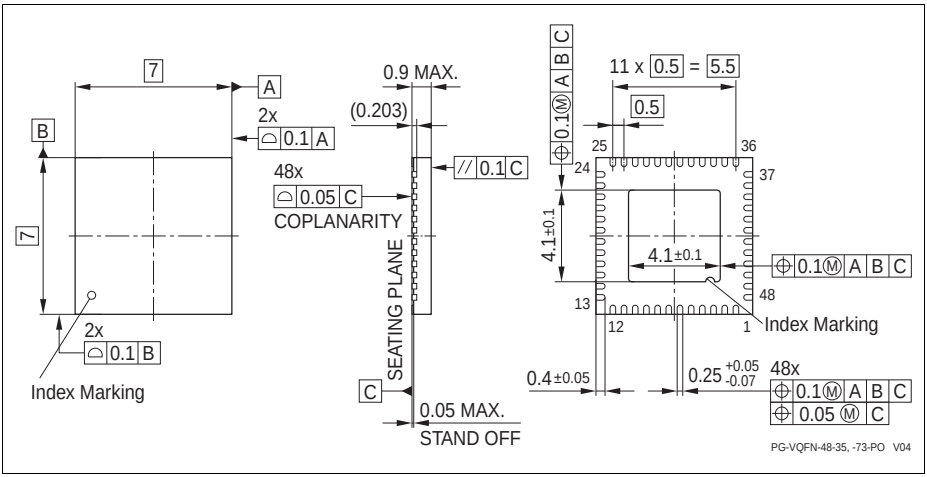


Figure 31 PG-VQFN-48-73