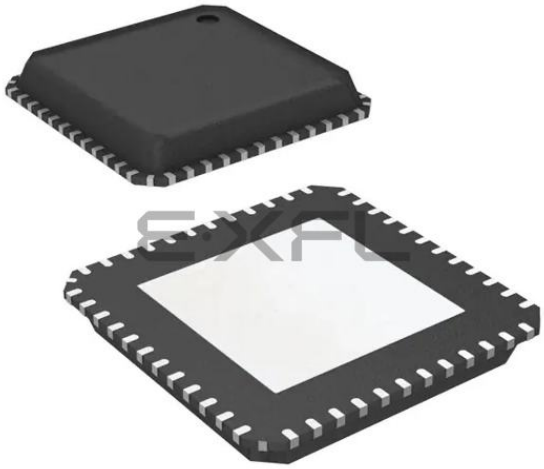
Infineon Technologies - XMC1404Q048X0200AAXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, LED, POR, PWM, WDT
Number of I/O	34
Program Memory Size	200KB (200K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-73
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1404q048x0200aaxuma1

XMC1400 AA-Step

Microcontroller Series
for Industrial Applications

XMC1000 Family

ARM® Cortex®-M0
32-bit processor core

Data Sheet

V1.3 2016-10

Microcontrollers

1 Summary of Features

The XMC1400 devices are members of the XMC1000 Family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1400 series addresses the real-time control needs of motor control and digital power conversion. It also features peripherals for LED Lighting applications and Human-Machine Interface (HMI).

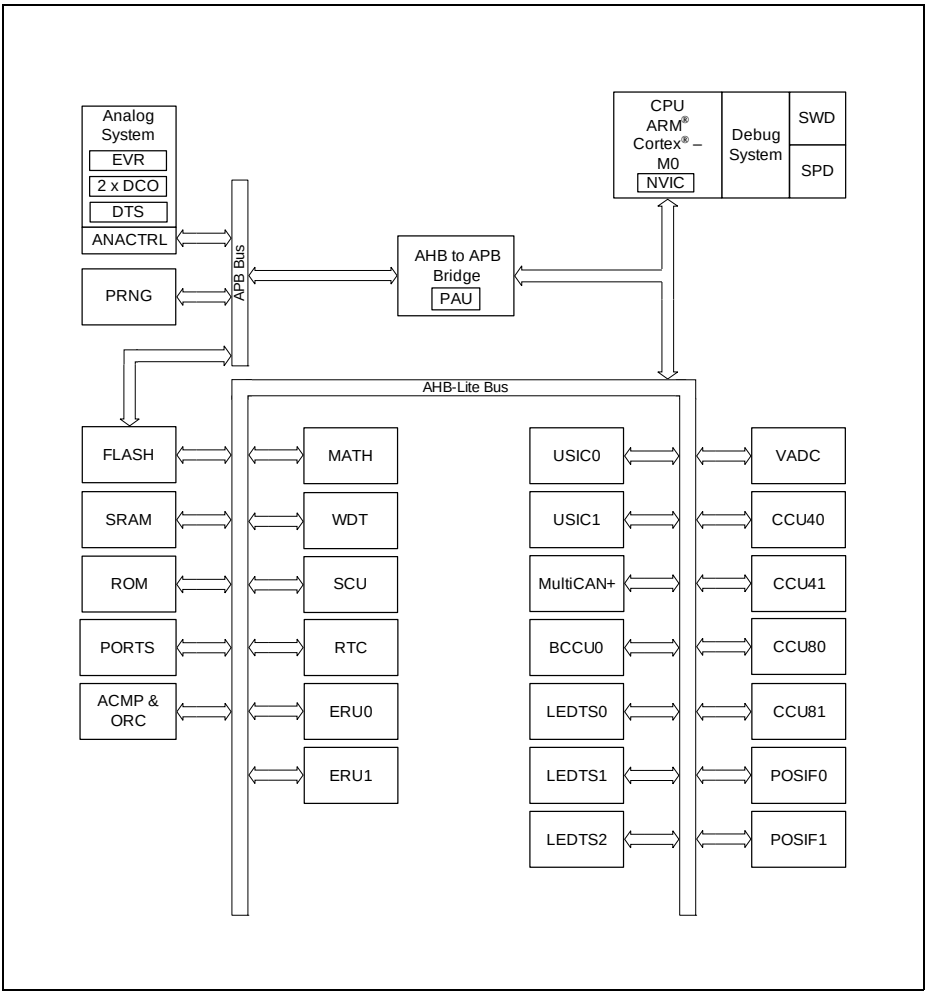


Figure 1 Block Diagram

Table 2 Synopsis of XMC1400 Device Types (cont'd)

Derivative	Package	Flash Kbytes
XMC1403-Q048X0200	PG-VQFN-48	200
XMC1403-Q064X0064	PG-VQFN-64	64
XMC1403-Q064X0128	PG-VQFN-64	128
XMC1403-Q064X0200	PG-VQFN-64	200
XMC1404-Q048X0064	PG-VQFN-48	64
XMC1404-Q048X0128	PG-VQFN-48	128
XMC1404-Q048X0200	PG-VQFN-48	200
XMC1404-Q064X0064	PG-VQFN-64	64
XMC1404-Q064X0128	PG-VQFN-64	128
XMC1404-Q064X0200	PG-VQFN-64	200
XMC1404-F064X0064	PG-LQFP-64	64
XMC1404-F064X0128	PG-LQFP-64	128
XMC1404-F064X0200	PG-LQFP-64	200

1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is an 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location : 1000 $0F00_H$ (MSB) - 1000 $0F1B_H$ (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

Table 3 XMC1400 Chip Identification Number

Derivative	Value	Marking
XMC1401-Q048F0064	00014082 07CF00FF 1E071FF7 20006000 00000D00 00001000 00011000 10204083_H	AA
XMC1401-Q048F0128	00014082 07CF00FF 1E071FF7 20006000 00000D00 00001000 00021000 10204083_H	AA
XMC1401-F064F0064	000140A2 07CF00FF 1E071FF7 20006000 00000D00 00001000 00011000 10204083_H	AA
XMC1401-F064F0128	000140A2 07CF00FF 1E071FF7 20006000 00000D00 00001000 00021000 10204083_H	AA
XMC1402-T038X0032	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00009000 10204083_H	AA
XMC1402-T038X0064	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00011000 10204083_H	AA
XMC1402-T038X0128	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00021000 10204083_H	AA
XMC1402-T038X0200	00014013 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00033000 10204083_H	AA
XMC1402-Q040X0032	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00009000 10204083_H	AA
XMC1402-Q040X0064	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00011000 10204083_H	AA
XMC1402-Q040X0128	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00021000 10204083_H	AA
XMC1402-Q040X0200	00014043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00033000 10204083_H	AA
XMC1402-Q048X0032	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00009000 10204083_H	AA

Table 3 XMC1400 Chip Identification Number (cont'd)

Derivative	Value	Marking
XMC1402-Q048X0064	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00011000 10204083_H	AA
XMC1402-Q048X0128	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00021000 10204083_H	AA
XMC1402-Q048X0200	00014083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00033000 10204083_H	AA
XMC1402-Q064X0064	00014093 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00011000 10204083_H	AA
XMC1402-Q064X0128	00014093 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00021000 10204083_H	AA
XMC1402-Q064X0200	00014093 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00033000 10204083_H	AA
XMC1402-F064X0064	000140A3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00011000 10204083_H	AA
XMC1402-F064X0128	000140A3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00021000 10204083_H	AA
XMC1402-F064X0200	000140A3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00033000 10204083_H	AA
XMC1403-Q040X0064	00014043 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00011000 10204083_H	AA
XMC1403-Q040X0128	00014043 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00021000 10204083_H	AA
XMC1403-Q040X0200	00014043 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00033000 10204083_H	AA
XMC1403-Q048X0064	00014083 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00011000 10204083_H	AA
XMC1403-Q048X0128	00014083 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00021000 10204083_H	AA
XMC1403-Q048X0200	00014083 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00033000 10204083_H	AA
XMC1403-Q064X0064	00014093 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00011000 10204083_H	AA
XMC1403-Q064X0128	00014093 07CF00FF 1E071FF7 00B00000 00000D00 00001000 00021000 10204083_H	AA

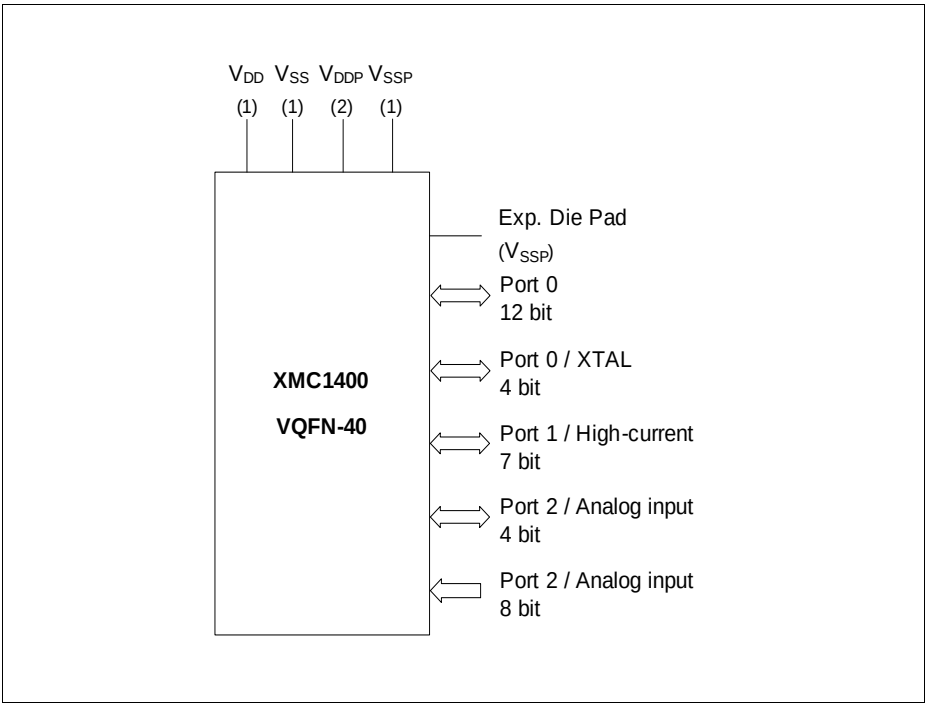


Figure 3 XMC1400 Logic Symbol for PG-VQFN-40-17

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

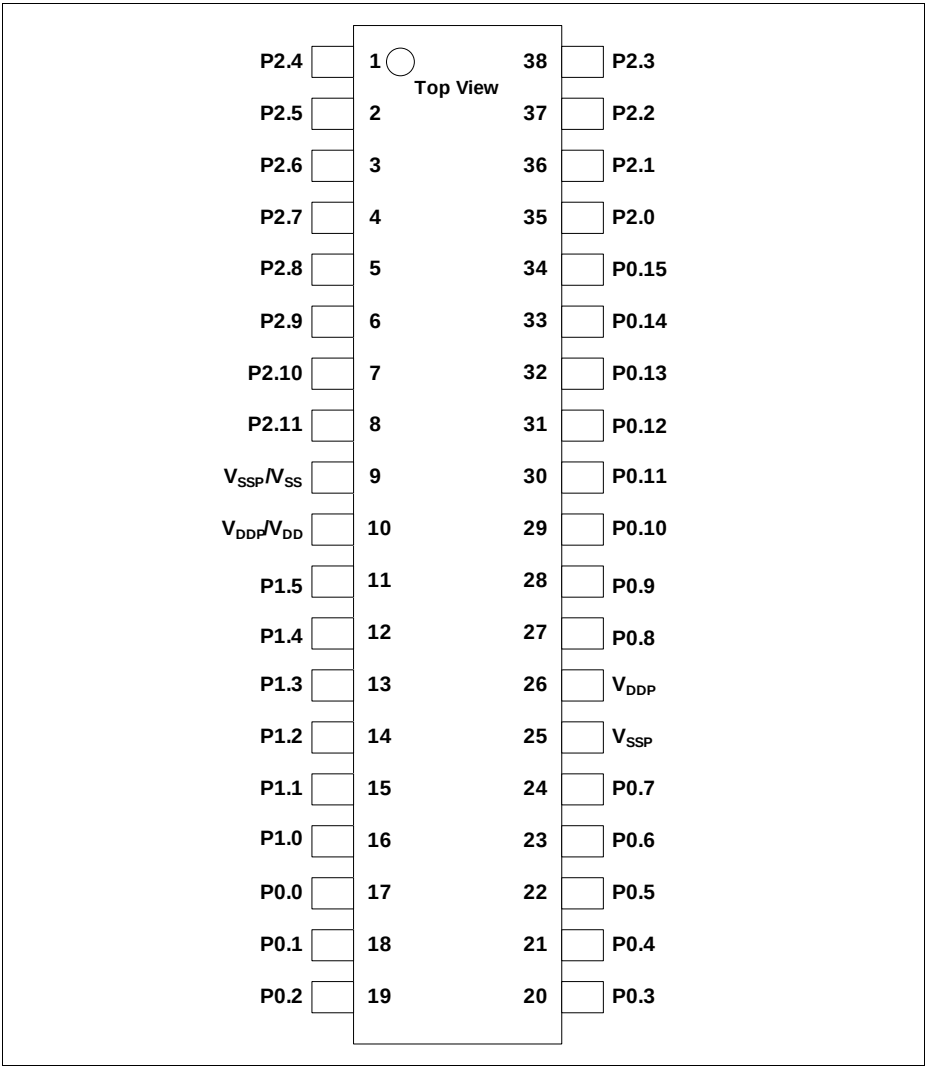


Figure 6 XMC1400 PG-TSSOP-38-9 Pin Configuration (top view)

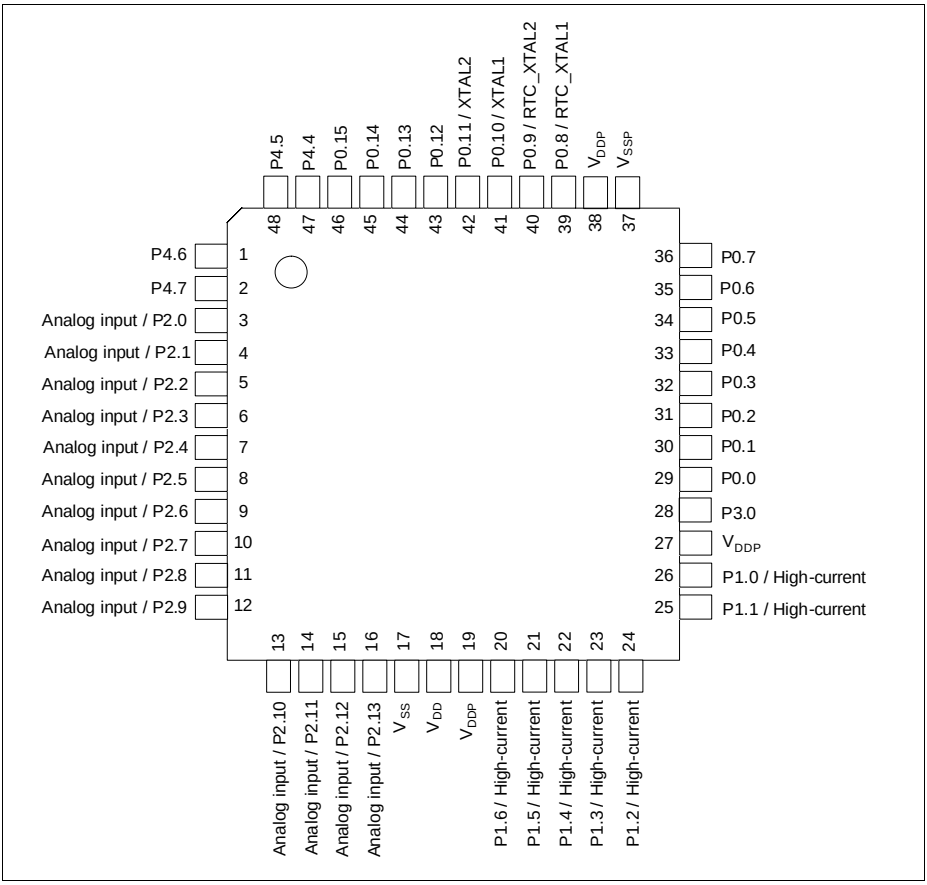


Figure 8 XMC1400 PG-VQFN-48-73 Pin Configuration (top view)

Table 5 Package Pin Mapping (cont'd)

Function	LQFP 64, VQFN 64	VQFN 48	VQFN 40	TSSOP 38	Pad Type	Notes
P0.9/ RTC_ XTAL2	52	40	34	28	STD_INOUT /clock_O	
P0.10/ XTAL1	53	41	35	29	STD_INOUT /clock_IN	
P0.11/ XTAL2	54	42	36	30	STD_INOUT /clock_O	
P0.12	55	43	37	31	STD_INOUT	
P0.13	56	44	38	32	STD_INOUT	
P0.14	57	45	39	33	STD_INOUT	
P0.15	58	46	40	34	STD_INOUT	
P1.0	34	26	22	16	High Current	
P1.1	33	25	21	15	High Current	
P1.2	32	24	20	14	High Current	
P1.3	31	23	19	13	High Current	
P1.4	30	22	18	12	High Current	
P1.5	29	21	17	11	High Current	
P1.6	28	20	16	-	High Current	
P1.7	27	-	-	-	High Current	
P1.8	26	-	-	-	STD_INOUT	
P2.0	9	3	1	35	STD_INOUT /AN	
P2.1	10	4	2	36	STD_INOUT /AN	
P2.2	11	5	3	37	STD_IN/AN	
P2.3	12	6	4	38	STD_IN/AN	
P2.4	13	7	5	1	STD_IN/AN	
P2.5	14	8	6	2	STD_IN/AN	
P2.6	15	9	7	3	STD_IN/AN	
P2.7	16	10	8	4	STD_IN/AN	

Table 10 Hardware I/O Controlled Functions

Function	Outputs	Outputs	Inputs	Inputs	Pull Control	Pull Control	Pull Control	Pull Control
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P0.0	LEDTS0. EXTENDED7		LEDTS0.TSIN7	LEDTS0.TSIN7	Reserved for LEDTS Scheme A: pull-down disabled always	Reserved for LEDTS Scheme A: pull-down enabled always	Reserved for LEDTS Scheme B: pull-up enabled and pull-down disabled, and vice versa	
P0.1	LEDTS0. EXTENDED6		LEDTS0.TSIN6	LEDTS0.TSIN6				
P0.2	LEDTS0. EXTENDED5		LEDTS0.TSIN5	LEDTS0.TSIN5				
P0.3	LEDTS0. EXTENDED4		LEDTS0.TSIN4	LEDTS0.TSIN4				
P0.4	LEDTS0. EXTENDED3		LEDTS0.TSIN3	LEDTS0.TSIN3				
P0.5	LEDTS0. EXTENDED2		LEDTS0.TSIN2	LEDTS0.TSIN2				
P0.6	LEDTS0. EXTENDED1		LEDTS0.TSIN1	LEDTS0.TSIN1				
P0.7	LEDTS0. EXTENDED0		LEDTS0.TSIN0	LEDTS0.TSIN0				
P0.8	LEDTS1. EXTENDED0		LEDTS1.TSIN0	LEDTS1.TSIN0				
P0.9	LEDTS1. EXTENDED1		LEDTS1.TSIN1	LEDTS1.TSIN1				
P0.10	LEDTS1. EXTENDED2		LEDTS1.TSIN2	LEDTS1.TSIN2				
P0.11	LEDTS1. EXTENDED3		LEDTS1.TSIN3	LEDTS1.TSIN3				
P0.12	LEDTS1. EXTENDED4		LEDTS1.TSIN4	LEDTS1.TSIN4				
P0.13	LEDTS1. EXTENDED5		LEDTS1.TSIN5	LEDTS1.TSIN5				
P0.14	LEDTS1. EXTENDED6		LEDTS1.TSIN6	LEDTS1.TSIN6				
P0.15	LEDTS1. EXTENDED7		LEDTS1.TSIN7	LEDTS1.TSIN7				
P1.0		USIC0_CH0.DOUT0		USIC0_CH0.HWIN0	$\overline{\text{BCCU0.OUT2}}$	BCCU0.OUT2		
P1.1		USIC0_CH0.DOUT1		USIC0_CH0.HWIN1	$\overline{\text{BCCU0.OUT3}}$	BCCU0.OUT3		
P1.2		USIC0_CH0.DOUT2		USIC0_CH0.HWIN2	$\overline{\text{BCCU0.OUT4}}$	BCCU0.OUT4		

Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input Hysteresis on port pin P2.3 - P2.9[8]	HYS_P2	CC	0.08 × V_{DDP}	–	V	CMOS Mode (5 V), Standard Hysteresis
			0.03 × V_{DDP}	–	V	CMOS Mode (3.3 V), Standard Hysteresis
			0.02 × V_{DDP}	–	V	CMOS Mode (2.2 V), Standard Hysteresis
			0.35 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode(5 V), Large Hysteresis
			0.25 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode(3.3 V), Large Hysteresis
			0.15 × V_{DDP}	0.65 × V_{DDP}	V	CMOS Mode(2.2 V), Large Hysteresis
Pin capacitance (digital inputs/outputs)	C_{IO}	CC	–	10	pF	
Pull-up current on port pins	I_{PUP}	CC	–	-80	µA	$V_{IH,min}$ (5 V)
			-95	–	µA	$V_{IL,max}$ (5 V)
			–	-50	µA	$V_{IH,min}$ (3.3 V)
			-65	–	µA	$V_{IL,max}$ (3.3 V)
Pull-down current on port pins	I_{PDP}	CC	–	40	µA	$V_{IL,max}$ (5 V)
			95	–	µA	$V_{IH,min}$ (5 V)
			–	30	µA	$V_{IL,max}$ (3.3 V)
			60	–	µA	$V_{IH,min}$ (3.3 V)
Input leakage current except P0.11[9]	I_{OZP}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105$ °C
Input leakage current for P0.11[9]	I_{OZP1}	CC	-10	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105$ °C
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	[10]
Maximum current per pin (excluding P1, V_{DDP} and V_{SS})	I_{MP}	SR	-10	11	mA	–
Maximum current per high currrent pins	I_{MP1A}	SR	-10	50	mA	–

Table 17 ADC Characteristics (Operating Conditions apply)[1)] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum sample rate in 8-bit mode[4)]	f_{C8} CC	–	–	f_{ADC} / 38.5	–	1 sample pending
		–	–	f_{ADC} / 54.5	–	2 samples pending
RMS noise[5)]	EN_{RMS} CC	–	1.5	–	LSB 12	DC input, SHSCFG.AREF = 00_B, GNCTRxz.GAINy = 00_B (unity gain), V_{DD} = 5.0 V, V_{AIN} = 2.5 V, 25°C
DNL error	EA_{DNL} CC	–	±2.0	–	LSB 12	
INL error	EA_{INL} CC	–	±4.0	–	LSB 12	
Gain error with external reference	EA_{GAIN} CC	–	±0.5	–	%	SHSCFG.AREF = 00_B (calibrated)
Gain error with internal reference[6)]	EA_{GAIN} CC	–	±3.6	–	%	SHSCFG.AREF = $1X_B$ (calibrated), -40°C - 110°C
		–	±2.0	–	%	SHSCFG.AREF = $1X_B$ (calibrated), 0°C - 85°C
Offset error	EA_{OFF} CC	–	±8.0	–	mV	Calibrated, V_{DD} = 5.0 V

1) The parameters are defined for ADC clock frequencies f_{SH} = 32 MHz for the full supply range, and f_{SH} = 48 MHz at V_{DD_int}, V_{DD_ext} = 5 V. Usage of any other frequencies may affect the ADC performance.

2) The alternate reference ground connection is separate for each converter. This mode, therefore, provides the lowest noise impact.

3) No pending samples assumed, excluding sampling time and calibration.

4) Includes synchronization and calibration (average of gain and offset calibration).

5) This parameter can also be defined as an SNR value: SNR[dB] = 20 × log(A_{MAXeff} / N_{RMS}).
With A_{MAXeff} = 2^N / 2, SNR[dB] = 20 × log (2048 / N_{RMS}) [N = 12].
N_{RMS} = 1.5 LSB12, therefore, equals SNR = 20 × log (2048 / 1.5) = 62.7 dB.

6) Includes error from the reference voltage.

3.2.4 Analog Comparator Characteristics

Table 19 below shows the Analog Comparator characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 19 Analog Comparator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Notes/ Test Conditions
			Min.	Typ.	Max.		
Input Voltage	V_{CMP}	SR	-0.05	–	V_{DDP} + 0.05	V	
Input Offset	V_{CMPOFF}	CC	–	+/-3	–	mV	High power mode ΔV_{CMP} < 200 mV
Propagation Delay[1)]	t_{PDELAY}	CC	–	25	–	ns	High power mode, ΔV_{CMP} = 100 mV
			–	80	–	ns	High power mode, ΔV_{CMP} = 25 mV
			–	250	–	ns	Low power mode, ΔV_{CMP} = 100 mV
			–	700	–	ns	Low power mode, ΔV_{CMP} = 25 mV
Current Consumption	I_{ACMP}	CC	–	100	–	µA	First active ACMP in high power mode, ΔV_{CMP} > 30 mV
			–	66	–	µA	Each additional ACMP in high power mode, ΔV_{CMP} > 30 mV
			–	10	–	µA	First active ACMP in low power mode
			–	6	–	µA	Each additional ACMP in low power mode
Input Hysteresis	V_{HYS}	CC	–	+/-15	–	mV	
Filter Delay[1)]	t_{FDELAY}	CC	–	5	–	ns	

1) Total Analog Comparator Delay is the sum of Propagation Delay and Filter Delay.

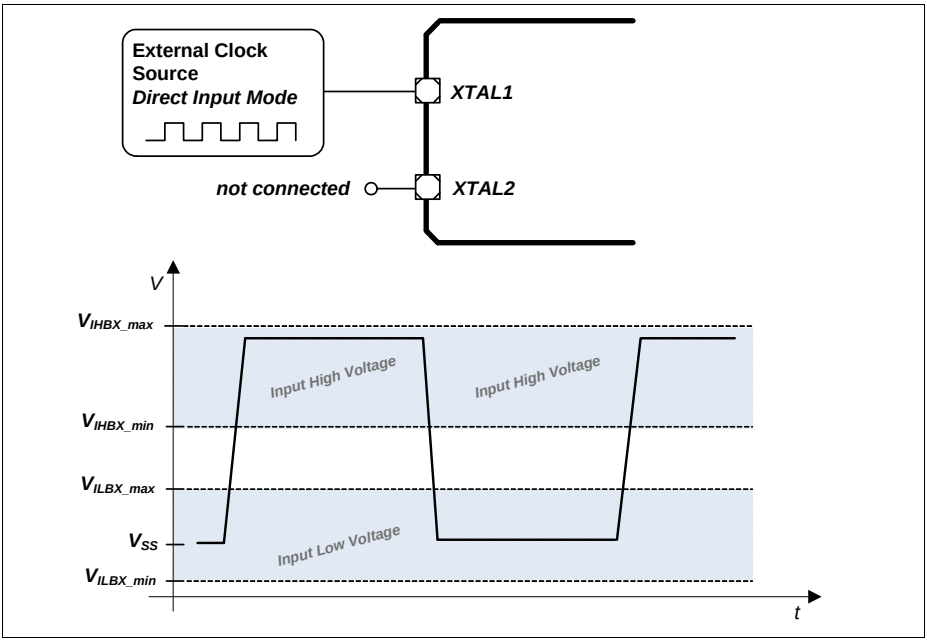


Figure 16 Oscillator in Direct Input Mode

Table 22 RTC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	–	32.768	–	kHz	
Oscillator start-up time[1)2)]	t_{OSCS} CC	–	–	5	s	
Input voltage at RTC_XTAL1	V_{IX} SR	-0.3	–	1.5	V	
Input amplitude (peak-to-peak) at RTC_XTAL1[2)3)]	V_{PPX} SR	0.2	–	1.2	V	

1) t_{OSCS} is defined from the moment the oscillator is enabled by the user with SCU_ANAOSCLPCTRL.MODE until the oscillations reach an amplitude at RTC_XTAL1 of 0.9 * V_{PPX}.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

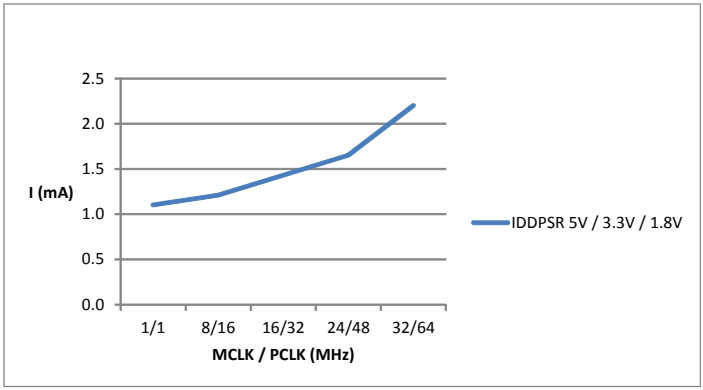
3) If the shaper unit is enabled and not bypassed.

Table 23 Power Supply parameter table; V_{DDP} = 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.[1]	Max.		
Sleep mode current Peripherals clock disabled Flash active f_{MCLK} / f_{PCLK} in MHz[5]	I_{DDPSD} CC	–	2.8	–	mA	48 / 96
		–	2.2	–	mA	24 / 48
		–	2.0	–	mA	16 / 32
		–	1.9	–	mA	8 / 16
		–	1.7	–	mA	1 / 1
Sleep mode current Peripherals clock disabled Flash powered down f_{MCLK} / f_{PCLK} in MHz[6]	I_{DDPSR} CC	–	2.2	–	mA	48 / 96
		–	1.7	–	mA	24 / 48
		–	1.4	–	mA	16 / 32
		–	1.2	–	mA	8 / 16
		–	1.1	–	mA	1 / 1
Deep Sleep mode current[7]	I_{DDPDS} CC	–	0.27	–	mA	
Wake-up time from Sleep to Active mode[8]	t_{SSA} CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode[9]	t_{DSA} CC	–	290	–	µsec	

1) The typical values are measured at T_A = + 25 °C and V_{DDP} = 5 V.
2) CPU and all peripherals clock enabled, Flash is in active mode.
3) CPU enabled, all peripherals clock disabled, Flash is in active mode.
4) CPU in sleep, all peripherals clock enabled and Flash is in active mode.
5) CPU in sleep, Flash is in active mode.
6) CPU in sleep, Flash is powered down and code executed from RAM after wake-up.
7) CPU in sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.
8) CPU in sleep, Flash is in active mode during sleep mode.
9) CPU in sleep, Flash is in powered down mode during deep sleep mode.

Figure 18 shows typical graphs for sleep mode current for V_{DDP} = 5 V, V_{DDP} = 3.3 V, V_{DDP} = 1.8 V across different clock frequencies.



Condition:
1. TA = +25° C

Figure 18 Sleep mode, peripherals clocks disabled, Flash powered down: Supply current I_{DDPSD} over supply voltage V_{DDP} for different clock frequencies

3.3.4 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 29 SWD Interface Timing Parameters(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SWDCLK high time	t_1 SR	50	–	500000	ns	–
SWDCLK low time	t_2 SR	50	–	500000	ns	–
SWDIO input setup to SWDCLK rising edge	t_3 SR	10	–	–	ns	–
SWDIO input hold after SWDCLK rising edge	t_4 SR	10	–	–	ns	–
SWDIO output valid time after SWDCLK rising edge	t_5 CC	–	–	68	ns	C_L = 50 pF
		–	–	62	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6 CC	4	–	–	ns	

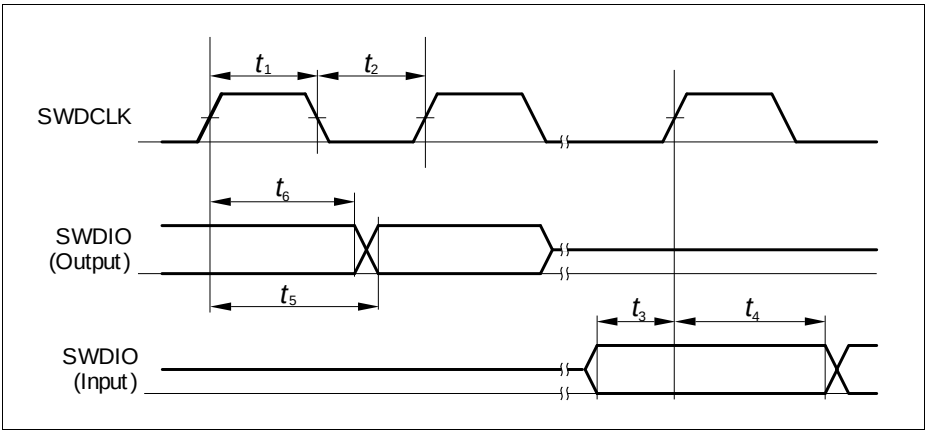


Figure 24 SWD Timing

3.3.5 SPD Timing Requirements

The optimum SPD decision time between 0_B and 1_B is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

Table 30 Optimum Number of Sample Clocks for SPD

Sample Freq.	Sampling Factor	Sample Clocks 0_B	Sample Clocks 1_B	Effective Decision Time[1)]	Remark
8 MHz	4	1 to 5	6 to 12	0.69 µs	The other closest option (0.81 µs) for the effective decision time is less robust.

1) Nominal sample frequency period multiplied with 0.5 + (max. number of 0_B sample clocks)

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers