Infineon Technologies - XMC1404Q064X0064AAXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, LED, POR, PWM, WDT
Number of I/O	48
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-64-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1404q064x0064aaxuma1

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Features

CPU subsystem

- 32-bit ARM Cortex-M0 CPU Core
  - 0.84 DMIPS/MHz (Dhrystone 2.1) at 48 MHz
- Nested Vectored Interrupt Controller
- 64 interrupt nodes
- MATH coprocessor
  - 24-bit trigonometric calculation (CORDIC)
  - 32-bit divide operation
- 2x4 channels ERU for event interconnections

On-Chip Memories

- 8 Kbyte ROM
- 16 Kbyte SRAM (with parity)
- up to 200 Kbyte Flash (with ECC)

Supply, Reset and Clock

- 1.8 V to 5.5 V supply with power on reset and brownout detector
- On-chip clock monitor
- External crystal oscillator support (32 kHz and 4 to 20 MHz)
- Internal slow and fast oscillators without the need of PLL

System Control

- Window watchdog
- Real time clock module
- Pseudo random number generator

Communication Peripherals

- Four USIC channels, usable as
  - UART (up to 12 Mb/s)
  - single-SPI (up to 12 Mb/s)
  - double-SPI (up to 2 × 12 Mb/s)
  - quad-SPI (up to 4 × 12 Mb/s)
  - IIC (up to 400 kb/s)
  - IIS (up to 12 Mb/s)
  - LIN interfaces (20kb/s)
- LEDTS in Human-Machine interface
  - up to 24 touch pads
  - drive up to 144 LEDs
- MultiCAN+, Full-CAN/Basic-CAN with 2 nodes, 32 message objects (up to 1 MBaud)

Analog Frontend Peripherals

- A/D Converters (up to 12 analog inputs)
  - 2 sample and hold stages
  - fast 12-bit ADC (up to 1.1 MS/s), adjustable gain
  - 0 V to 5.5 V input range
- Up to 8 channels out of range comparators
- Up to 4 fast analog comparators
- Temperature Sensor

Industrial Control Peripherals

- 2x4 16-bit 96 MHz CCU4 timers for signal monitoring and PWM
- 2x4 16-bit 96 MHz CCU8 timers for complex PWM, complementary high/low side switches and multi phase control
- 2x POSIF for hall and quadrature encoders, motor positioning
- 9 channel BCCU (brightness and color control) for LED lighting applications

Up to 56 Input/Output Ports

- 1.8 V to 5.5 V capable
- up to 8 high current pads (50 mA sink)

On-Chip Debug Support

- 4 breakpoints, 2 watchpoints
- ARM serial wire debug, single-pin debug interfaces

Programming Support

- Single-pin bootloader
- Secure bootstrap loader SBSL (optional)

Packages

- TSSOP-38 (9.7 × 6.4 mm^2)
- VQFN-40/48/64 (5×5/7×7/8×8 mm^2)
- LQFP-64 (12 × 12 mm^2)

Tools

- Free DAVE™ toolchain with low level drivers and apps

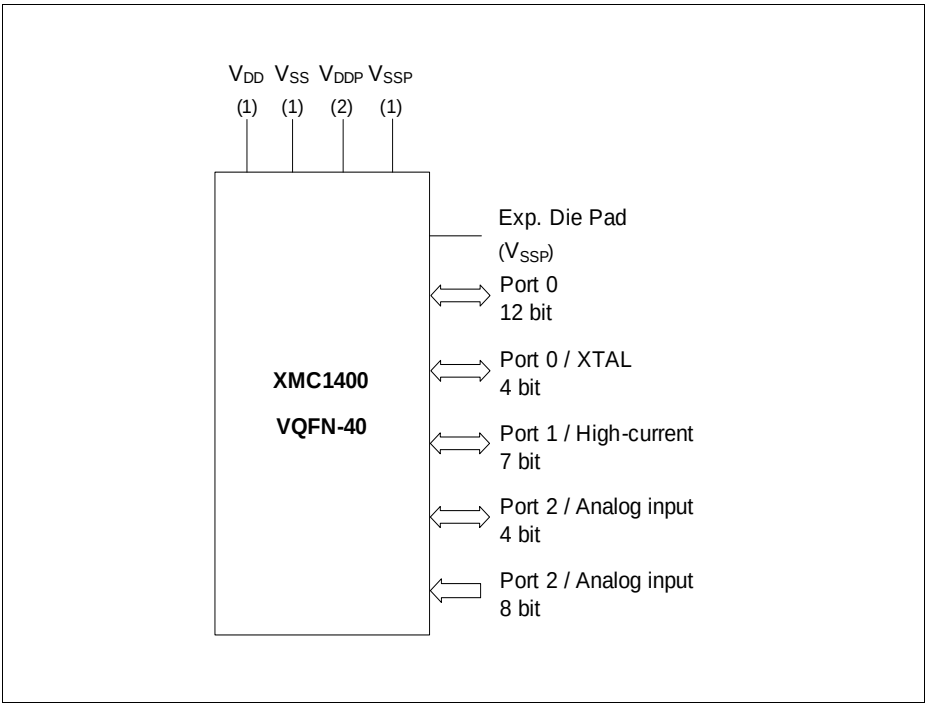


Figure 3 XMC1400 Logic Symbol for PG-VQFN-40-17

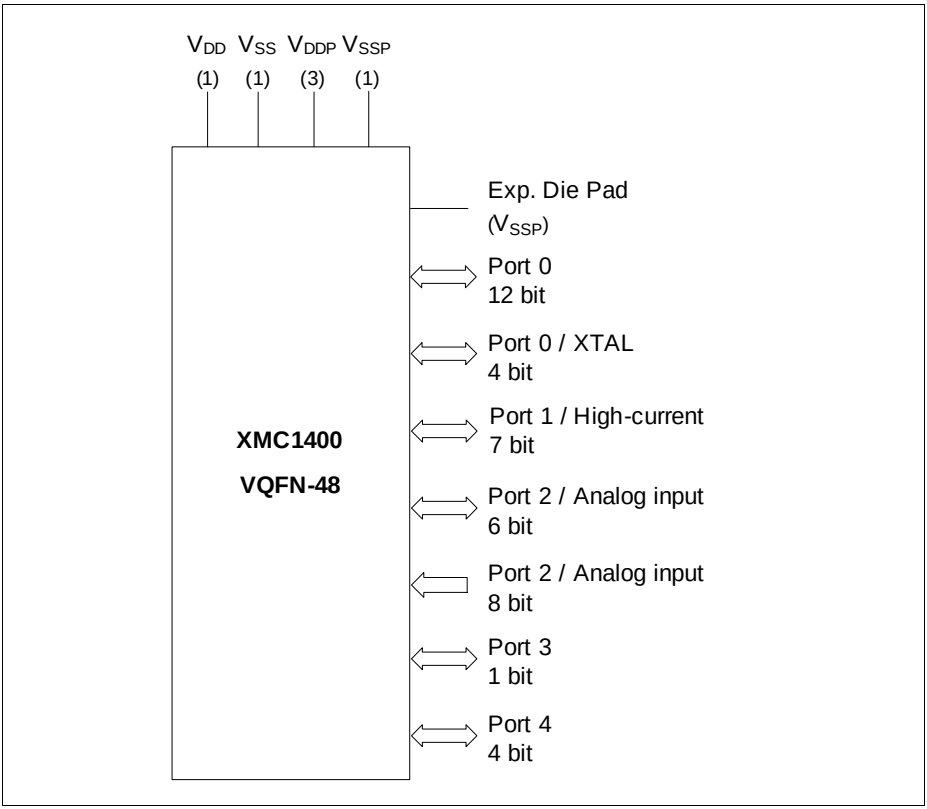


Figure 4 XMC1400 Logic Symbol for PG-VQFN-48-73

2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

Table 4 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type
Px.y	N	N		Pad Class

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type:

- STD_INOUT (standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- STD_INOUT/clock (standard bi-directional pads with oscillator function)
- High Current (high current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameter chapter.

Table 5 Package Pin Mapping

Function	LQFP 64, VQFN 64	VQFN 48	VQFN 40	TSSOP 38	Pad Type	Notes
P0.0	41	29	23	17	STD_INOUT	
P0.1	42	30	24	18	STD_INOUT	
P0.2	43	31	25	19	STD_INOUT	
P0.3	44	32	26	20	STD_INOUT	
P0.4	45	33	27	21	STD_INOUT	
P0.5	46	34	28	22	STD_INOUT	
P0.6	47	35	29	23	STD_INOUT	
P0.7	48	36	30	24	STD_INOUT	
P0.8/ RTC_ XTAL1	51	39	33	27	STD_INOUT /clock_IN	

Table 5 Package Pin Mapping (cont'd)

Function	LQFP 64, VQFN 64	VQFN 48	VQFN 40	TSSOP 38	Pad Type	Notes
VDD	24	18	14	10	Power	Supply VDD, ADC reference voltage/ ORC reference voltage
VDDP	25	19	15	10	Power	When VDD is supplied, VDDP has to be supplied with the same voltage.
VDDP	2	-	-	-	Power	I/O port supply
VDDP	35	27	-	-	Power	I/O port supply
VDDP	50	38	32	26	Power	I/O port supply
VSSP	1	-	-	-	Power	I/O port ground
VSSP	49	37	31	25	Power	I/O port ground
VSSP	Exp. Pad (in VQFN 64 only)	Exp. Pad	Exp. Pad	-	Power	**Exposed Die Pad** The exposed die pad is connected internally to VSSP. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, please refer to the Package and Reliability chapter.

2.2.2 Port Pin for Boot Modes

Port functions can be overruled by the boot mode selected. The type of boot mode is selected via BMI. **Table 6** shows the port pins used for the various boot modes.

Table 6 Port Pin for Boot Modes

Pin	Boot	Boot Description
P0.13	CS(O)	SSC BSL mode
P0.14	SWDIO_0	Debug mode (SWD)
	SPD_0	Debug mode (SPD)
	RX/TX	ASC BSL half-duplex mode
	RX	ASC BSL full-duplex mode
	RX	CAN BSL mode
	SCLK(O)	SSC BSL mode
P0.15	SWDCLK_0	Debug mode (SWD)
	TX	ASC BSL full-duplex mode
	TX	CAN BSL mode
	DATA(I/O)	SSC BSL mode
P1.2	SWDCLK_1	Debug mode (SWD)
	TX	ASC BSL full-duplex mode
	TX	CAN BSL mode
P1.3	SWDIO_1	Debug mode (SWD)
	SPD_1	Debug mode (SPD)
	RX/TX	ASC BSL half-duplex mode
	RX	ASC BSL full-duplex mode
	RX	CAN BSL mode
P4.6	HWCON0	Boot Pins (Boot from pins mode must be selected)
P4.7	HWCON1	

Table 9 Port I/O Functions (cont'd)

Function	Outputs									Inputs											
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P2.2										ACMP2.INN	VADC0.G0CH7		ORC0.AIN	USIC1_CH0.DX5E		USIC0_CH0.DX3A	USIC0_CH0.DX4A	USIC0_CH1.DX5A			ERU0.0B1
P2.3												VADC0.G1CH5	ORC1.AIN	USIC1_CH0.DX3E	USIC1_CH0.DX4E	USIC1_CH1.DX5C	USIC0_CH0.DX5B	USIC0_CH1.DX3C	USIC0_CH1.DX4C		ERU0.1B1
P2.4												VADC0.G1CH6	ORC2.AIN	USIC1_CH1.DX3C	USIC1_CH1.DX4C	USIC0_CH0.DX3B	USIC0_CH0.DX4B	USIC1_CH0.DX5F	USIC0_CH1.DX5B		ERU0.0A1
P2.5												VADC0.G1CH7	ORC3.AIN	USIC1_CH1.DX5D		USIC0_CH0.DX5D		USIC0_CH1.DX3E	USIC0_CH1.DX4E		ERU0.1A1
P2.6										ACMP1.INN	VADC0.G0CH0		ORC4.AIN	USIC1_CH1.DX3E	USIC1_CH1.DX4E	USIC0_CH0.DX3E	USIC0_CH0.DX4E	USIC0_CH1.DX5D			ERU0.2A1
P2.7										ACMP1.INP		VADC0.G1CH1	ORC5.AIN	USIC1_CH1.DX5E		USIC0_CH0.DX5C		USIC0_CH1.DX3D	USIC0_CH1.DX4D		ERU0.3A1
P2.8										ACMP0.INN	VADC0.G0CH1	VADC0.G1CH0	ORC6.AIN			USIC0_CH0.DX3D	USIC0_CH0.DX4D	USIC0_CH1.DX5C			ERU0.3B1
P2.9										ACMP0.INP	VADC0.G0CH2	VADC0.G1CH4	ORC7.AIN			USIC0_CH0.DX5A		USIC0_CH1.DX3B	USIC0_CH1.DX4B		ERU0.3B0
P2.10	ERU0.PDOUT1	CCU40.OUT2	ERU0.GOUT1	LEDTS1.COL4	CCU80.OUT30	ACMP0.OUT	USIC0_CH1.DOUT0		CAN.N1_TXD		VADC0.G0CH3	VADC0.G1CH2				USIC0_CH0.DX3C	USIC0_CH0.DX4C	USIC0_CH1.DX0F		CAN.N1_RXDE	ERU0.2B0
P2.11	ERU0.PDOUT0	CCU40.OUT3	ERU0.GOUT0	LEDTS1.COL3	CCU80.OUT31	USIC0_CH1.SCLKOUT	USIC0_CH1.DOUT0		CAN.N1_TXD	ACMP.REF	VADC0.G0CH4	VADC0.G1CH3						USIC0_CH1.DX0E	USIC0_CH1.DX1E	CAN.N1_RXDF	ERU0.2B1
P2.12	BCCU0.OUT3	VADC0.EMUX00	USIC1_CH0.SCLKOUT	USIC1_CH1.SCLKOUT		ACMP2.OUT	USIC1_CH1.DOUT0	LEDTS2.COL6		ACMP3.INN						USIC1_CH0.DX3A	USIC1_CH0.DX4A	USIC1_CH1.DX0C	USIC1_CH1.DX1B		ERU1.3A2
P2.13	BCCU0.OUT4	CCU40.OUT3	USIC1_CH0.MCLKOUT	CCU81.OUT31		VADC0.EMUX01	USIC1_CH1.DOUT0	CCU81.OUT33	CCU41.OUT3	ACMP3.INP						USIC1_CH0.DX5A		USIC1_CH1.DX0D			ERU1.3A3
P3.0	BCCU0.OUT0	USIC1_CH1.DOUT0	USIC1_CH1.SCLKOUT	LEDTS2.COLA	CCU80.OUT21	ACMP1.OUT	USIC1_CH0.SELO1	CCU81.OUT21	CCU41.OUT0	BCCU0.TRAPINC	CCU41.IN0AA	CCU41.IN1AA	CCU41.IN2AA	CCU41.IN3AA	CCU81.IN0AA	CCU81.IN1AA	CCU81.IN2AA	USIC1_CH1.DX0E	USIC1_CH1.DX1D	CCU81.IN3AA	ERU1.0A1
P3.1	BCCU0.OUT1	USIC1_CH1.DOUT0		LEDTS2.COL0	CCU80.OUT20	ACMP3.OUT	USIC1_CH0.SELO0	CCU81.OUT20	CCU41.OUT1								USIC1_CH0.DX2F	USIC1_CH1.DX0F			ERU1.1A1

Table 10 Hardware I/O Controlled Functions

Function	Outputs	Outputs	Inputs	Inputs	Pull Control	Pull Control	Pull Control	Pull Control
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P0.0	LEDTS0. EXTENDED7		LEDTS0.TSIN7	LEDTS0.TSIN7	Reserved for LEDTS Scheme A: pull-down disabled always	Reserved for LEDTS Scheme A: pull-down enabled always	Reserved for LEDTS Scheme B: pull-up enabled and pull-down disabled, and vice versa	
P0.1	LEDTS0. EXTENDED6		LEDTS0.TSIN6	LEDTS0.TSIN6				
P0.2	LEDTS0. EXTENDED5		LEDTS0.TSIN5	LEDTS0.TSIN5				
P0.3	LEDTS0. EXTENDED4		LEDTS0.TSIN4	LEDTS0.TSIN4				
P0.4	LEDTS0. EXTENDED3		LEDTS0.TSIN3	LEDTS0.TSIN3				
P0.5	LEDTS0. EXTENDED2		LEDTS0.TSIN2	LEDTS0.TSIN2				
P0.6	LEDTS0. EXTENDED1		LEDTS0.TSIN1	LEDTS0.TSIN1				
P0.7	LEDTS0. EXTENDED0		LEDTS0.TSIN0	LEDTS0.TSIN0				
P0.8	LEDTS1. EXTENDED0		LEDTS1.TSIN0	LEDTS1.TSIN0				
P0.9	LEDTS1. EXTENDED1		LEDTS1.TSIN1	LEDTS1.TSIN1				
P0.10	LEDTS1. EXTENDED2		LEDTS1.TSIN2	LEDTS1.TSIN2				
P0.11	LEDTS1. EXTENDED3		LEDTS1.TSIN3	LEDTS1.TSIN3				
P0.12	LEDTS1. EXTENDED4		LEDTS1.TSIN4	LEDTS1.TSIN4				
P0.13	LEDTS1. EXTENDED5		LEDTS1.TSIN5	LEDTS1.TSIN5				
P0.14	LEDTS1. EXTENDED6		LEDTS1.TSIN6	LEDTS1.TSIN6				
P0.15	LEDTS1. EXTENDED7		LEDTS1.TSIN7	LEDTS1.TSIN7				
P1.0		USIC0_CH0.DOUT0		USIC0_CH0.HWIN0	$\overline{\text{BCCU0.OUT2}}$	BCCU0.OUT2		
P1.1		USIC0_CH0.DOUT1		USIC0_CH0.HWIN1	$\overline{\text{BCCU0.OUT3}}$	BCCU0.OUT3		
P1.2		USIC0_CH0.DOUT2		USIC0_CH0.HWIN2	$\overline{\text{BCCU0.OUT4}}$	BCCU0.OUT4		

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 12 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels (V_{DDP})
  - temperature

If a pin current is outside of the **Operating Conditions** but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 12 Overload Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV}	SR	-5	–	5	mA	
Absolute sum of all input circuit currents during overload condition	I_{OVS}	SR	–	–	25	mA	

Figure 11 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

3.2.2 Analog to Digital Converters (ADC)

Table 17 shows the Analog to Digital Converter (ADC) characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 17 ADC Characteristics (Operating Conditions apply)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	V_{DD_int} SR	2.0	–	3.0	V	SHSCFG.AREF = 11_B; CALCTR.CALGNSTC = $0C_H$ for f_{SH} = 32 MHz, 12_H for f_{SH} = 48 MHz
		3.0	–	5.5	V	SHSCFG.AREF = 10_B
Supply voltage range (external reference)	V_{DD_ext} SR	3.0	–	5.5	V	SHSCFG.AREF = 00_B
Analog input voltage range	V_{AIN} SR	V_{SSP} - 0.05	–	V_{DDP} + 0.05	V	
Auxiliary analog reference ground[2)]	V_{REFGND} SR	V_{SSP} - 0.05	–	1.0	V	G0CH0
		V_{SSP} - 0.05	–	0.2	V	G1CH0
Internal reference voltage (full scale value)	V_{REFINT} CC	5			V	
Switched capacitance of an analog input	C_{AINS} CC	–	1.2	2	pF	GNCTRxz.GAINy = 00_B (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01_B (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10_B (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11_B (gain g3)
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	

3.2.3 Out of Range Comparator (ORC) Characteristics

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above V_{DDP} on selected input pins (ORCx.AIN) and generates a service request trigger (ORCx.OUT).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 18 Out of Range Comparator (ORC) Characteristics (Operating Conditions apply; V_{DDP} = 3.0 V - 5.5 V; C_L = 0.25pF)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC}	CC	–	–	180	mV	$V_{AIN} \geq V_{DDP} + V_{ODC}$
Hysteresis	V_{OHYS}	CC	15	–	54	mV	
Always detected Overvoltage Pulse	t_{OPDD}	CC	103	–	–	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			88	–	–	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Never detected Overvoltage Pulse	t_{OPDN}	CC	–	–	21	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			–	–	11	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Detection Delay	t_{ODD}	CC	39	–	132	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			31	–	121	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Release Delay	t_{ORD}	CC	44	–	240	ns	$V_{AIN} \leq V_{DDP}$; V_{DDP} = 5 V
			57	–	340	ns	$V_{AIN} \leq V_{DDP}$; V_{DDP} = 3.3 V
Enable Delay	t_{OED}	CC	–	–	300	ns	ORCCTRL.ENORCx = 1

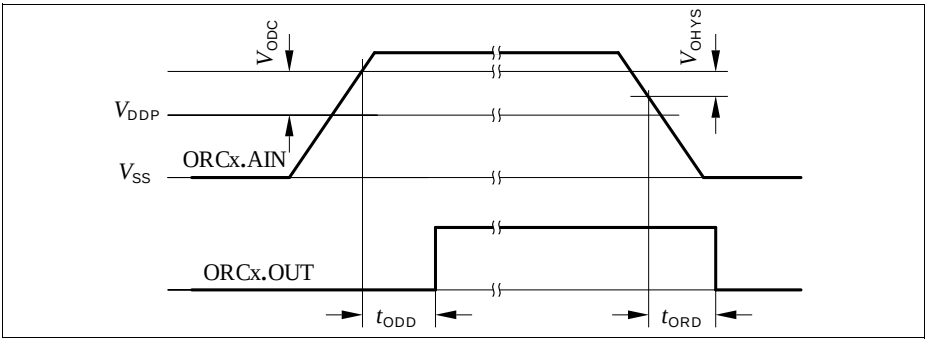


Figure 13 ORCx.OUT Trigger Generation

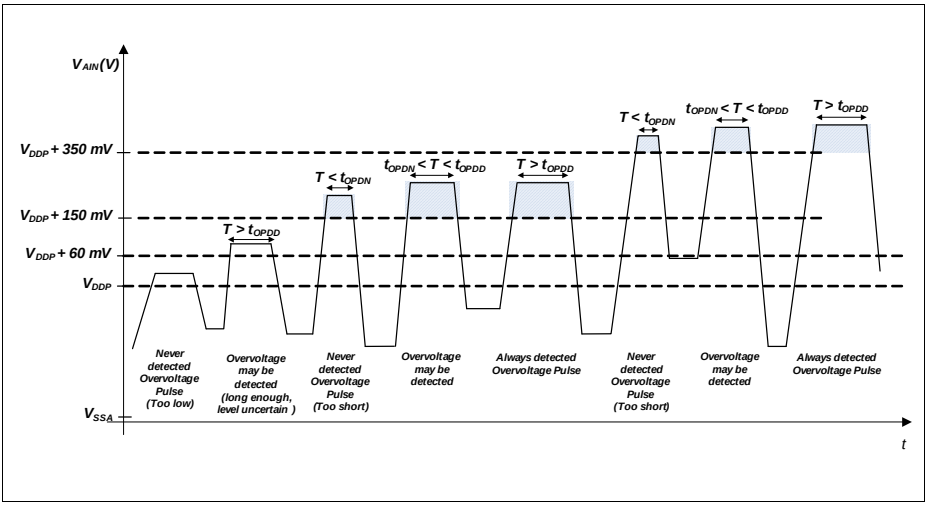
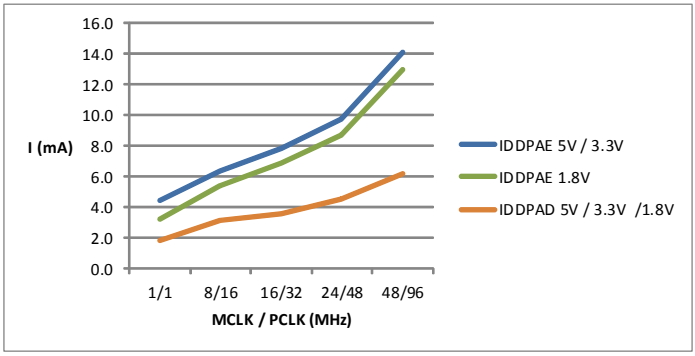


Figure 14 ORC Detection Ranges

Figure 17 shows typical graphs for active mode supply current for V_{DDP} = 5 V, V_{DDP} = 3.3 V, V_{DDP} = 1.8 V across different clock frequencies.



Condition:
1. TA = +25° C

Figure 17 Active mode, a) peripherals clocks enabled, b) peripherals clocks disabled: Supply current I_{DDPA} over supply voltage V_{DDP} for different clock frequencies

3.2.8 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase time per page / sector	t_{ERASE} CC	6.8	7.1	7.6	ms	
Program time per block	t_{PSER} CC	102	152	204	µs	
Wake-Up time	t_{WU} CC	–	32.2	–	µs	
Read time per word	t_a CC	–	50	–	ns	
Data Retention Time	t_{RET} CC	10	–	–	years	Max. 100 erase / program cycles
Flash Wait States [1]	$N_{WSFLASH}$ CC	0	0	0		f_{MCLK} = 8 MHz
		0	1	1		f_{MCLK} = 16 MHz
		1	2	2		f_{MCLK} = 32 MHz
		2	2	3		f_{MCLK} = 48 MHz
Erase Cycles	N_{ECYC} CC	–	–	$5*10^4$	cycles	Sum of page and sector erase cycles
Total Erase Cycles	N_{TECYC} CC	–	–	$2*10^6$	cycles	

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

3.3.2 Power-Up and Supply Threshold Characteristics

Table 26 provides the characteristics of the supply threshold in XMC1400.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DDP} is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 26 Power-Up and Supply Threshold Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} ramp-up time	t_{RAMPUP} SR	V_{DDP}/ $S_{VDDPrise}$	–	10^7	µs	
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	V/µs	Slope during normal operation
	S_{VDDP10} SR	0	–	10	V/µs	Slope during fast transient within +/-10% of V_{DDP}
	$S_{VDDPrise}$ SR	0	–	10	V/µs	Slope during power-on or restart after brownout event
	$S_{VDDPfall}$[1] SR	0	–	0.25	V/µs	Slope during supply falling out of the +/-10% limits[2]
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00_B
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01_B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10_B

Table 32 USIC SSC Slave Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 hold after last clock input DX1 receive edge[1]	t_{11} SR	17	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1]	t_{12} SR	21	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1]	t_{13} SR	15	–	–	ns	
Data output DOUT[3:0] valid time	t_{14} CC	-	–	71	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

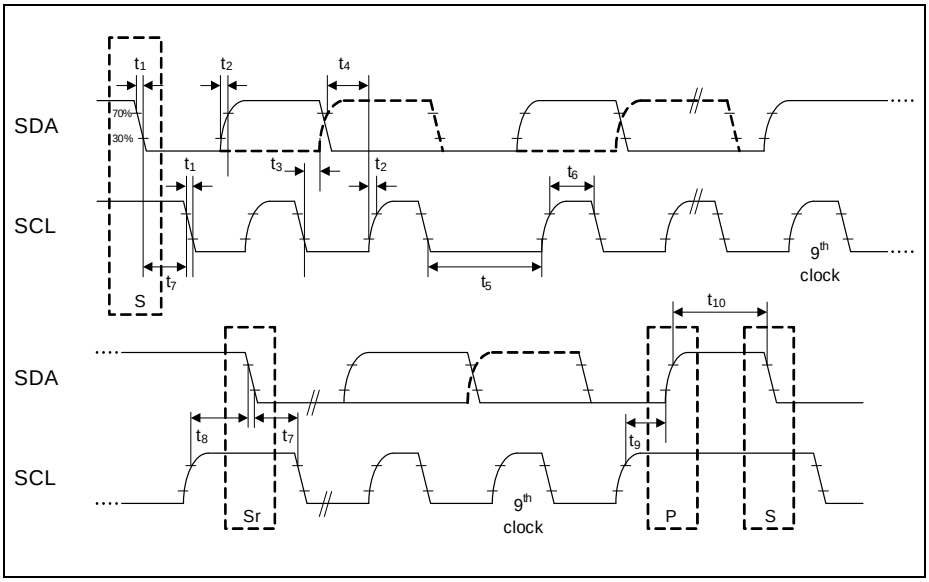


Figure 26 USIC IIC Timing

3.3.6.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: Operating Conditions apply.

Table 35 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	t_2 CC	0.35 x t_{1min}	-	-	ns	
Clock Low	t_3 CC	0.35 x t_{1min}	-	-	ns	
Hold time	t_4 CC	0	-	-	ns	
Clock rise time	t_5 CC	-	-	0.15 x t_{1min}	ns	

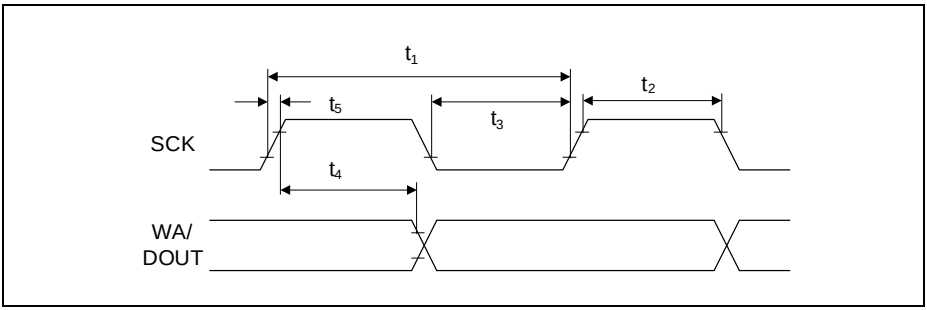


Figure 27 USIC IIS Master Transmitter Timing

Table 36 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	t_7 SR	0.35 x t_{6min}	-	-	ns	
Clock Low	t_8 SR	0.35 x t_{6min}	-	-	ns	
Set-up time	t_9 SR	0.3 x t_{6min}	-	-	ns	
Hold time	t_{10} SR	15	-	-	ns	

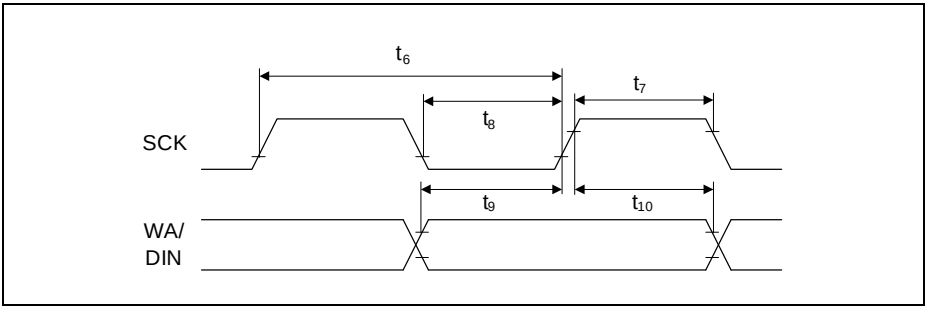


Figure 28 USIC IIS Slave Receiver Timing

4.2 Package Outlines

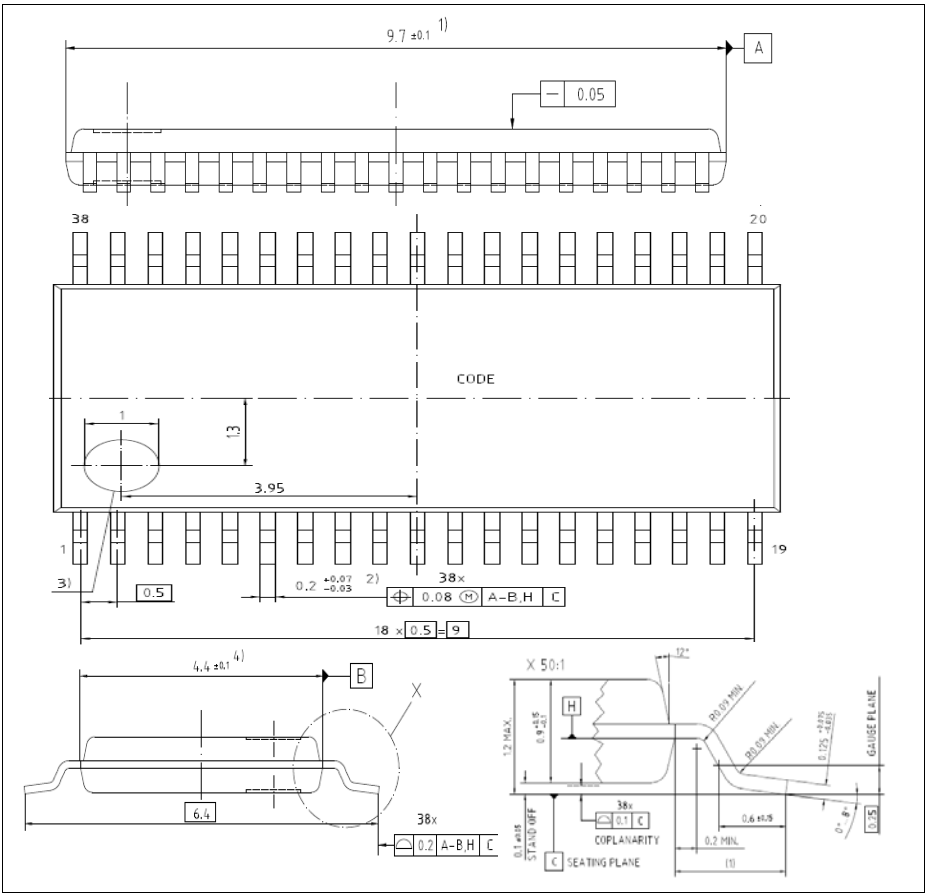


Figure 29 PG-TSSOP-38-9