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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, LCD, POR, PWM, WDT
Number of I/O	41
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 25x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l052c6t6

3.2 Central processing unit STM8

3.2.1 Advanced STM8 core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains six internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64-Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

3.2.2 Interrupt controller

The medium-density value line STM8L052C6 features a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 40 external interrupt sources on 11 vectors
- Trap and reset interrupts

3.9 Analog-to-digital converter

- 12-bit analog-to-digital converter (ADC1) with 25 channels (including 1 fast channel) and internal reference voltage
- Conversion time down to 1 μ s with $f_{\text{SYSCLK}} = 16$ MHz
- Programmable resolution
- Programmable sampling time
- Single and continuous mode of conversion
- Scan capability: automatic conversion performed on a selected group of analog inputs
- Analog watchdog
- Triggered by timer

Note: ADC1 can be served by DMA1.

3.10 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface allows application software to control the routing of different I/Os to the TIM1 timer input captures. It also controls the routing of internal analog signals to ADC1 and the internal reference voltage V_{REFINT} .

3.11 Timers

The medium-density value line STM8L052C6 contains one advanced control timer (TIM1), two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

All the timers can be served by DMA1.

[Table 2](#) compares the features of the advanced control, general-purpose and basic timers.

Table 2. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA1 request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	up/down	Any integer from 1 to 65536	Yes	3 + 1	3
TIM2			Any power of 2 from 1 to 128		2	None
TIM3						
TIM4	8-bit	up	Any power of 2 from 1 to 32768		0	

4 Pin description

Figure 3. STM8L052C6 48-pin LQFP48 package pinout (with LCD)

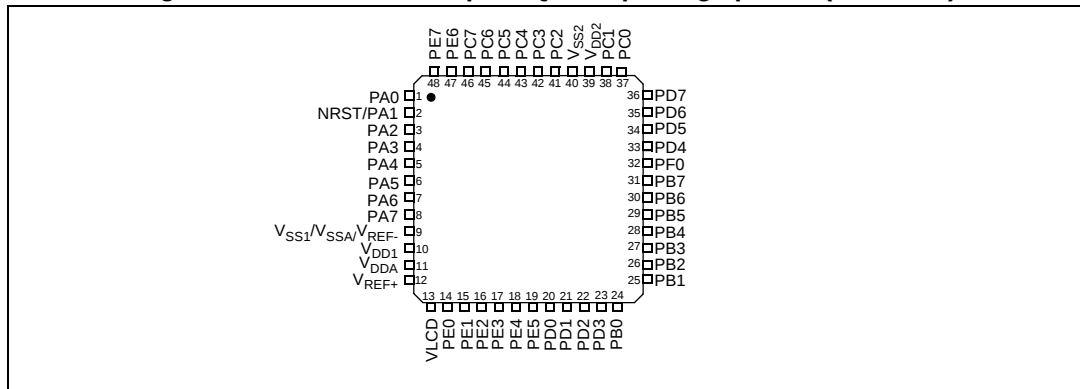


Table 3. Legend/abbreviation for Table 4

Type	I= input, O = output, S = power supply	
Level	FT	Five-volt tolerant
	TT	3.6 V tolerant
	Output	HS = high sink/source (20 mA)
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. "under reset") and after internal reset release (i.e. at reset state).	

Table 4. Medium-density value line STM8L052C6pin description

Pin #	Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
2	NRST/PA1 ⁽¹⁾	I/O			X		HS		X	Reset	PA1
3	PA2/OSC_IN/ [USART1_TX] ⁽⁸⁾ / [SPI1_MISO] ⁽⁸⁾	I/O		X	X	X	HS	X	X	Port A2	HSE oscillator input / [USART1 transmit] / [SPI1 master in- slave out]
4	PA3/OSC_OUT/[USART1_RX] ⁽⁸⁾ / [SPI1_MOSI] ⁽⁸⁾	I/O		X	X	X	HS	X	X	Port A3	HSE oscillator output / [USART1 receive] / [SPI1 master out/slave in]

Table 4. Medium-density value line STM8L052C6pin description (continued)

Pin #	Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
36	PD7/TIM1_CH1N/ LCD_SEG21/ ADC1_IN7/RTC_ALARM/V REFINT	I/O	TT ⁽²⁾	X	X	X	HS	X	X	Port D7	Timer 1 - inverted channel 1 / LCD segment 21 / ADC1_IN7 / RTC alarm / Internal voltage reference output
14	PE0 ⁽³⁾ /LCD_SEG1	I/O	FT	X	X	X	HS	X	X	Port E0	LCD segment 1
15	PE1/TIM1_CH2N/ LCD_SEG2	I/O	TT ⁽²⁾	X	X	X	HS	X	X	Port E1	Timer 1 - inverted channel 2 / LCD segment 2
16	PE2/TIM1_CH3N/ LCD_SEG3	I/O	TT ⁽²⁾	X	X	X	HS	X	X	Port E2	Timer 1 - inverted channel 3 / LCD segment 3
17	PE3/LCD_SEG4	I/O	TT ⁽²⁾	X	X	X	HS	X	X	Port E3	LCD segment 4
18	PE4/LCD_SEG5	I/O	TT ⁽²⁾	X	X	X	HS	X	X	Port E4	LCD segment 5
19	PE5/LCD_SEG6/ ADC1_IN23	I/O	TT ⁽²⁾	X	X	X	HS	X	X	Port E5	LCD segment 6 / ADC1_IN23
47	PE6/LCD_SEG26/ PVD_IN	I/O	TT ⁽²⁾	X	X	X	HS	X	X	Port E6	LCD segment 26/PVD_IN
48	PE7/LCD_SEG27	I/O	TT ⁽²⁾	X	X	X	HS	X	X	Port E7	LCD segment 27
32	PF0/ADC1_IN24	I/O		X	X	X	HS	X	X	Port F0	ADC1_IN24
13	VLCD	S									LCD booster external capacitor
13	Reserved										Reserved. Must be tied to V _{DD}
10	V _{DD}	S									Digital power supply
11	V _{DDA}	S									Analog supply voltage
12	V _{REF+}	S									ADC1 positive voltage reference
9	V _{SS1} /V _{SSA} /V _{REF-}	S									I/O ground / Analog ground voltage / ADC1 negative voltage reference
39	V _{DD2}	S									IOs supply voltage
40	V _{SS2}	S									IOs ground voltage
1	PA0 ⁽⁶⁾ /[USART1_CK] ⁽⁸⁾ / SWIM/BEEP/IR_TIM ⁽⁷⁾	I/O		X	X ⁽⁶⁾	X	HS ⁽⁷⁾	X	X	Port A0	[USART1 synchronous clock] ⁽⁸⁾ / SWIM input and out- put / Beep output / Infrared Timer output

- At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output open-drain or push-pull, not as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L15x and STM8L16x reference manual (RM0031).
- In the 3.6 V tolerant I/Os, protection diode to V_{DD} is not implemented.

Table 6. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xFF
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00

Table 7. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 501E to 0x00 5049	Reserved area (44 bytes)			
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH_PUKR	Flash program memory unprotection key register	0x00
0x00 5053		FLASH_DUKR	Data EEPROM unprotection key register	0x00
0x00 5054		FLASH_IAPSR	Flash in-application programming status register	0x00
0x00 5055 to 0x00 506F	Reserved area (27 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5070	DMA1	DMA1_GCSR	DMA1 global configuration & status register	0xFC
0x00 5071		DMA1_GIR1	DMA1 global interrupt register 1	0x00
0x00 5072 to 0x00 5074		Reserved area (3 bytes)		
0x00 5075		DMA1_C0CR	DMA1 channel 0 configuration register	0x00
0x00 5076		DMA1_C0SPR	DMA1 channel 0 status & priority register	0x00
0x00 5077		DMA1_C0NDTR	DMA1 number of data to transfer register (channel 0)	0x00
0x00 5078		DMA1_C0PARH	DMA1 peripheral address high register (channel 0)	0x52
0x00 5079		DMA1_C0PARL	DMA1 peripheral address low register (channel 0)	0x00
0x00 507A		Reserved area (1 byte)		
0x00 507B		DMA1_C0M0ARH	DMA1 memory 0 address high register (channel 0)	0x00
0x00 507C		DMA1_C0M0ARL	DMA1 memory 0 address low register (channel 0)	0x00
0x00 507D to 0x00 507E		Reserved area (2 bytes)		
0x00 507F		DMA1_C1CR	DMA1 channel 1 configuration register	0x00
0x00 5080		DMA1_C1SPR	DMA1 channel 1 status & priority register	0x00
0x00 5081		DMA1_C1NDTR	DMA1 number of data to transfer register (channel 1)	0x00
0x00 5082		DMA1_C1PARH	DMA1 peripheral address high register (channel 1)	0x52
0x00 5083		DMA1_C1PARL	DMA1 peripheral address low register (channel 1)	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5084	DMA1	Reserved area (1 byte)		
0x00 5085		DMA1_C1M0ARH	DMA1 memory 0 address high register (channel 1)	0x00
0x00 5086		DMA1_C1M0ARL	DMA1 memory 0 address low register (channel 1)	0x00
0x00 5087 0x00 5088		Reserved area (2 bytes)		
0x00 5089		DMA1_C2CR	DMA1 channel 2 configuration register	0x00
0x00 508A		DMA1_C2SPR	DMA1 channel 2 status & priority register	0x00
0x00 508B		DMA1_C2NDTR	DMA1 number of data to transfer register (channel 2)	0x00
0x00 508C		DMA1_C2PARH	DMA1 peripheral address high register (channel 2)	0x52
0x00 508D		DMA1_C2PARL	DMA1 peripheral address low register (channel 2)	0x00
0x00 508E		Reserved area (1 byte)		
0x00 508F		DMA1_C2M0ARH	DMA1 memory 0 address high register (channel 2)	0x00
0x00 5090		DMA1_C2M0ARL	DMA1 memory 0 address low register (channel 2)	0x00
0x00 5091 0x00 5092		Reserved area (2 bytes)		
0x00 5093		DMA1_C3CR	DMA1 channel 3 configuration register	0x00
0x00 5094		DMA1_C3SPR	DMA1 channel 3 status & priority register	0x00
0x00 5095		DMA1_C3NDTR	DMA1 number of data to transfer register (channel 3)	0x00
0x00 5096		DMA1_C3PARH_ C3M1ARH	DMA1 peripheral address high register (channel 3)	0x40
0x00 5097		DMA1_C3PARL_ C3M1ARL	DMA1 peripheral address low register (channel 3)	0x00
0x00 5098		Reserved area (1 byte)		
0x00 5099		DMA1_C3M0ARH	DMA1 memory 0 address high register (channel 3)	0x00
0x00 509A		DMA1_C3M0ARL	DMA1 memory 0 address low register (channel 3)	0x00
0x00 509B to 0x00 509D		Reserved area (3 bytes)		
0x00 509E		SYSCFG_RMPCR1	Remapping register 1	0x00
0x00 509F		SYSCFG_RMPCR2	Remapping register 2	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5280	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5281		TIM3_CR2	TIM3 control register 2	0x00
0x00 5282		TIM3_SMCR	TIM3 Slave mode control register	0x00
0x00 5283		TIM3_ETR	TIM3 external trigger register	0x00
0x00 5284		TIM3_DER	TIM3 DMA1 request enable register	0x00
0x00 5285		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5286		TIM3_SR1	TIM3 status register 1	0x00
0x00 5287		TIM3_SR2	TIM3 status register 2	0x00
0x00 5288		TIM3_EGR	TIM3 event generation register	0x00
0x00 5289		TIM3_CCMR1	TIM3 Capture/Compare mode register 1	0x00
0x00 528A		TIM3_CCMR2	TIM3 Capture/Compare mode register 2	0x00
0x00 528B		TIM3_CCER1	TIM3 Capture/Compare enable register 1	0x00
0x00 528C		TIM3_CNTRH	TIM3 counter high	0x00
0x00 528D		TIM3_CNTRL	TIM3 counter low	0x00
0x00 528E		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 528F		TIM3_ARRH	TIM3 Auto-reload register high	0xFF
0x00 5290		TIM3_ARRL	TIM3 Auto-reload register low	0xFF
0x00 5291		TIM3_CCR1H	TIM3 Capture/Compare register 1 high	0x00
0x00 5292		TIM3_CCR1L	TIM3 Capture/Compare register 1 low	0x00
0x00 5293		TIM3_CCR2H	TIM3 Capture/Compare register 2 high	0x00
0x00 5294		TIM3_CCR2L	TIM3 Capture/Compare register 2 low	0x00
0x00 5295		TIM3_BKR	TIM3 break register	0x00
0x00 5296		TIM3_OISR	TIM3 output idle state register	0x00
0x00 5297 to 0x00 52AF	Reserved area (25 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52B0	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 52B1		TIM1_CR2	TIM1 control register 2	0x00
0x00 52B2		TIM1_SMCR	TIM1 Slave mode control register	0x00
0x00 52B3		TIM1_ETR	TIM1 external trigger register	0x00
0x00 52B4		TIM1_DER	TIM1 DMA1 request enable register	0x00
0x00 52B5		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 52B6		TIM1_SR1	TIM1 status register 1	0x00
0x00 52B7		TIM1_SR2	TIM1 status register 2	0x00
0x00 52B8		TIM1_EGR	TIM1 event generation register	0x00
0x00 52B9		TIM1_CCMR1	TIM1 Capture/Compare mode register 1	0x00
0x00 52BA		TIM1_CCMR2	TIM1 Capture/Compare mode register 2	0x00
0x00 52BB		TIM1_CCMR3	TIM1 Capture/Compare mode register 3	0x00
0x00 52BC		TIM1_CCMR4	TIM1 Capture/Compare mode register 4	0x00
0x00 52BD		TIM1_CCER1	TIM1 Capture/Compare enable register 1	0x00
0x00 52BE		TIM1_CCER2	TIM1 Capture/Compare enable register 2	0x00
0x00 52BF		TIM1_CNTRH	TIM1 counter high	0x00
0x00 52C0		TIM1_CNTRL	TIM1 counter low	0x00
0x00 52C1		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 52C2		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 52C3		TIM1_ARRH	TIM1 Auto-reload register high	0xFF
0x00 52C4		TIM1_ARRL	TIM1 Auto-reload register low	0xFF
0x00 52C5		TIM1_RCR	TIM1 Repetition counter register	0x00
0x00 52C6		TIM1_CCR1H	TIM1 Capture/Compare register 1 high	0x00
0x00 52C7		TIM1_CCR1L	TIM1 Capture/Compare register 1 low	0x00
0x00 52C8		TIM1_CCR2H	TIM1 Capture/Compare register 2 high	0x00
0x00 52C9		TIM1_CCR2L	TIM1 Capture/Compare register 2 low	0x00
0x00 52CA		TIM1_CCR3H	TIM1 Capture/Compare register 3 high	0x00
0x00 52CB		TIM1_CCR3L	TIM1 Capture/Compare register 3 low	0x00
0x00 52CC		TIM1_CCR4H	TIM1 Capture/Compare register 4 high	0x00
0x00 52CD		TIM1_CCR4L	TIM1 Capture/Compare register 4 low	0x00
0x00 52CE		TIM1_BKR	TIM1 break register	0x00
0x00 52CF		TIM1_DTR	TIM1 dead-time register	0x00
0x00 52D0		TIM1_OISR	TIM1 output idle state register	0x00
0x00 52D1		TIM1_DCR1	DMA1 control register 1	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52D2	TIM1	TIM1_DCR2	TIM1 DMA1 control register 2	0x00
0x00 52D3		TIM1_DMA1R	TIM1 DMA1 address for burst mode	0x00
0x00 52D4 to 0x00 52DF	Reserved area (12 bytes)			
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_DER	TIM4 DMA1 request enable register	0x00
0x00 52E4		TIM4_IER	TIM4 Interrupt enable register	0x00
0x00 52E5		TIM4_SR1	TIM4 status register 1	0x00
0x00 52E6		TIM4_EGR	TIM4 Event generation register	0x00
0x00 52E7		TIM4_CNTR	TIM4 counter	0x00
0x00 52E8		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E9		TIM4_ARR	TIM4 Auto-reload register	0x00
0x00 52EA to 0x00 52FE	Reserved area (21 bytes)			
0x00 52FF	IRTIM	IR_CR	Infrared control register	0x00
0x00 5300 to 0x00 533F	Reserved area (64 bytes)			

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option bytes can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See [Table 10](#) for details on option byte addresses.

The option bytes can also be modified 'on the fly' by the application in IAP mode, except for the ROP and UBC values which can only be taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8L05x/15x Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0470) for information on SWIM programming procedures.

Table 10. Option byte addresses

Address	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0xAA
0x00 4802	UBC (User Boot code size)	OPT1	UBC[7:0]								0x00
0x00 4807	Reserved									0x00	
0x00 4808	Independent watchdog option	OPT3 [3:0]	Reserved				WWDG_HALT	WWDG_HW	IWDG_HALT	IWDG_HW	0x00
0x00 4809	Number of stabilization clock cycles for HSE and LSE oscillators	OPT4	Reserved				LSECNT[1:0]		HSECNT[1:0]		0x00
0x00 480A	Brownout reset (BOR)	OPT5 [3:0]	Reserved				BOR_TH			BOR_ON	0x00
0x00 480B	Bootloader option bytes (OPTBL)	OPTBL [15:0]	OPTBL[15:0]								0x00
0x00 480C											0x00

8.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A .

8.3.1 General operating conditions

Table 15. General operating conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
$f_{\text{SYSCLK}}^{(1)}$	System clock frequency	$1.8 \text{ V} \leq V_{DD} < 3.6 \text{ V}$	0	16	MHz
V_{DD}	Standard operating voltage	-	1.8	3.6	V
V_{DDA}	Analog operating voltage	Must be at the same potential as V_{DD}	1.8	3.6	V
$P_D^{(2)}$	Power dissipation at $T_A = 85^\circ\text{C}$	LQFP48	-	288	mW
$P_D^{(3)}$	Power dissipation at $T_A = 85^\circ\text{C}$	TSSOP20	-	181	mW
T_A	Temperature range	$1.8 \text{ V} \leq V_{DD} < 3.6 \text{ V}$	-40	85	$^\circ\text{C}$
T_J	Junction temperature range	$-40^\circ\text{C} \leq T_A < 85^\circ\text{C}$	-40	105 ⁽⁴⁾	$^\circ\text{C}$

1. $f_{\text{SYSCLK}} = f_{\text{CPU}}$

2. To calculate $P_{D\text{max}}(T_A)$, use the formula $P_{D\text{max}} = (T_{J\text{max}} - T_A) / \Theta_{JA}$ with $T_{J\text{max}}$ in this table and Θ_{JA} in "Thermal characteristics" table.

3. To calculate $P_{D\text{max}}(T_A)$, use the formula $P_{D\text{max}} = (T_{J\text{max}} - T_A) / \Theta_{JA}$ with $T_{J\text{max}}$ in this table and Θ_{JA} in "Thermal characteristics" table.

4. $T_{J\text{max}}$ is given by the test limit. Above this value, the product behavior is not guaranteed.

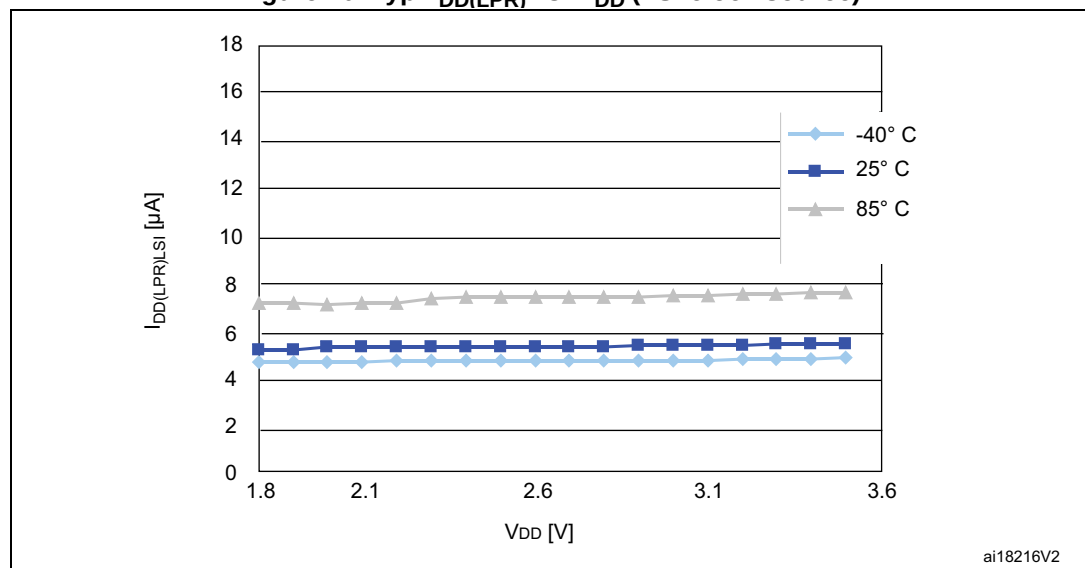
In the following table, data is based on characterization results, unless otherwise specified.

Table 19. Total current consumption and timing in Low power run mode at $V_{DD} = 1.8\text{ V}$ to 3.6 V

Symbol	Parameter	Conditions ⁽¹⁾			Typ	Max	Unit
$I_{DD(LPR)}$	Supply current in Low power run mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	5.1	5.4	μA
				$T_A = 55\text{ }^{\circ}\text{C}$	5.7	6	
				$T_A = 85\text{ }^{\circ}\text{C}$	6.8	7.5	
			with TIM2 active ⁽²⁾	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	5.4	5.7	
				$T_A = 55\text{ }^{\circ}\text{C}$	6.0	6.3	
				$T_A = 85\text{ }^{\circ}\text{C}$	7.2	7.8	
		LSE ⁽³⁾ external clock (32.768 kHz)	all peripherals OFF	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	5.25	5.6	
				$T_A = 55\text{ }^{\circ}\text{C}$	5.67	6.1	
				$T_A = 85\text{ }^{\circ}\text{C}$	5.85	6.3	
			with TIM2 active ⁽²⁾	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	5.59	6	
				$T_A = 55\text{ }^{\circ}\text{C}$	6.10	6.4	
				$T_A = 85\text{ }^{\circ}\text{C}$	6.30	7	

1. No floating I/Os
2. Timer 2 clock enabled and counter running
3. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\text{ LSE}}$) must be added. Refer to [Table 29](#)

Figure 10. Typ. $I_{DD(LPR)}$ vs. V_{DD} (LSI clock source)



LSE crystal/ceramic resonator oscillator

The LSE clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 29. LSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low speed external oscillator frequency	-	-	32.768	-	kHz
R_F	Feedback resistor	$\Delta V = 200$ mV	-	1.2	-	M Ω
$C^{(1)}$	Recommended load capacitance ⁽²⁾	-	-	8	-	pF
$I_{DD(LSE)}$	LSE oscillator power consumption	-	-	-	1.4 ⁽³⁾	μ A
		$V_{DD} = 1.8$ V	-	450	-	nA
		$V_{DD} = 3$ V	-	600	-	
		$V_{DD} = 3.6$ V	-	750	-	
g_m	Oscillator transconductance	-	3 ⁽³⁾	-	-	μ A/V
$t_{SU(LSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	s

1. $C=C_{L1}=C_{L2}$ is approximately equivalent to $2 \times$ crystal C_{LOAD} .
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with a small R_m value. Refer to crystal manufacturer for more details.
3. Data guaranteed by Design. Not tested in production.
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 13. LSE oscillator circuit diagram

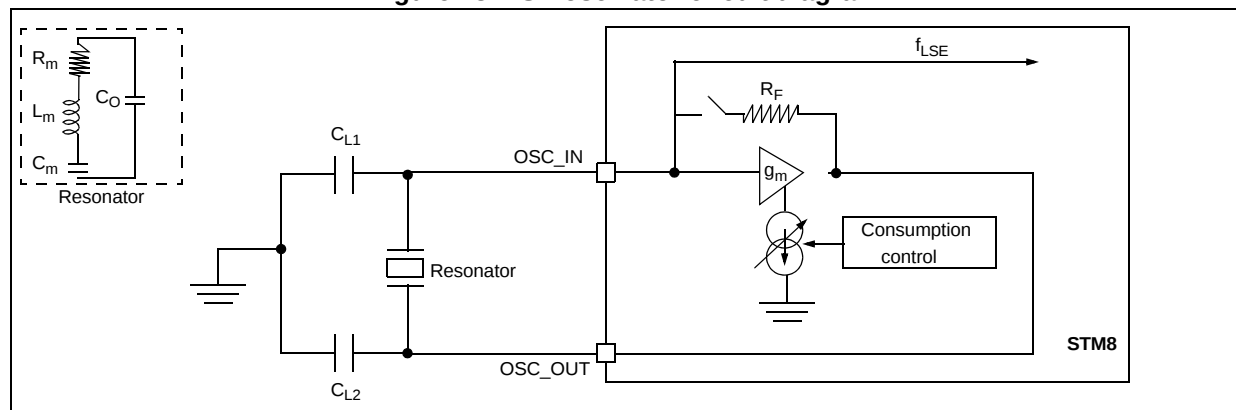


Figure 16. Typical V_{IL} and V_{IH} vs. V_{DD} (high sink I/Os)

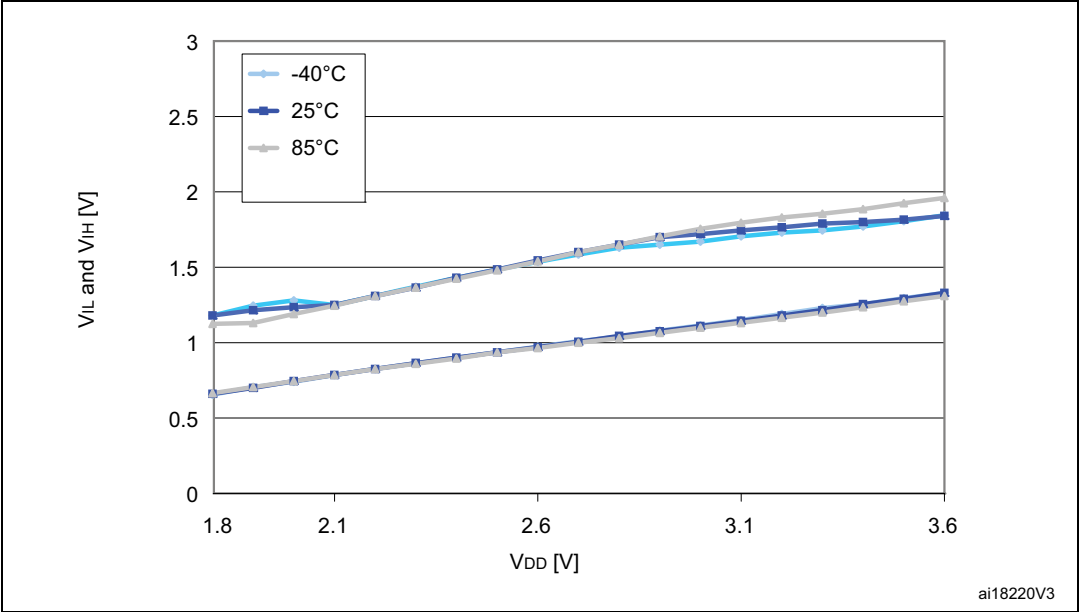
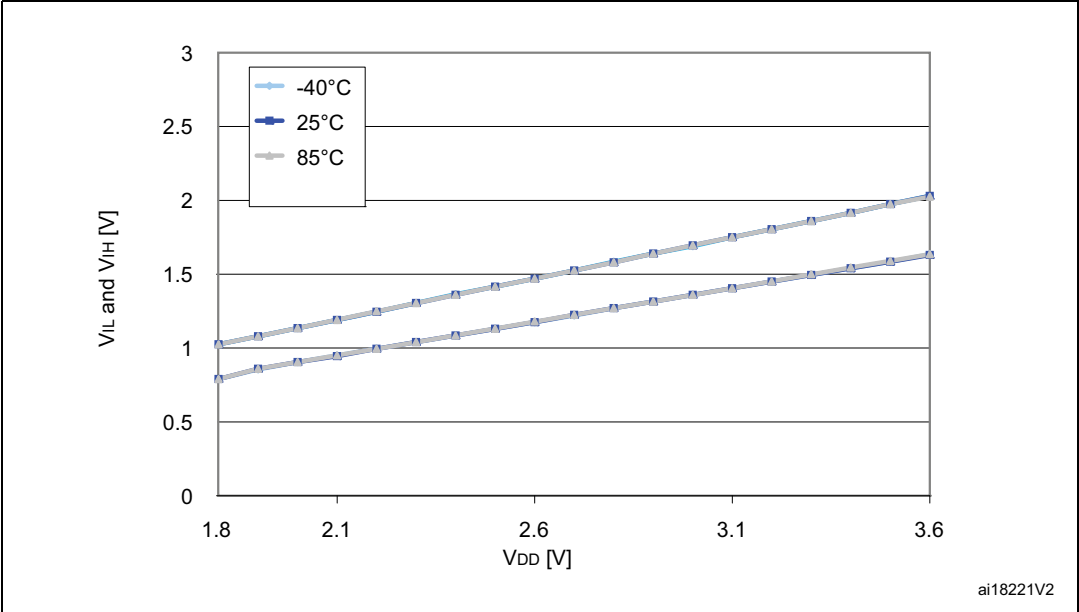


Figure 17. Typical V_{IL} and V_{IH} vs. V_{DD} (true open drain I/Os)



8.3.10 Embedded reference voltage

In the following table, data is based on characterization results, not tested in production, unless otherwise specified.

Table 43. Reference voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max.	Unit
I_{REFINT}	Internal reference voltage consumption	-	-	1.4	-	μA
$T_{S_VREFINT}^{(1)(2)}$	ADC sampling time when reading the internal reference voltage	-	-	5	10	μs
$I_{BUF}^{(2)}$	Internal reference voltage buffer consumption (used for ADC)	-	-	13.5	25	μA
$V_{REFINT\ out}$	Reference voltage output	-	1.202 ⁽³⁾	1.224	1.242 ⁽³⁾	V
$I_{LPBUF}^{(2)}$	Internal reference voltage low power buffer consumption	-	-	730	1200	nA
$I_{REFOUT}^{(2)}$	Buffer output current ⁽⁴⁾	-	-	-	1	μA
C_{REFOUT}	Reference voltage output load	-	-	-	50	pF
$t_{VREFINT}$	Internal reference voltage startup time	-	-	2	3	ms
$t_{BUFEN}^{(2)}$	Internal reference voltage buffer startup time once enabled ⁽¹⁾	-	-	-	10	μs
$ACC_{VREFINT}$	Accuracy of V_{REFINT} stored in the $VREFINT_Factory_CONV$ byte ⁽⁵⁾	-	-	-	± 5	mV
$STAB_{VREFINT}$	Stability of V_{REFINT} over temperature	$-40\ ^\circ C \leq T_A \leq 85\ ^\circ C$	-	20	50	ppm/ $^\circ C$
	Stability of V_{REFINT} over temperature	$0\ ^\circ C \leq T_A \leq 50\ ^\circ C$	-	-	20	ppm/ $^\circ C$
$STAB_{VREFINT}$	Stability of V_{REFINT} after 1000 hours	-	-	-	TBD	ppm

1. Defined when ADC output reaches its final value $\pm 1/2LSB$

2. Data guaranteed by Design. Not tested in production.

3. Tested in production at $V_{DD} = 3\ V \pm 10\ mV$.

4. To guaranty less than 1% V_{REFOUT} deviation.

5. Measured at $V_{DD} = 3\ V \pm 10\ mV$. This value takes into account V_{DD} accuracy and ADC conversion accuracy.

Figure 33. ADC1 accuracy characteristics

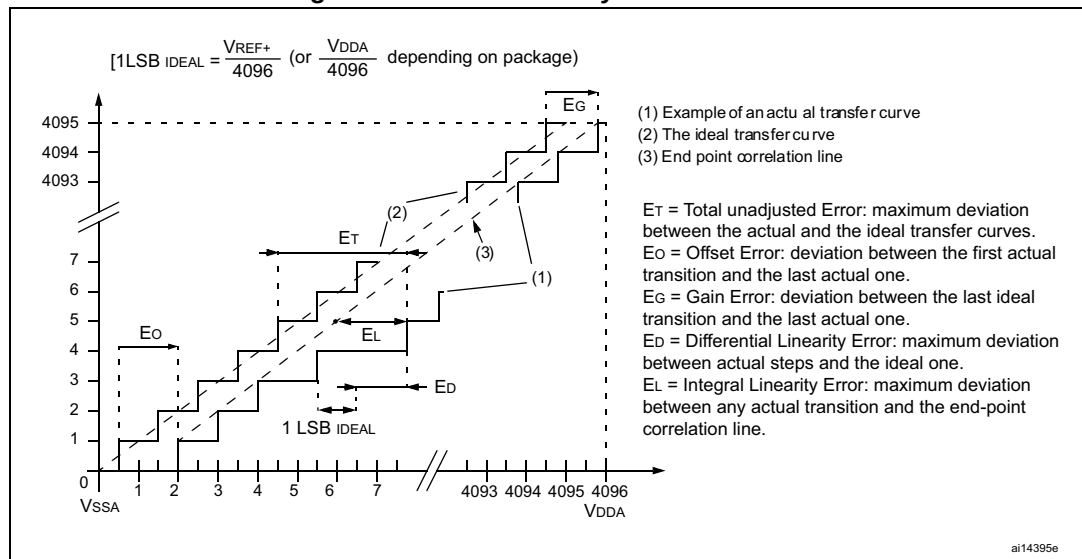
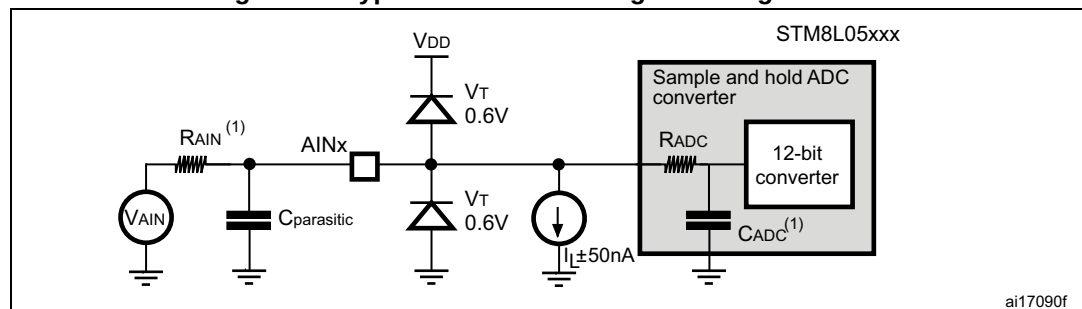


Figure 34. Typical connection diagram using the ADC

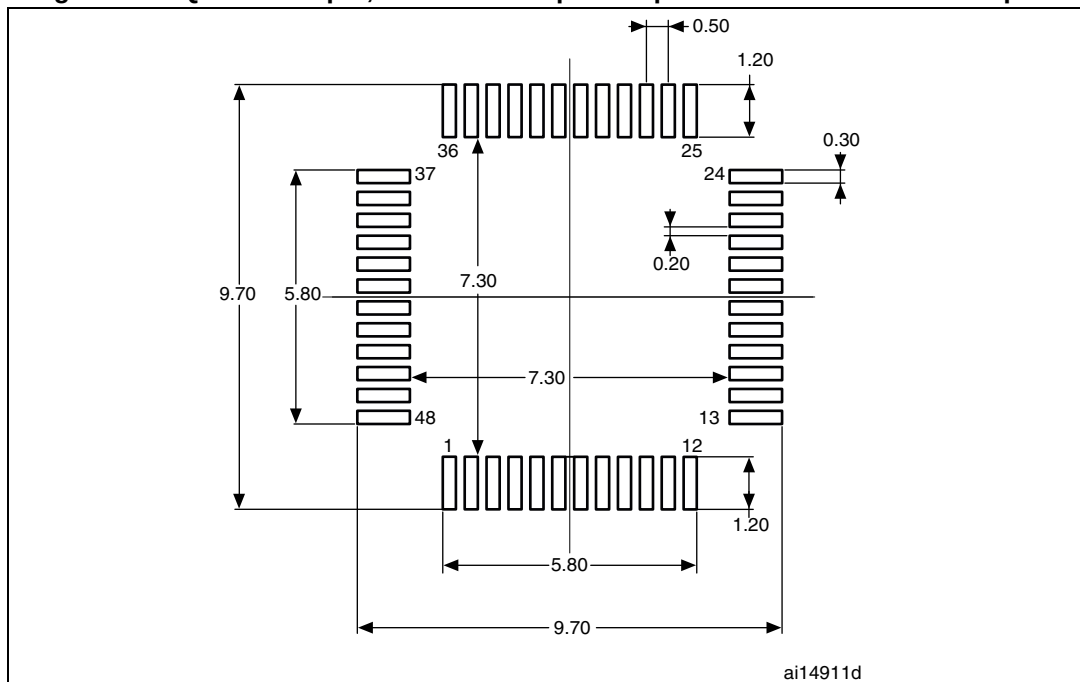


1. Refer to [Table 44](#) for the values of R_{AIN} and C_{ADC} .
2. $C_{\text{parasitic}}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{\text{parasitic}}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

Table 53. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

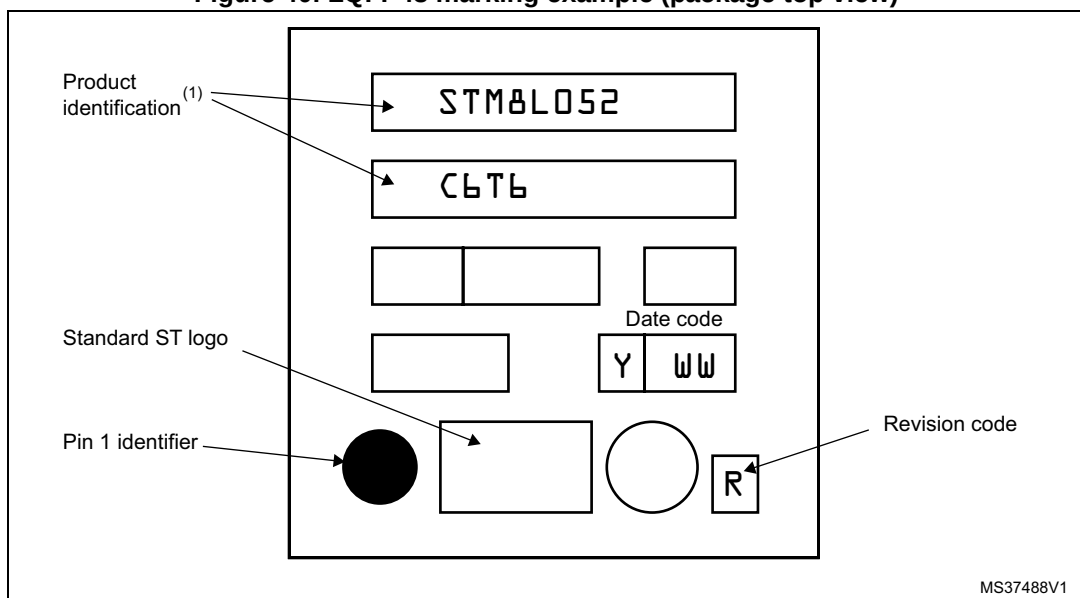
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 39. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint

1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 40. LQFP48 marking example (package top view)

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

11 Revision history

Table 55. Document revision history

Date	Revision	Changes
15-Jun-2012	1	Initial release.
09-Mar-2015	2	Updated: – the factory default setting for OPT5[3:0] in Table 10: Option byte addresses – Section 10: Part numbering, – the disclaimer. Added: – Figure 40: LQFP48 marking example (package top view).