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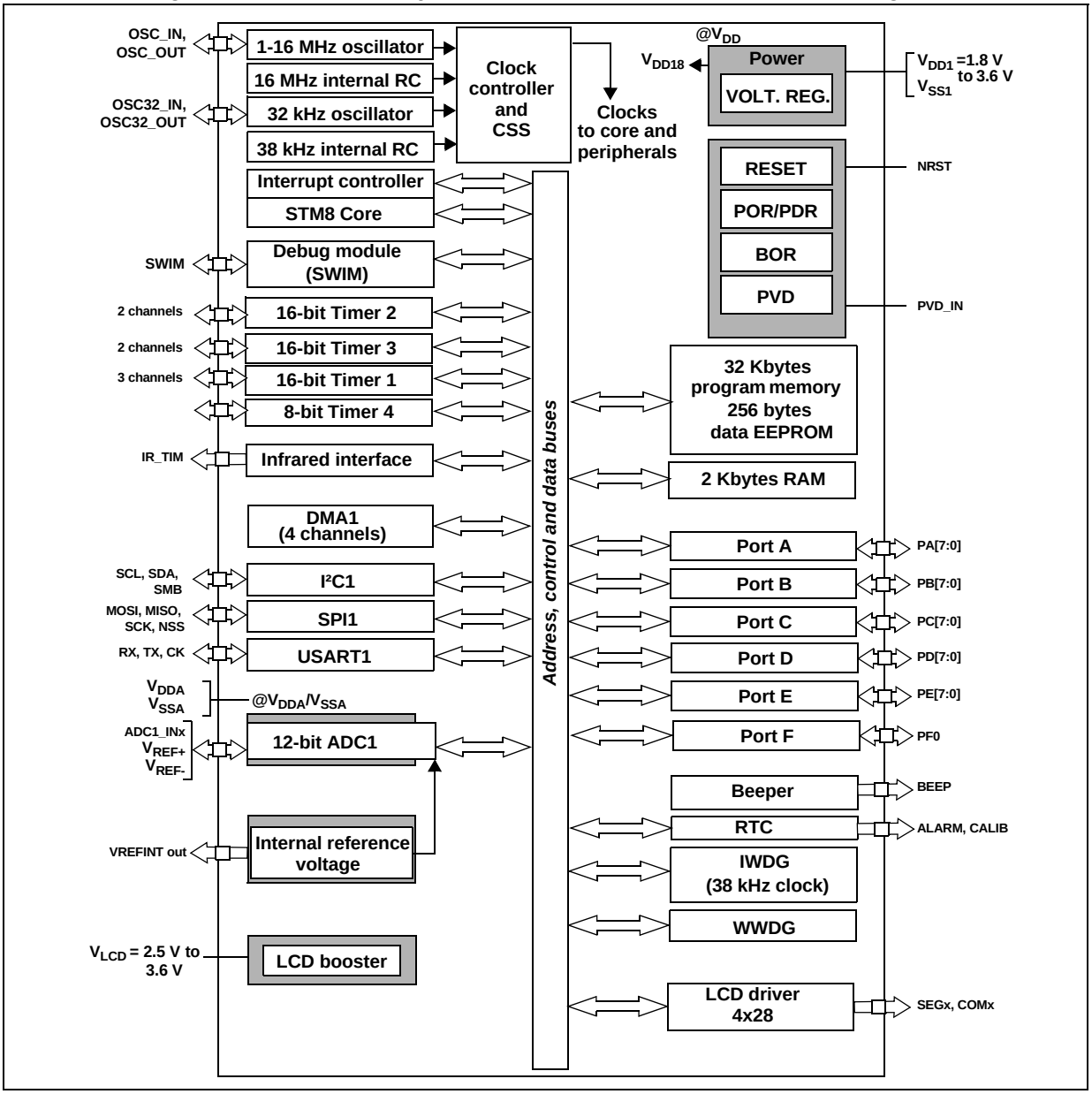
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, LCD, POR, PWM, WDT
Number of I/O	41
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 25x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l052c6t6tr

3 Functional overview

Figure 1. Medium-density value line STM8L052C6 device block diagram



1. **Legend**:
   ADC: Analog-to-digital converter
   BOR: Brownout reset
   DMA: Direct memory access
   I²C: Inter-integrated circuit multimaster interface
   LCD: Liquid crystal display
   POR/PDR: Power on reset / power down reset
   RTC: Real-time clock
   SPI: Serial peripheral interface
   SWIM: Single wire interface module
   USART: Universal synchronous asynchronous receiver transmitter
   WWDG: Window watchdog
   IWDG: independent watchdog

Table 4. Medium-density value line STM8L052C6pin description (continued)

Pin #	Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
5	PA4/TIM2_BKIN/ LCD_COM0/ADC1_IN2	I/O	TT(2)	X	X	X	HS	X	X	**Port A4**	Timer 2 - break input / LCD COM 0 / ADC1 input 2
6	PA5/TIM3_BKIN/ LCD_COM1/ADC1_IN1	I/O	TT(2)	X	X	X	HS	X	X	**Port A5**	Timer 3 - break input / LCD_COM 1 / ADC1 input 1
7	PA6/*[ADC1_TRIG]*/ LCD_COM2/ADC1_IN0	I/O	TT(2)	X	X	X	HS	X	X	**Port A6**	*[ADC1 - trigger]* / LCD_COM2 /ADC1 input 0
8	PA7/LCD_SEG0(3)	I/O	FT	X	X	X	HS	X	X	**Port A7**	LCD segment 0
24	PB0(4)/TIM2_CH1/ LCD_SEG10/ADC1_IN18	I/O	TT(2)	X(4)	X(4)	X	HS	X	X	**Port B0**	Timer 2 - channel 1 / LCD segment 10 / ADC1_IN18
25	PB1/TIM3_CH1/ LCD_SEG11/ ADC1_IN17	I/O	TT(2)	X	X	X	HS	X	X	**Port B1**	Timer 3 - channel 1 / LCD segment 11 / ADC1_IN17
26	PB2/ TIM2_CH2/ LCD_SEG12/ ADC1_IN16	I/O	TT(2)	X	X	X	HS	X	X	**Port B2**	Timer 2 - channel 2 / LCD segment 12 / ADC1_IN16
27	PB3/TIM2_ETR/ LCD_SEG13/ ADC1_IN15	I/O	TT(2)	X	X	X	HS	X	X	**Port B3**	Timer 2 - external trigger / LCD segment 13 /ADC1_IN15
28	PB4(4)/*[SPI1_NSS]*(8)/ LCD_SEG14/ ADC1_IN14	I/O	TT(2)	X(4)	X(4)	X	HS	X	X	**Port B4**	*[SPI1 master/slave select]* / LCD segment 14 / ADC1_IN14
29	PB5/*[SPI1_SCK]*(8)/ LCD_SEG15/ ADC1_IN13	I/O	TT(2)	X	X	X	HS	X	X	**Port B5**	*[SPI1 clock]* / LCD segment 15 / ADC1_IN13
30	PB6/[*SPI1_MOSI]*(8)/ LCD_SEG16/ ADC1_IN12	I/O	TT(2)	X	X	X	HS	X	X	**Port B6**	*[SPI1 master out/slave in]*/ LCD segment 16 / ADC1_IN12
31	PB7/*[SPI1_MISO]*(8)/ LCD_SEG17/ ADC1_IN11	I/O	TT(2)	X	X	X	HS	X	X	**Port B7**	*[SPI1 master in- slave out]* /LCD segment 17 / ADC1_IN11
37	PC0(3)/I2C1_SDA	I/O	FT	X		X		T(5)		**Port C0**	I2C1 data
38	PC1(3)/I2C1_SCL	I/O	FT	X		X		T(5)		**Port C1**	I2C1 clock
41	PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ VREFINT	I/O	TT(2)	X	X	X	HS	X	X	**Port C2**	USART1 receive / LCD segment 22 / ADC1_IN6 /Internal voltage reference output

Table 4. Medium-density value line STM8L052C6pin description (continued)

Pin #	Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
36	PD7/TIM1_CH1N /LCD_SEG21/ ADC1_IN7/RTC_ALARM/V REFINT	I/O	TT(2)	X	X	X	HS	X	X	**Port D7**	Timer 1 - inverted channel 1/ LCD segment 21 / ADC1_IN7 / RTC alarm / Internal voltage reference output
14	PE0(3)/LCD_SEG1	I/O	FT	X	X	X	HS	X	X	**Port E0**	LCD segment 1
15	PE1/TIM1_CH2N/ LCD_SEG2	I/O	TT(2)	X	X	X	HS	X	X	**Port E1**	Timer 1 - inverted channel 2 / LCD segment 2
16	PE2/TIM1_CH3N/ LCD_SEG3	I/O	TT(2)	X	X	X	HS	X	X	**Port E2**	Timer 1 - inverted channel 3 / LCD segment 3
17	PE3/LCD_SEG4	I/O	TT(2)	X	X	X	HS	X	X	**Port E3**	LCD segment 4
18	PE4/LCD_SEG5	I/O	TT(2)	X	X	X	HS	X	X	**Port E4**	LCD segment 5
19	PE5/LCD_SEG6/ ADC1_IN23	I/O	TT(2)	X	X	X	HS	X	X	**Port E5**	LCD segment 6 / ADC1_IN23
47	PE6/LCD_SEG26/ PVD_IN	I/O	TT(2)	X	X	X	HS	X	X	**Port E6**	LCD segment 26/PVD_IN
48	PE7/LCD_SEG27	I/O	TT(2)	X	X	X	HS	X	X	**Port E7**	LCD segment 27
32	PF0/ADC1_IN24	I/O		X	X	X	HS	X	X	**Port F0**	ADC1_IN24
13	VLCD	S								LCD booster external capacitor	
13	Reserved									Reserved. Must be tied to V_{DD}	
10	V_{DD}	S								Digital power supply	
11	V_{DDA}	S								Analog supply voltage	
12	V_{REF+}	S								ADC1 positive voltage reference	
9	$V_{SS1}/V_{SSA}/V_{REF-}$	S								I/O ground / Analog ground voltage / ADC1 negative voltage reference	
39	V_{DD2}	S								IOs supply voltage	
40	V_{SS2}	S								IOs ground voltage	
1	PA0(6)/*[USART1_CK]*(8)/ SWIM/BEEP/IR_TIM (7)	I/O		X	X(6)	X	HS (7)	X	X	**Port A0**	*[USART1 synchronous clock]*(8) / SWIM input and output /Beep output / Infrared Timer output

1. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output open-drain or push-pull, not as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L15x and STM8L16x reference manual (RM0031).
2. In the 3.6 V tolerant I/Os, protection diode to V_{DD} is not implemented.

3. In the 5 V tolerant I/Os, protection diode to V_{DD} is not implemented.
4. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
5. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to V_{DD} are not implemented).
6. The PA0 pin is in input pull-up during the reset phase and after reset release.
7. High Sink LED driver capability available on PA0.
8. [ ] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Note: The slope control of all GPIO pins, except true open drain pins, can be programmed. By default, the slope control is limited to 2 MHz.

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5084	DMA1	Reserved area (1 byte)		
0x00 5085		DMA1_C1M0ARH	DMA1 memory 0 address high register (channel 1)	0x00
0x00 5086		DMA1_C1M0ARL	DMA1 memory 0 address low register (channel 1)	0x00
0x00 5087 0x00 5088		Reserved area (2 bytes)		
0x00 5089		DMA1_C2CR	DMA1 channel 2 configuration register	0x00
0x00 508A		DMA1_C2SPR	DMA1 channel 2 status & priority register	0x00
0x00 508B		DMA1_C2NDTR	DMA1 number of data to transfer register (channel 2)	0x00
0x00 508C		DMA1_C2PARH	DMA1 peripheral address high register (channel 2)	0x52
0x00 508D		DMA1_C2PARL	DMA1 peripheral address low register (channel 2)	0x00
0x00 508E		Reserved area (1 byte)		
0x00 508F		DMA1_C2M0ARH	DMA1 memory 0 address high register (channel 2)	0x00
0x00 5090		DMA1_C2M0ARL	DMA1 memory 0 address low register (channel 2)	0x00
0x00 5091 0x00 5092		Reserved area (2 bytes)		
0x00 5093		DMA1_C3CR	DMA1 channel 3 configuration register	0x00
0x00 5094		DMA1_C3SPR	DMA1 channel 3 status & priority register	0x00
0x00 5095		DMA1_C3NDTR	DMA1 number of data to transfer register (channel 3)	0x00
0x00 5096		DMA1_C3PARH_ C3M1ARH	DMA1 peripheral address high register (channel 3)	0x40
0x00 5097		DMA1_C3PARL_ C3M1ARL	DMA1 peripheral address low register (channel 3)	0x00
0x00 5098		Reserved area (1 byte)		
0x00 5099		DMA1_C3M0ARH	DMA1 memory 0 address high register (channel 3)	0x00
0x00 509A		DMA1_C3M0ARL	DMA1 memory 0 address low register (channel 3)	0x00
0x00 509B to 0x00 509D		Reserved area (3 bytes)		
0x00 509E		SYSCFG_RMPCR1	Remapping register 1	0x00
0x00 509F		SYSCFG_RMPCR2	Remapping register 2	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50D3	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D4		WWDG_WR	WWDR window register	0x7F
0x00 50D5 to 00 50DF	Reserved area (11 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	BEEP	BEEP_CSR1	BEEP control/status register 1	0x00
0x00 50F1 0x00 50F2		Reserved area (2 bytes)		
0x00 50F3		BEEP_CSR2	BEEP control/status register 2	0x1F
0x00 50F4 to 0x00 513F	Reserved area (76 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5230	USART1	USART1_SR	USART1 status register	0xC0
0x00 5231		USART1_DR	USART1 data register	undefined
0x00 5232		USART1_BRR1	USART1 baud rate register 1	0x00
0x00 5233		USART1_BRR2	USART1 baud rate register 2	0x00
0x00 5234		USART1_CR1	USART1 control register 1	0x00
0x00 5235		USART1_CR2	USART1 control register 2	0x00
0x00 5236		USART1_CR3	USART1 control register 3	0x00
0x00 5237		USART1_CR4	USART1 control register 4	0x00
0x00 5238		USART1_CR5	USART1 control register 5	0x00
0x00 5239		USART1_GTR	USART1 guard time register	0x00
0x00 523A		USART1_PSCR	USART1 prescaler register	0x00
0x00 523B to 0x00 524F	Reserved area (21 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5251		TIM2_CR2	TIM2 control register 2	0x00
0x00 5252		TIM2_SMCR	TIM2 Slave mode control register	0x00
0x00 5253		TIM2_ETR	TIM2 external trigger register	0x00
0x00 5254		TIM2_DER	TIM2 DMA1 request enable register	0x00
0x00 5255		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5256		TIM2_SR1	TIM2 status register 1	0x00
0x00 5257		TIM2_SR2	TIM2 status register 2	0x00
0x00 5258		TIM2_EGR	TIM2 event generation register	0x00
0x00 5259		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 525A		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 525B		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 525C		TIM2_CNTRH	TIM2 counter high	0x00
0x00 525D		TIM2_CNTRL	TIM2 counter low	0x00
0x00 525E		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 525F		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 5260		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 5261		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5262		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5263		TIM2_CCR2H	TIM2 capture/compare register 2 high	0x00
0x00 5264		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5265		TIM2_BKR	TIM2 break register	0x00
0x00 5266		TIM2_OISR	TIM2 output idle state register	0x00
0x00 5267 to 0x00 527F	Reserved area (25 bytes)			

Table 7. General hardware register map (continued)

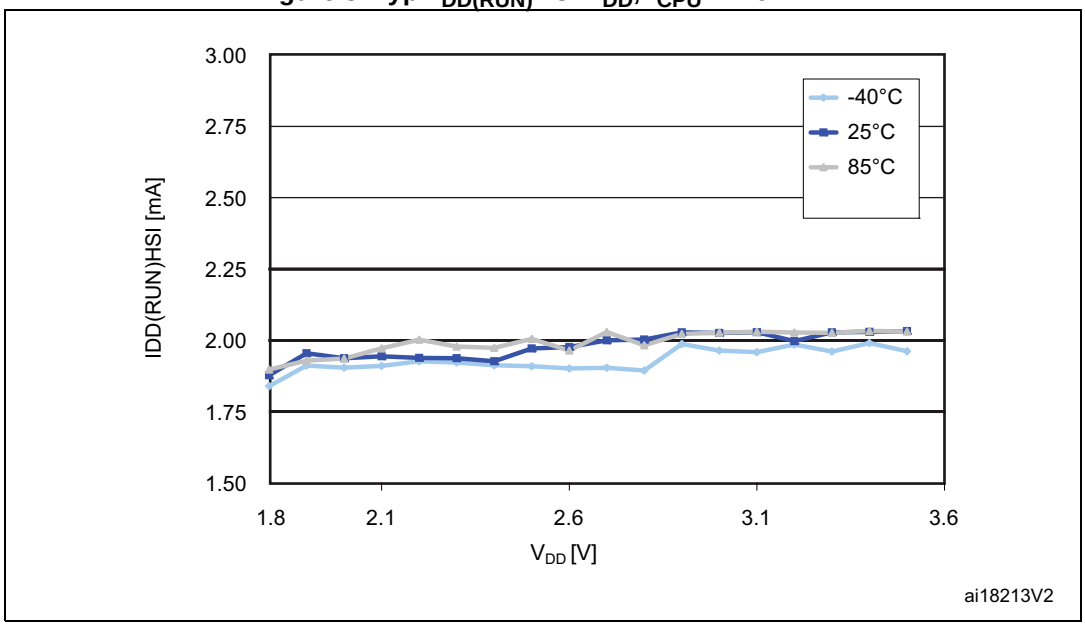
Address	Block	Register label	Register name	Reset status
0x00 5280	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5281		TIM3_CR2	TIM3 control register 2	0x00
0x00 5282		TIM3_SMCR	TIM3 Slave mode control register	0x00
0x00 5283		TIM3_ETR	TIM3 external trigger register	0x00
0x00 5284		TIM3_DER	TIM3 DMA1 request enable register	0x00
0x00 5285		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5286		TIM3_SR1	TIM3 status register 1	0x00
0x00 5287		TIM3_SR2	TIM3 status register 2	0x00
0x00 5288		TIM3_EGR	TIM3 event generation register	0x00
0x00 5289		TIM3_CCMR1	TIM3 Capture/Compare mode register 1	0x00
0x00 528A		TIM3_CCMR2	TIM3 Capture/Compare mode register 2	0x00
0x00 528B		TIM3_CCER1	TIM3 Capture/Compare enable register 1	0x00
0x00 528C		TIM3_CNTRH	TIM3 counter high	0x00
0x00 528D		TIM3_CNTRL	TIM3 counter low	0x00
0x00 528E		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 528F		TIM3_ARRH	TIM3 Auto-reload register high	0xFF
0x00 5290		TIM3_ARRL	TIM3 Auto-reload register low	0xFF
0x00 5291		TIM3_CCR1H	TIM3 Capture/Compare register 1 high	0x00
0x00 5292		TIM3_CCR1L	TIM3 Capture/Compare register 1 low	0x00
0x00 5293		TIM3_CCR2H	TIM3 Capture/Compare register 2 high	0x00
0x00 5294		TIM3_CCR2L	TIM3 Capture/Compare register 2 low	0x00
0x00 5295		TIM3_BKR	TIM3 break register	0x00
0x00 5296		TIM3_OISR	TIM3 output idle state register	0x00
0x00 5297 to 0x00 52AF	Reserved area (25 bytes)			

Table 11. Option byte description (continued)

Option byte No.	Option description
OPT5	**BOR_ON**: 0: Brownout reset off 1: Brownout reset on
	BOR_TH[3:1]: Brownout reset thresholds. Refer to *Table 20* for details on the thresholds according to the value of BOR_TH bits.
OPTBL	**OPTBL[15:0]**: This option is checked by the boot ROM code after reset. Depending on content of addresses 00 480B, 00 480C and 0x8000 (reset vector) the CPU jumps to the bootloader or to the reset vector. Refer to the UM0560 bootloader user manual for more details.

4. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 28*.
5. Tested in production.
6. The run from Flash consumption can be approximated with the linear formula: I_{DD}(run_from_Flash) = Freq * 195 µA/MHz + 440 µA
7. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 29*.

Figure 8. Typ. $I_{DD(RUN)}$ vs. V_{DD}, f_{CPU} = 16 MHz



1. Typical current consumption measured with code executed from RAM

Current consumption of on-chip peripherals

Table 24. Peripheral current consumption

Symbol	Parameter		Typ. V_{DD} = 3.0 V	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)		13	µA/MHz
$I_{DD(TIM2)}$	TIM2 supply current (1)		8	
$I_{DD(TIM3)}$	TIM3 supply current (1)		8	
$I_{DD(TIM4)}$	TIM4 timer supply current (1)		3	
$I_{DD(USART1)}$	USART1 supply current (2)		6	
$I_{DD(SPI1)}$	SPI1 supply current (2)		3	
$I_{DD(I2C1)}$	I^2C1 supply current (2)		5	
$I_{DD(DMA1)}$	DMA1 supply current(2)		3	
$I_{DD(WWDG)}$	WWDG supply current(2)		2	
$I_{DD(ALL)}$	Peripherals ON(3)		44	µA/MHz
$I_{DD(ADC1)}$	ADC1 supply current(4)		1500	µA
$I_{DD(PVD/BOR)}$	Power voltage detector and brownout Reset unit supply current (5)		2.6	
$I_{DD(BOR)}$	Brownout Reset unit supply current (5)		2.4	
$I_{DD(IDWDG)}$	Independent watchdog supply current	including LSI supply current	0.45	
		excluding LSI supply current	0.05	

1. Data based on a differential I_{DD} measurement between all peripherals OFF and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pins toggling. Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
3. Peripherals listed above the $I_{DD(ALL)}$ parameter ON: TIM1, TIM2, TIM3, TIM4, USART1, SPI1, I2C1, DMA1, WWDG.
4. Data based on a differential I_{DD} measurement between ADC in reset configuration and continuous ADC conversion.
5. Including supply current of internal reference voltage.

Table 25. Current consumption under external reset

Symbol	Parameter	Conditions		Typ	Unit
$I_{DD(RST)}$	Supply current under external reset (1)	All pins are externally tied to V_{DD}	V_{DD} = 1.8 V	48	µA
			V_{DD} = 3 V	76	
			V_{DD} = 3.6 V	91	

1. All pins except PA0, PB0 and PB4 are floating under reset. PA0, PB0 and PB4 are configured with pull-up under reset.

LSE crystal/ceramic resonator oscillator

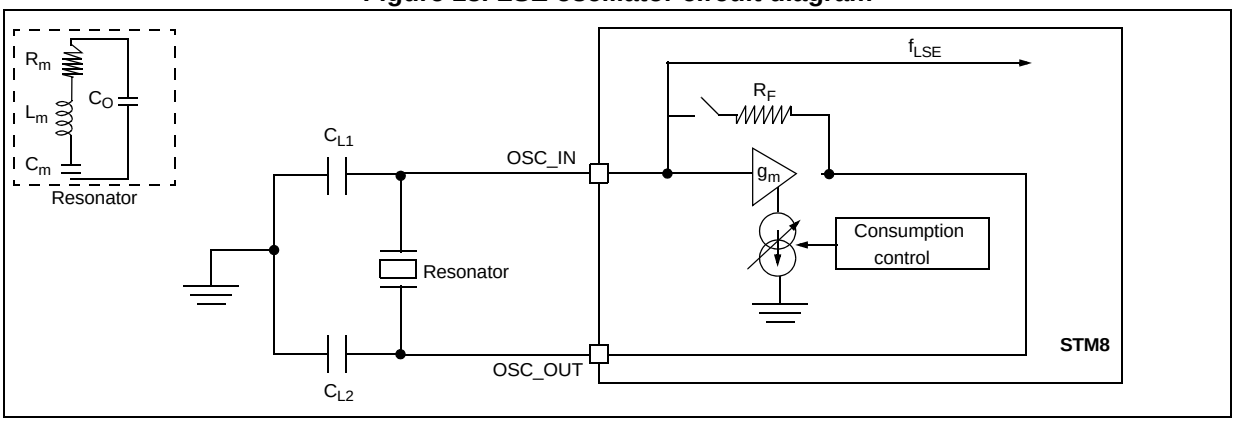
The LSE clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 29. LSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low speed external oscillator frequency	-	-	32.768	-	kHz
R_F	Feedback resistor	ΔV = 200 mV	-	1.2	-	MΩ
C(1)	Recommended load capacitance (2)	-	-	8	-	pF
$I_{DD(LSE)}$	LSE oscillator power consumption	-	-	-	1.4(3)	µA
		V_{DD} = 1.8 V	-	450	-	nA
		V_{DD} = 3 V	-	600	-	
		V_{DD} = 3.6 V	-	750	-	
g_m	Oscillator transconductance	-	3(3)		-	µA/V
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized	-	1	-	s

1. $C=C_{L1}=C_{L2}$ is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with a small R_m value. Refer to crystal manufacturer for more details.
3. Data guaranteed by Design. Not tested in production.
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 13. LSE oscillator circuit diagram



Internal clock sources

Subject to general operating conditions for V_{DD}, and T_A.

High speed internal RC oscillator (HSI)

In the following table, data is based on characterization results, not tested in production, unless otherwise specified.

Table 30. HSI oscillator characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16		MHz
ACC_{HSI}	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 3.0 V, T_A = 25 °C	-1 (2)	-	1(2)	%
		1.8 V ≤ V_{DD} ≤ 3.6 V, -40 °C ≤ T_A ≤ 85 °C	-5	-	5	%
TRIM	HSI user trimming step(3)	Trimming code ≠ multiple of 16	-	0.4	0.7	%
		Trimming code = multiple of 16	-		± 1.5	%
$t_{su(HSI)}$	HSI oscillator setup time (wakeup time)	-	-	3.7	6(4)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	100	140(4)	µA

1. V_{DD} = 3.0 V, T_A = -40 to 85 °C unless otherwise specified.
2. Tested in production.
3. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0). Refer to the AN3101 “STM8L15x internal RC oscillator calibration” application note for more details.
4. Guaranteed by design, not tested in production.

Figure 14. Typical HSI frequency vs. V_{DD}

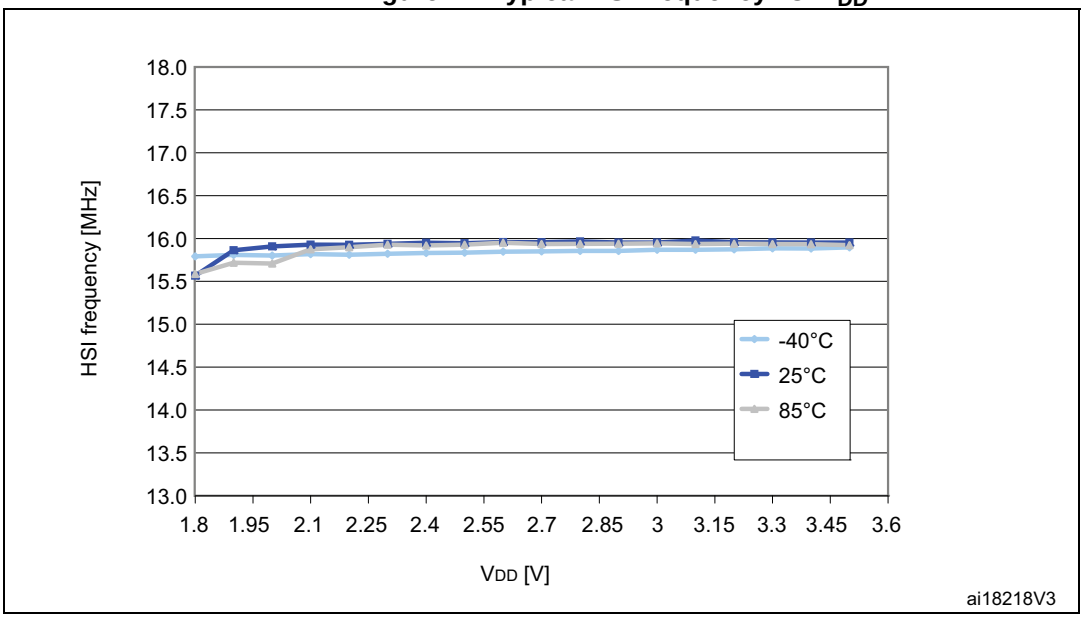


Figure 16. Typical V_{IL} and V_{IH} vs. V_{DD} (high sink I/Os)

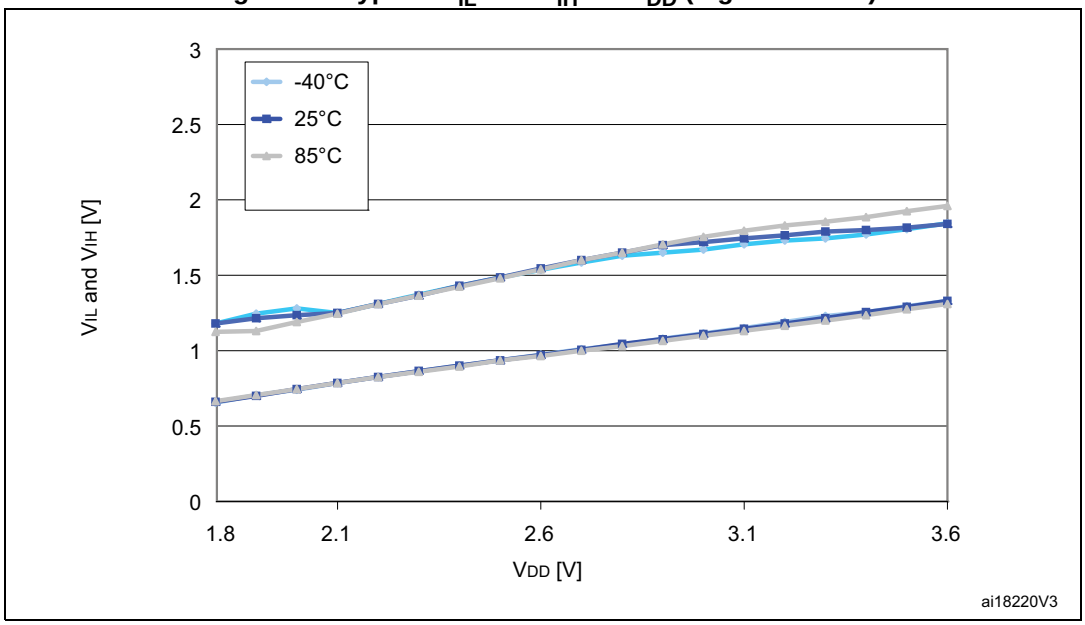


Figure 17. Typical V_{IL} and V_{IH} vs. V_{DD} (true open drain I/Os)

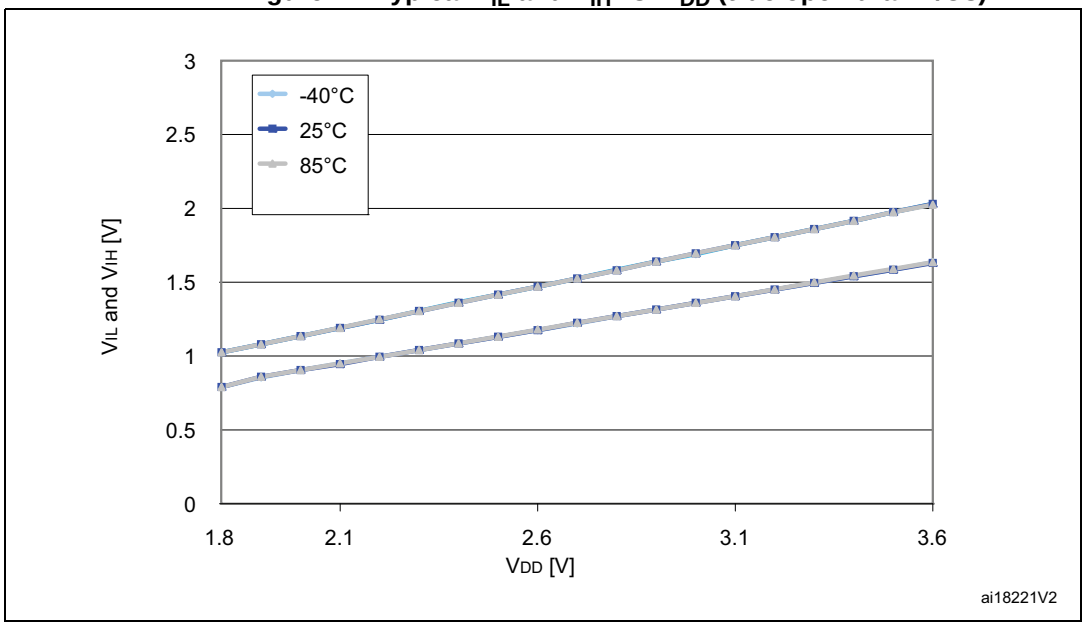
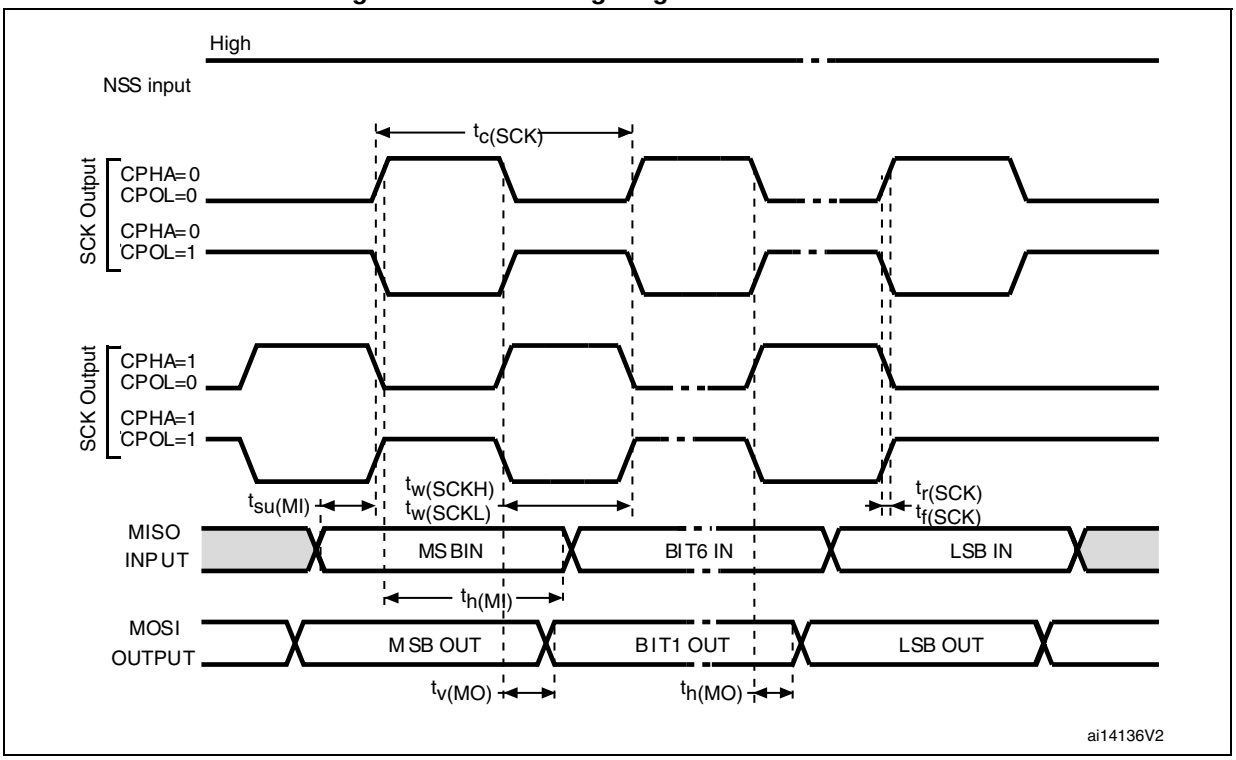
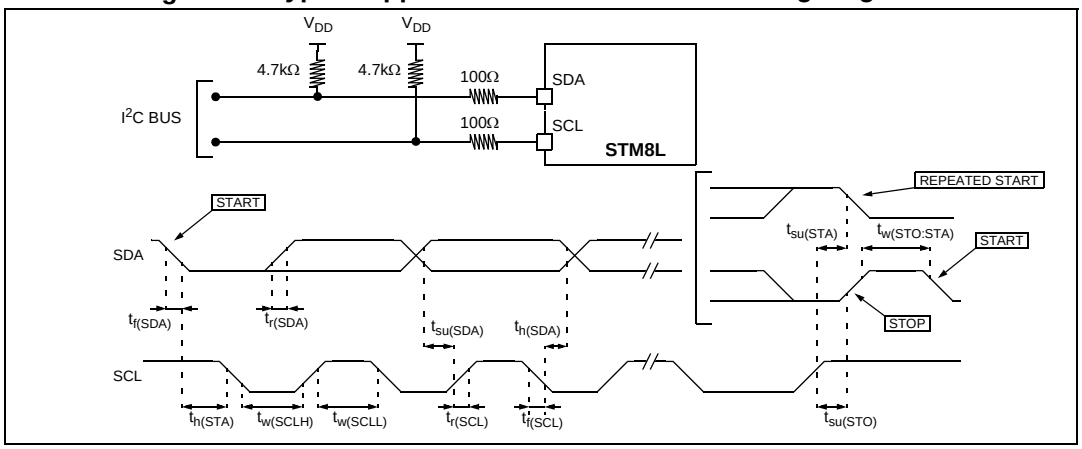


Figure 31. SPI1 timing diagram - master mode



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 32. Typical application with I²C bus and timing diagram 1)



1. Measurement points are done at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}

Figure 36. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

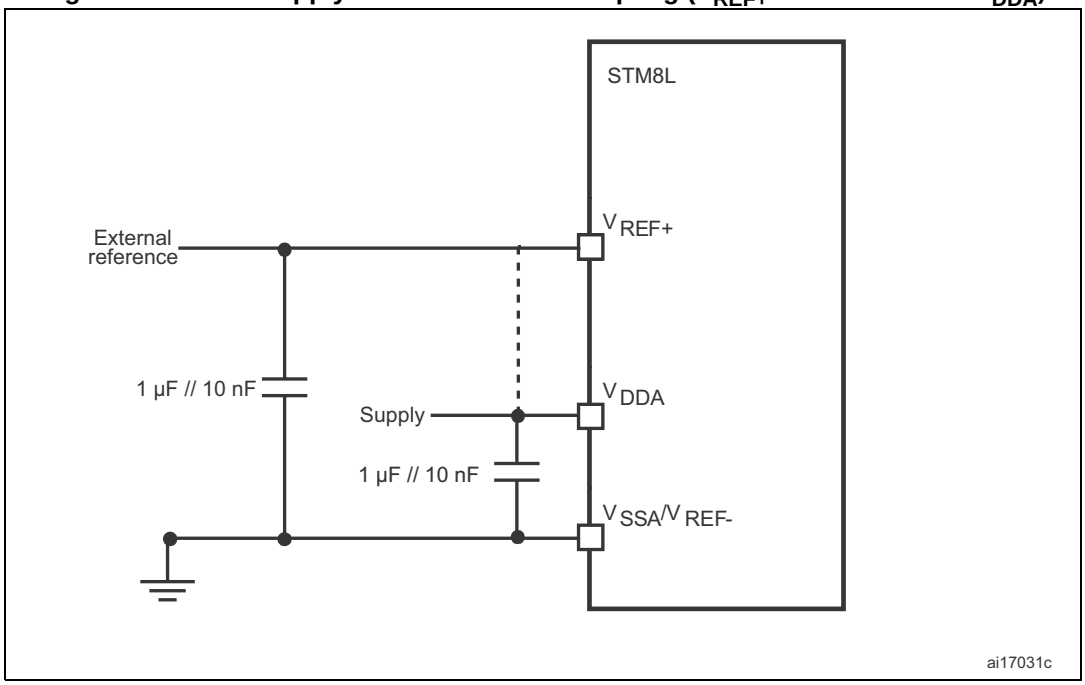


Figure 37. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

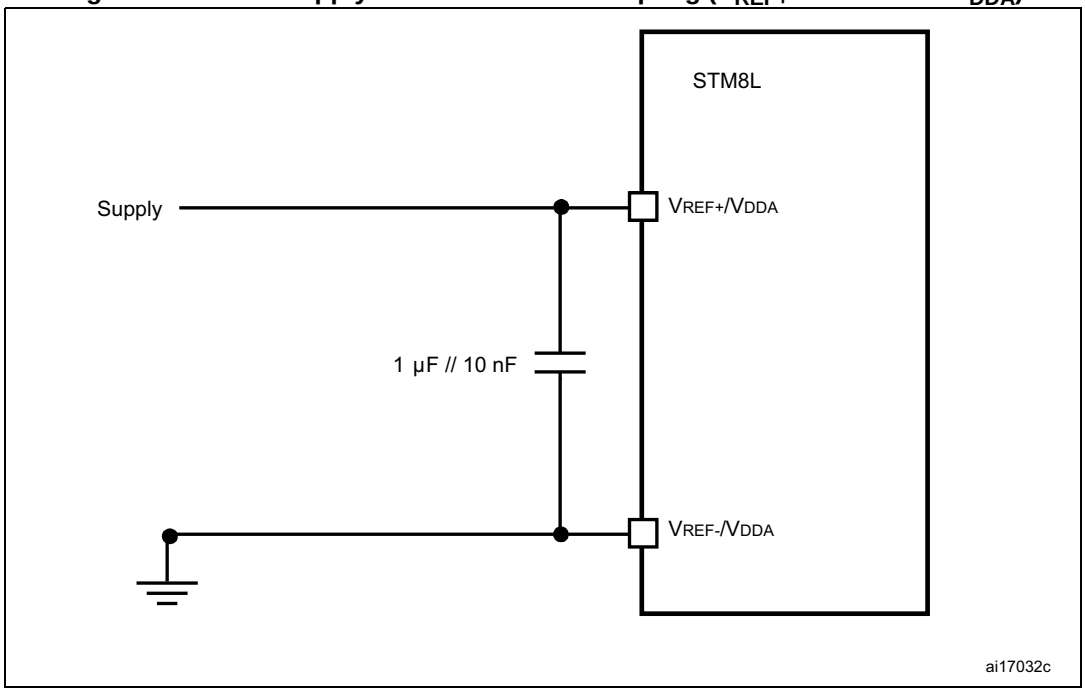


Table 53. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.