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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, SPI, UART/USART
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 26x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk10dx256vlh7

Table of Contents

1 Ordering parts.....	3	5.4.2 Thermal attributes.....	21
1.1 Determining valid orderable parts.....	3	6 Peripheral operating requirements and behaviors.....	21
2 Part identification.....	3	6.1 Core modules.....	22
2.1 Description.....	3	6.1.1 Debug trace timing specifications.....	22
2.2 Format.....	3	6.1.2 JTAG electricals.....	22
2.3 Fields.....	3	6.2 System modules.....	25
2.4 Example.....	4	6.3 Clock modules.....	25
3 Terminology and guidelines.....	4	6.3.1 MCG specifications.....	25
3.1 Definition: Operating requirement.....	4	6.3.2 Oscillator electrical specifications.....	27
3.2 Definition: Operating behavior.....	5	6.3.3 32 kHz Oscillator Electrical Characteristics.....	30
3.3 Definition: Attribute.....	5	6.4 Memories and memory interfaces.....	30
3.4 Definition: Rating.....	6	6.4.1 Flash electrical specifications.....	30
3.5 Result of exceeding a rating.....	6	6.4.2 EzPort Switching Specifications.....	35
3.6 Relationship between ratings and operating requirements.....	6	6.4.3 Flexbus Switching Specifications.....	36
3.7 Guidelines for ratings and operating requirements.....	7	6.5 Security and integrity modules.....	39
3.8 Definition: Typical value.....	7	6.6 Analog.....	39
3.9 Typical value conditions.....	8	6.6.1 ADC electrical specifications.....	39
4 Ratings.....	9	6.6.2 CMP and 6-bit DAC electrical specifications.....	47
4.1 Thermal handling ratings.....	9	6.6.3 12-bit DAC electrical characteristics.....	49
4.2 Moisture handling ratings.....	9	6.6.4 Voltage reference electrical specifications.....	52
4.3 ESD handling ratings.....	9	6.7 Timers.....	53
4.4 Voltage and current operating ratings.....	9	6.8 Communication interfaces.....	53
5 General.....	10	6.8.1 CAN switching specifications.....	53
5.1 AC electrical characteristics.....	10	6.8.2 DSPI switching specifications (limited voltage range).....	54
5.2 Nonswitching electrical specifications.....	10	6.8.3 DSPI switching specifications (full voltage range).....	55
5.2.1 Voltage and current operating requirements.....	10	6.8.4 I2C switching specifications.....	57
5.2.2 LVD and POR operating requirements.....	11	6.8.5 UART switching specifications.....	57
5.2.3 Voltage and current operating behaviors.....	12	6.8.6 I2S/SAI Switching Specifications.....	57
5.2.4 Power mode transition operating behaviors.....	13	6.9 Human-machine interfaces (HMI).....	61
5.2.5 Power consumption operating behaviors.....	14	6.9.1 TSI electrical specifications.....	61
5.2.6 Designing with radiated emissions in mind.....	18	7 Dimensions.....	62
5.2.7 Capacitance attributes.....	18	7.1 Obtaining package dimensions.....	62
5.3 Switching specifications.....	19	8 Pinout.....	63
5.3.1 Device clock specifications.....	19	8.1 K10 Signal Multiplexing and Pin Assignments.....	63
5.3.2 General switching specifications.....	19	8.2 K10 Pinouts.....	65
5.4 Thermal specifications.....	20	9 Revision History.....	67
5.4.1 Thermal operating requirements.....	20		

Terminology and guidelines

Field	Description	Values
FFF	Program flash memory size	• 32 = 32 KB • 64 = 64 KB • 128 = 128 KB • 256 = 256 KB • 512 = 512 KB • 1M0 = 1 MB
R	Silicon revision	• Z = Initial • (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = -40 to 105 • C = -40 to 85
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • FT = 48 QFN (7 mm x 7 mm) • LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm) • MP = 64 MAPBGA (5 mm x 5 mm) • LK = 80 LQFP (12 mm x 12 mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 MAPBGA (8 mm x 8 mm) • LQ = 144 LQFP (20 mm x 20 mm) • MD = 144 MAPBGA (13 mm x 13 mm) • MJ = 256 MAPBGA (17 mm x 17 mm)
CC	Maximum CPU frequency (MHz)	• 5 = 50 MHz • 7 = 72 MHz • 10 = 100 MHz • 12 = 120 MHz • 15 = 150 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

MK10DN512ZVMD10

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.61	—	mA	8
I _{DD_STOP}	Stop mode current at 3.0 V					
	• @ –40 to 25°C	—	0.35	0.567	mA	
	• @ 70°C	—	0.384	0.793	mA	
	• @ 105°C	—	0.628	1.2	mA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ –40 to 25°C	—	5.9	32.7	μA	
	• @ 70°C	—	26.1	59.8	μA	
	• @ 105°C	—	98.1	188	μA	
I _{DD_LLS}	Low leakage stop mode current at 3.0 V					9
	• @ –40 to 25°C	—	2.6	8.6	μA	
	• @ 70°C	—	10.3	29.1	μA	
	• @ 105°C	—	42.5	92.5	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					9
	• @ –40 to 25°C	—	1.9	5.8	μA	
	• @ 70°C	—	6.9	12.1	μA	
	• @ 105°C	—	28.1	41.9	μA	
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• @ –40 to 25°C	—	1.59	5.5	μA	
	• @ 70°C	—	4.3	9.5	μA	
	• @ 105°C	—	17.5	34	μA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ –40 to 25°C	—	1.47	5.4	μA	
	• @ 70°C	—	2.97	8.1	μA	
	• @ 105°C	—	12.41	32	μA	
I _{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	• @ –40 to 25°C	—	0.19	0.22	μA	
	• @ 70°C	—	0.49	0.64	μA	
	• @ 105°C	—	2.2	3.2	μA	

Table continues on the next page...

5.4.2 Thermal attributes

Board type	Symbol	Description	64 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	59	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	41	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	48	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	35	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	23	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	11	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification. For the MAPBGA, the board meets the JESD51-9 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal. For the LQFP, the board meets the JESD51-7 specification.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

Table 12. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J1	TCLK frequency of operation - Boundary Scan - JTAG and CJTAG - Serial Wire Debug	0 0 0	10 25 50	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width - Boundary Scan - JTAG and CJTAG - Serial Wire Debug	50 20 10	— — —	ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

Table 13. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation - Boundary Scan - JTAG and CJTAG - Serial Wire Debug	0 0 0	10 20 40	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width - Boundary Scan - JTAG and CJTAG - Serial Wire Debug	50 25 12.5	— — —	ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns

Table continues on the next page...

6.3.1 MCG specifications

Table 14. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f _{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C		—	32.768	—	kHz	
f _{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
Δf _{dco_res_t}	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	%f _{dco}	1
Δf _{dco_res_t}	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only		—	± 0.2	± 0.5	%f _{dco}	1
Δf _{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	+0.5/-0.7	—	%f _{dco}	1
Δf _{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 0.3	± 0.3	%f _{dco}	1
f _{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	4	—	MHz	
f _{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
f _{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f _{ints_t}	—	—	kHz	
f _{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f _{ints_t}	—	—	kHz	
FLL							
f _{fill_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f _{dco}	DCO output frequency range	Low range (DRS=00) 640 × f _{fill_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f _{fill_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f _{fill_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f _{fill_ref}	80	83.89	100	MHz	
f _{dco_t_DMx32}	DCO output frequency	Low range (DRS=00) 732 × f _{fill_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f _{fill_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f _{fill_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f _{fill_ref}	—	95.98	—	MHz	

Table continues on the next page...

6.3.2.1 Oscillator DC electrical specifications

Table 15. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	μA	
	• 8 MHz (RANGE=01)	—	300	—	μA	
	• 16 MHz	—	950	—	μA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	μA	
	• 4 MHz	—	400	—	μA	
	• 8 MHz (RANGE=01)	—	500	—	μA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	

Table continues on the next page...

- Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3.3 32 kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

6.3.3.1 32 kHz oscillator DC electrical specifications

Table 17. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	$M\Omega$
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp} ¹	Peak-to-peak amplitude of oscillation	—	0.6	—	V

- When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.3.2 32kHz oscillator frequency specifications

Table 18. 32kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$V_{ec_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

- Proper PC board layout procedures must be followed to achieve specifications.
- This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
- The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT} .

6.4 Memories and memory interfaces

6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

Table 20. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1
t_{swapx01}	Swap Control execution time	—	200	—	μs	
t_{swapx02}	• control code 0x02	—	70	150	μs	
t_{swapx04}	• control code 0x04	—	70	150	μs	
t_{swapx08}	• control code 0x08	—	—	30	μs	
$t_{\text{pgmpart32k}}$	Program Partition for EEPROM execution time	—	70	—	ms	
t_{setramff}	Set FlexRAM Function execution time:	—	50	—	μs	
t_{setram8k}	• Control Code 0xFF	—	0.3	0.5	ms	
$t_{\text{setram32k}}$	• 8 KB EEPROM backup	—	0.7	1.0	ms	
	• 32 KB EEPROM backup	—				
Byte-write to FlexRAM for EEPROM operation						
$t_{\text{eewr8bers}}$	Byte-write to erased FlexRAM location execution time	—	175	260	μs	3
t_{eewr8b8k}	Byte-write to FlexRAM execution time:	—	340	1700	μs	
$t_{\text{eewr8b16k}}$	• 8 KB EEPROM backup	—	385	1800	μs	
$t_{\text{eewr8b32k}}$	• 16 KB EEPROM backup	—	475	2000	μs	
	• 32 KB EEPROM backup	—				
Word-write to FlexRAM for EEPROM operation						
$t_{\text{eewr16bers}}$	Word-write to erased FlexRAM location execution time	—	175	260	μs	
$t_{\text{eewr16b8k}}$	Word-write to FlexRAM execution time:	—	340	1700	μs	
$t_{\text{eewr16b16k}}$	• 8 KB EEPROM backup	—	385	1800	μs	
$t_{\text{eewr16b32k}}$	• 16 KB EEPROM backup	—	475	2000	μs	
	• 32 KB EEPROM backup	—				
Longword-write to FlexRAM for EEPROM operation						
$t_{\text{eewr32bers}}$	Longword-write to erased FlexRAM location execution time	—	360	540	μs	
$t_{\text{eewr32b8k}}$	Longword-write to FlexRAM execution time:	—	545	1950	μs	
$t_{\text{eewr32b16k}}$	• 8 KB EEPROM backup	—	630	2050	μs	
$t_{\text{eewr32b32k}}$	• 16 KB EEPROM backup	—	810	2250	μs	
	• 32 KB EEPROM backup	—				

- Assumes 25 MHz flash clock frequency.
- Maximum times for erase parameters based on expectations at cycling end-of-life.
- For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

Table 27. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
f_{ADACK}	ADC asynchronous clock source	- ADLPC = 1, ADHSC = 0 - ADLPC = 1, ADHSC = 1 - ADLPC = 0, ADHSC = 0 - ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	12-bit modes <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB ⁴	5
DNL	Differential non-linearity	12-bit modes <12-bit modes	— —	±0.7 ±0.2	-1.1 to +1.9 -0.3 to 0.5	LSB ⁴	5
INL	Integral non-linearity	12-bit modes <12-bit modes	— —	±1.0 ±0.5	-2.7 to +1.9 -0.7 to +0.5	LSB ⁴	5
E_{FS}	Full-scale error	12-bit modes <12-bit modes	— —	-4 -1.4	-5.4 -1.8	LSB ⁴	$V_{ADIN} = V_{DDA}$ 5
E_Q	Quantization error	16-bit modes ≤13-bit modes	— —	-1 to 0 —	— ±0.5	LSB ⁴	
ENOB	Effective number of bits	16-bit differential mode - Avg = 32 - Avg = 4 16-bit single-ended mode - Avg = 32 - Avg = 4	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	— — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	
THD	Total harmonic distortion	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	— —	-94 -85	— —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	82 78	95 90	— —	dB dB	7

Table continues on the next page...

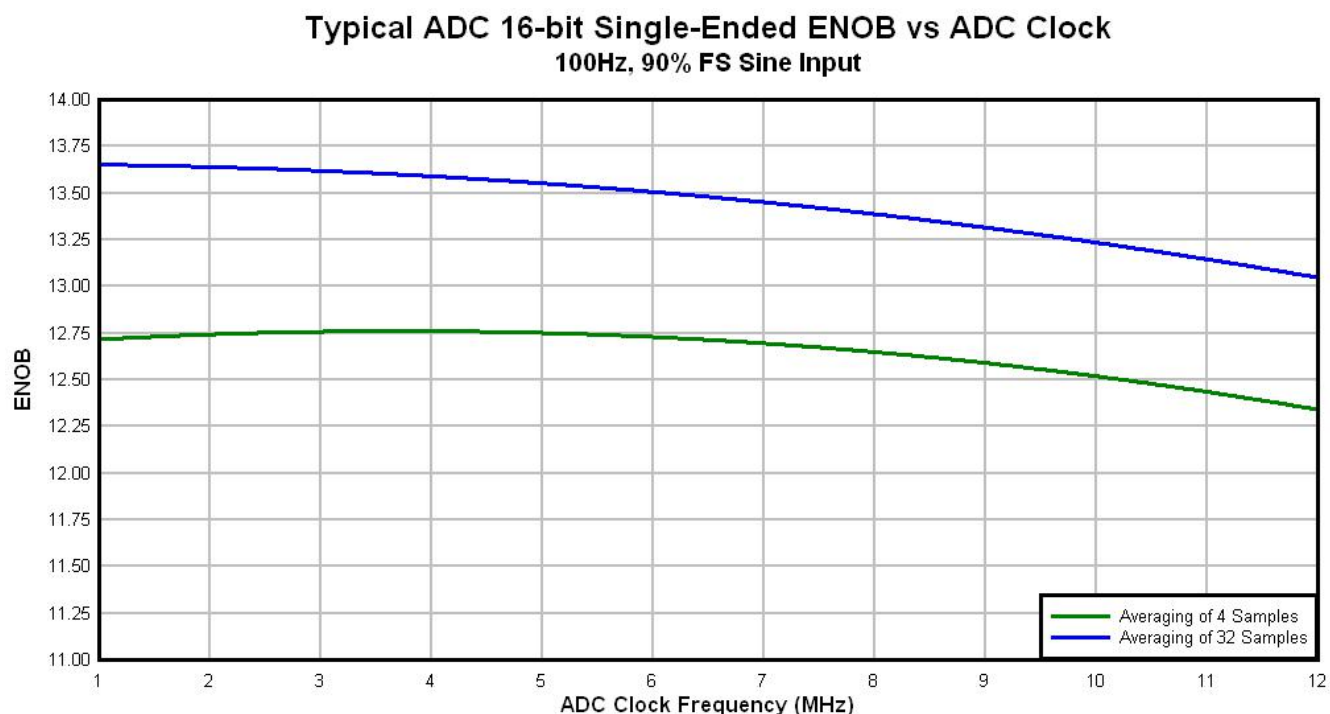


Figure 16. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.6.1.3 16-bit ADC with PGA operating conditions

Table 28. 16-bit ADC with PGA operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
V _{REFPGA}	PGA ref voltage		V _{REF_OU} T	V _{REF_OU} T	V _{REF_OU} T	V	2, 3
V _{ADIN}	Input voltage		V _{SSA}	—	V _{DDA}	V	
V _{CM}	Input Common Mode range		V _{SSA}	—	V _{DDA}	V	
R _{PGAD}	Differential input impedance	Gain = 1, 2, 4, 8 Gain = 16, 32 Gain = 64	— — —	128 64 32	— — —	kΩ	IN+ to IN- ⁴
R _{AS}	Analog source resistance		—	100	—	Ω	5
T _S	ADC sampling time		1.25	—	—	μs	6

Table continues on the next page...

Table 29. 16-bit ADC with PGA characteristics (continued)

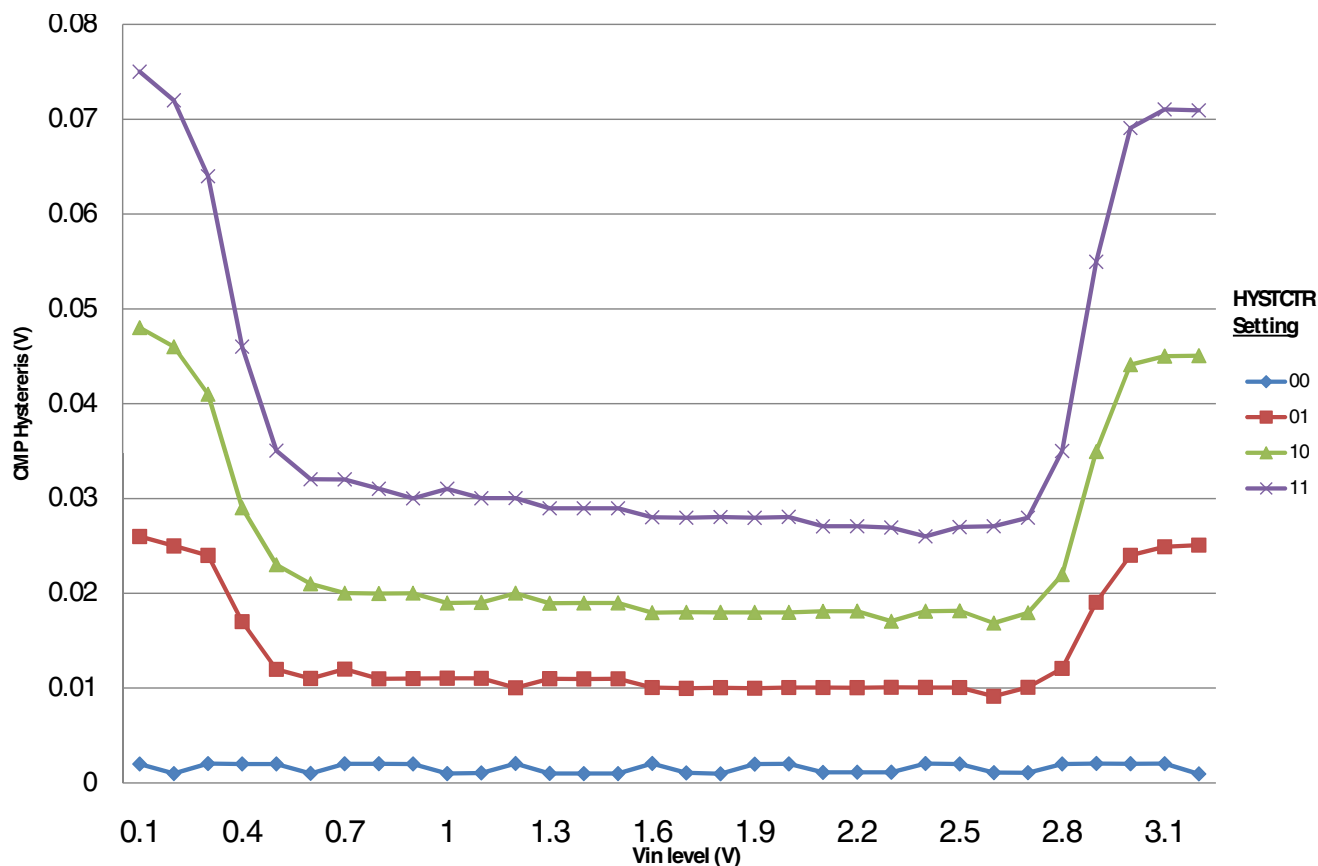
Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
G	Gain ⁴	- PGAG=0 - PGAG=1 - PGAG=2 - PGAG=3 - PGAG=4 - PGAG=5 - PGAG=6	0.95 1.9 3.8 7.6 15.2 30.0 58.8	1 2 4 8 16 31.6 63.3	1.05 2.1 4.2 8.4 16.6 33.2 67.8		R _{AS} < 100Ω
BW	Input signal bandwidth	16-bit modes < 16-bit modes	— —	— —	4 40	kHz kHz	
PSRR	Power supply rejection ratio	Gain=1	—	-84	—	dB	V _{DDA} = 3V ±100mV, f _{VDDA} = 50Hz, 60Hz
CMRR	Common mode rejection ratio	- Gain=1 - Gain=64	— —	-84 -85	— —	dB dB	V _{CM} = 500mVpp, f _{VCM} = 50Hz, 100Hz
V _{OFS}	Input offset voltage		—	0.2	—	mV	Output offset = V _{OFS} *(Gain+1)
T _{GSW}	Gain switching settling time		—	—	10	μs	5
dG/dT	Gain drift over full temperature range	- Gain=1 - Gain=64	— —	6 31	10 42	ppm/°C ppm/°C	
dG/dV _{DDA}	Gain drift over supply voltage	- Gain=1 - Gain=64	— —	0.07 0.14	0.21 0.31	%/V %/V	V _{DDA} from 1.71 to 3.6V
E _{IL}	Input leakage error	All modes	I _{in} × R _{AS}			mV	I _{in} = leakage current (refer to the MCU's voltage and current operating ratings)
V _{PP,DIFF}	Maximum differential input signal swing		$\left(\frac{(\min(V_X, V_{DDA} - V_X) - 0.2) \times 4}{\text{Gain}} \right)$ where V _X = V _{REFPGA} × 0.583			V	6
SNR	Signal-to-noise ratio	- Gain=1 - Gain=64	80 52	90 66	— —	dB dB	16-bit differential mode, Average=32
THD	Total harmonic distortion	- Gain=1 - Gain=64	85 49	100 95	— —	dB dB	16-bit differential mode, Average=32, f _{in} =100Hz

Table continues on the next page...

Table 30. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
V_{CMPOH}	Output high	$V_{DD} - 0.5$	—	—	V
V_{CMPOI}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	—	—	40	μ s
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μ A
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}-0.6V$.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$


Figure 17. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)

6.6.3.2 12-bit DAC operating behaviors

Table 32. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	150	μA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	700	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFFF	$V_{DACR} - 100$	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	± 8	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2$ V	—	—	± 1	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF_OUT}$	—	—	± 1	LSB	4
V_{OFFSET}	Offset error	—	± 0.4	± 0.8	%FSR	5
E_G	Gain error	—	± 0.1	± 0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4$ V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	$\mu V/C$	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
R_{op}	Output resistance load = 3 k Ω	—	—	250	Ω	
SR	Slew rate -80h → F7Fh → 80h - High power (SP_{HP}) - Low power (SP_{LP})	1.2 0.05	1.7 0.12	— —	V/ μs	
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth - High power (SP_{HP}) - Low power (SP_{LP})	550 40	— —	— —	kHz	

- Settling within ± 1 LSB
- The INL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
- The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
- The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV with $V_{DDA} > 2.4$ V
- Calculated by a best fit curve from $V_{SS} + 100$ mV to $V_{DACR} - 100$ mV
- $V_{DDA} = 3.0$ V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

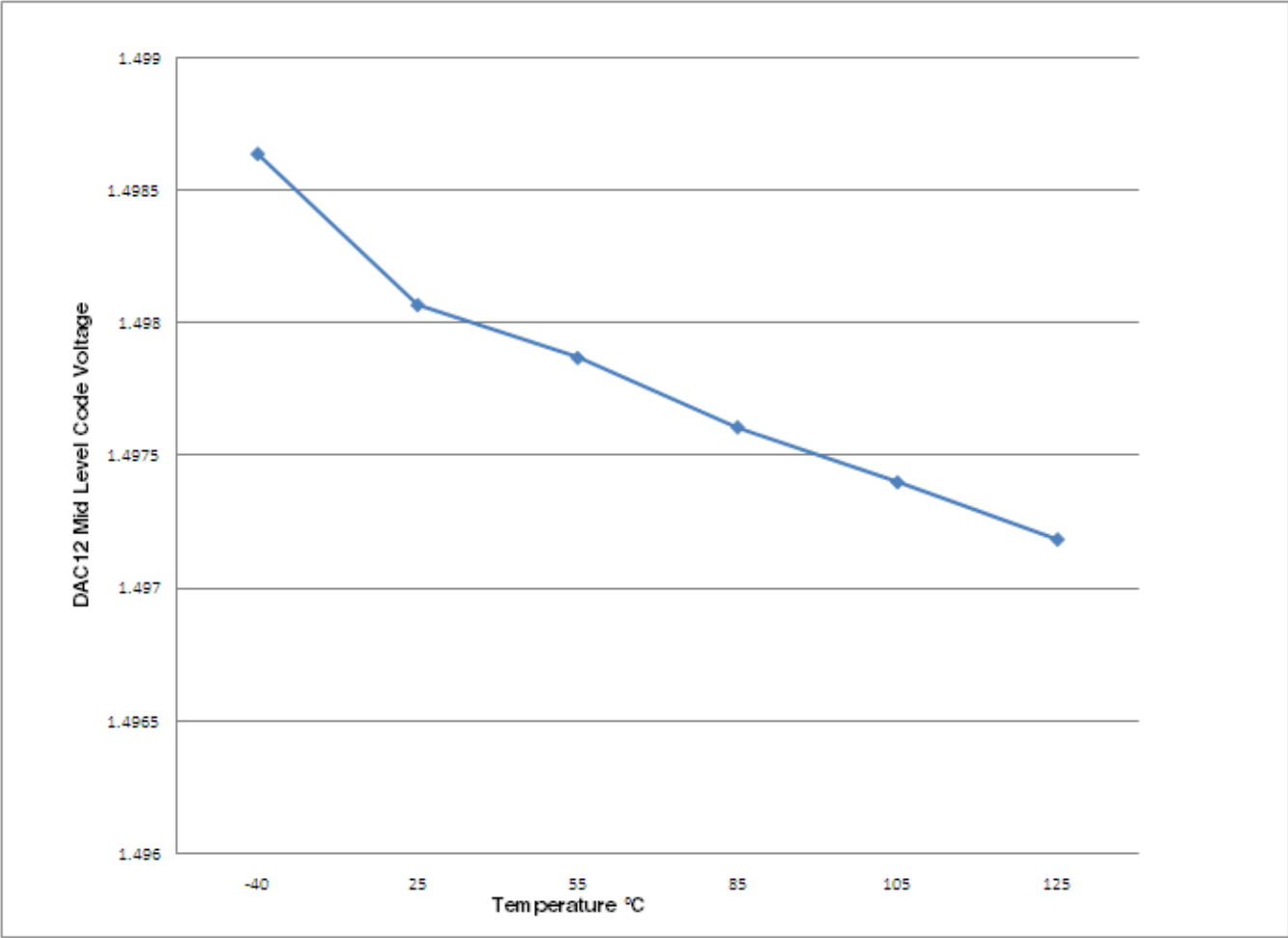


Figure 20. Offset at half scale vs. temperature

6.6.4 Voltage reference electrical specifications

Table 33. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V _{DDA}	Supply voltage	1.71	3.6	V	
T _A	Temperature	Operating temperature range of the device		°C	
C _L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

6.8.1 CAN switching specifications

See [General switching specifications](#).

6.8.2 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 37. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	$2 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 2$	—	ns	1
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 2$	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

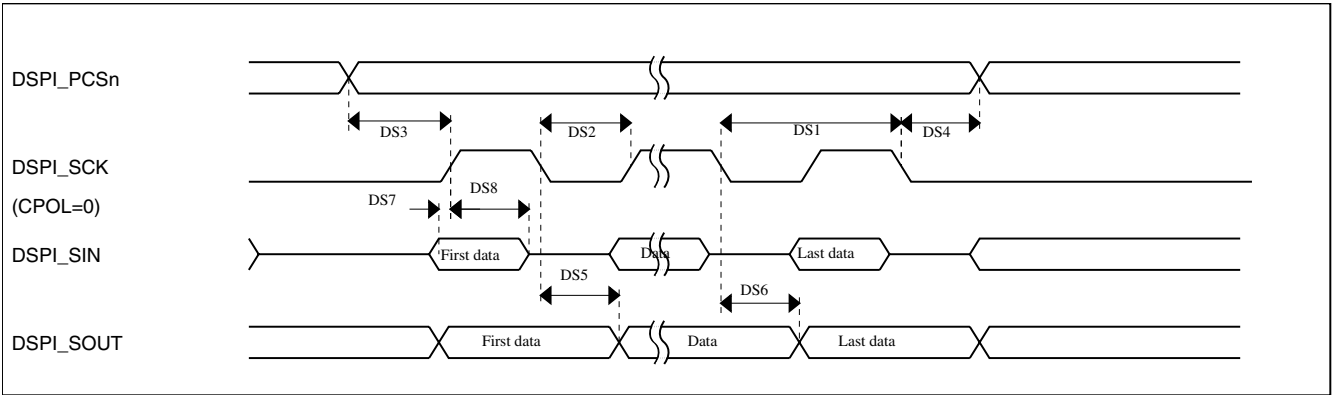


Figure 21. DSPI classic SPI timing — master mode

Table 41. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	-1.0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	20.5	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

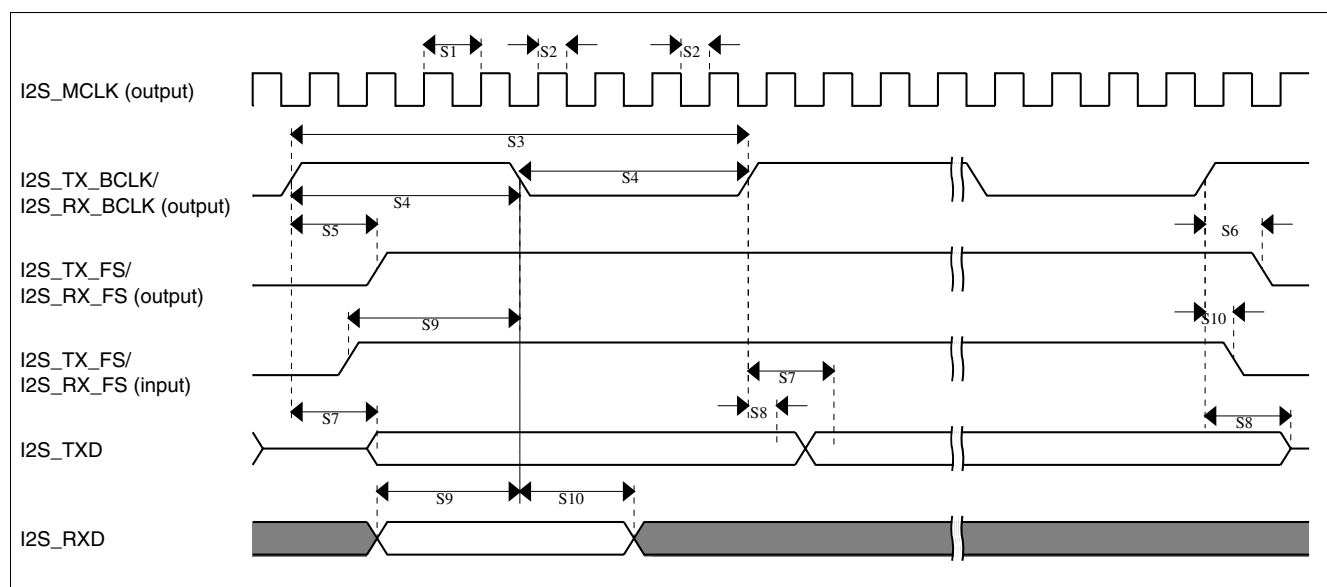


Figure 25. I2S/SAI timing — master modes

Table 42. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period

Table continues on the next page...

Table 42. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	5.8	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	5.8	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

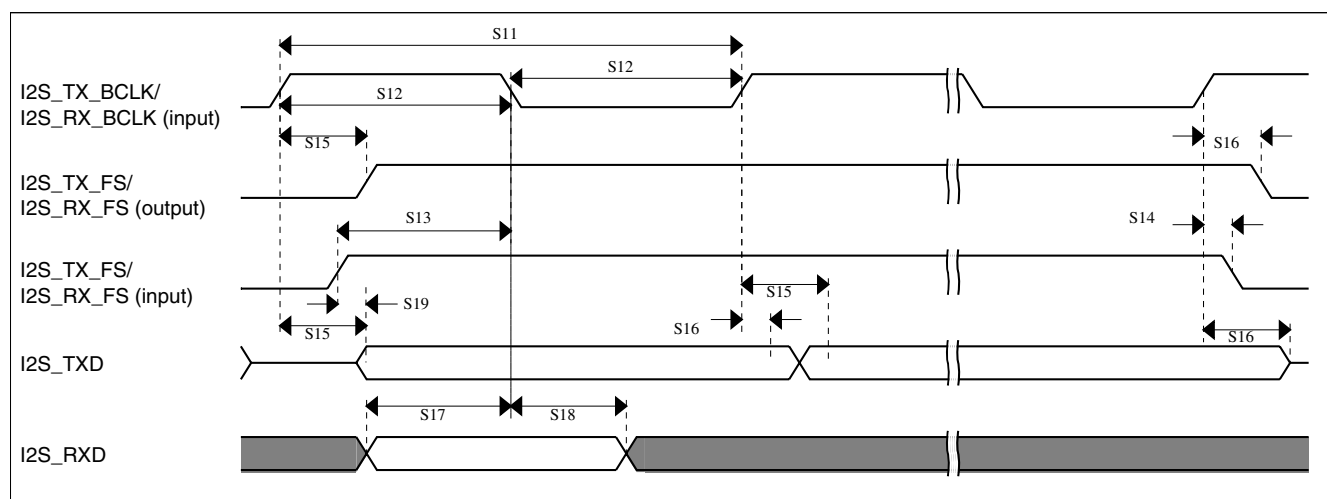


Figure 26. I2S/SAI timing — slave modes

6.8.6.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 43. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period

Table continues on the next page...

Table 43. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	53	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

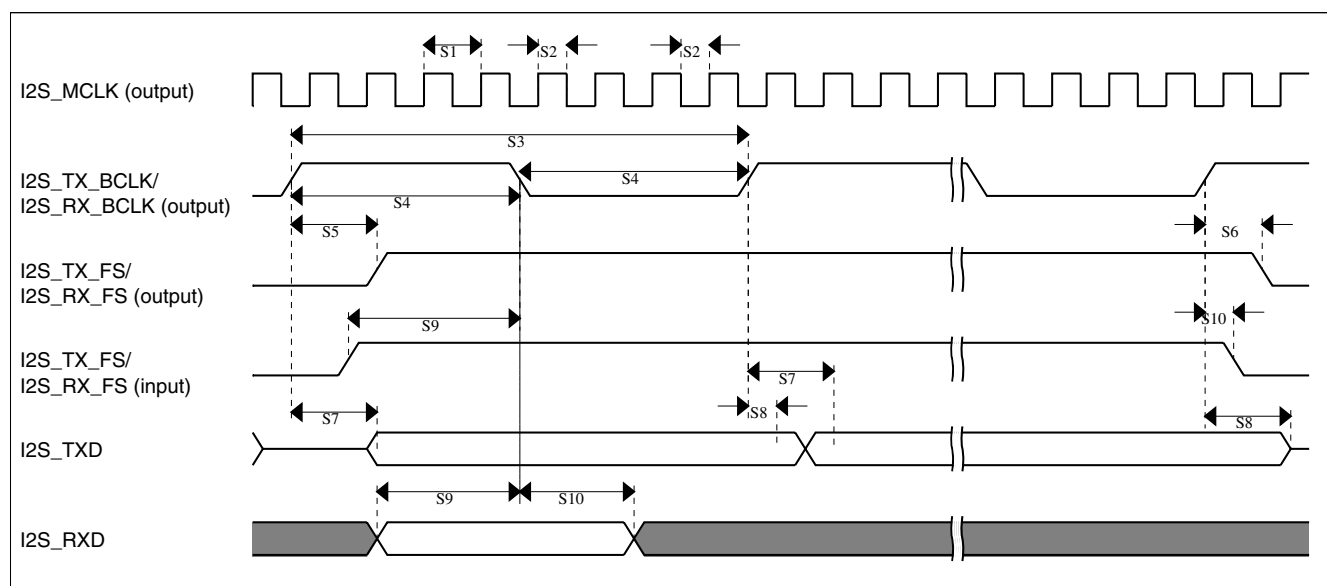


Figure 27. I2S/SAI timing — master modes

Table 44. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	7.6	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	67	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns

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