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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | H8S/2600 |
| Core Size | 16-Bit |
| Speed | 33MHz |
| Connectivity | EBI/EMI, I²C, IrDA, SCI, SmartCard, SPI, SSU, UART/USART |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | 98 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 48K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 16x10b; D/A 2x8b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LFQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f24278dvfqu |

2. Description of Numbers and Symbols

Aspects of the notations for register names, bit names, numbers, and symbolic names in this manual are explained below.

(1) Overall notation

In descriptions involving the names of bits and bit fields within this manual, the modules and registers to which the bits belong may be clarified by giving the names in the forms "module name"."register name"."bit name" or "register name"."bit name".

(2) Register notation

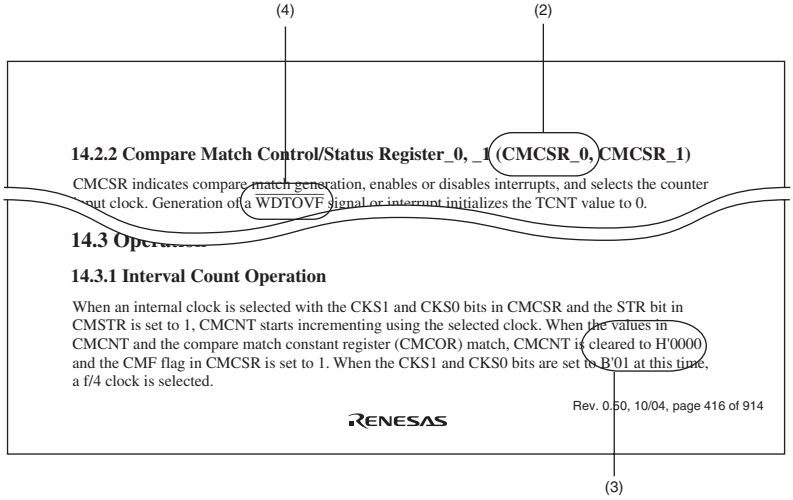
The style "register name"_"instance number" is used in cases where there is more than one instance of the same function or similar functions.
[Example] CMCSR_0: Indicates the CMCSR register for the compare-match timer of channel 0.

(3) Number notation

Binary numbers are given as B'nnnn (B' may be omitted if the number is obviously binary), hexadecimal numbers are given as H'nnnn or 0xnnnn, and decimal numbers are given as nnnn.
[Examples] Binary: B'11 or 11
Hexadecimal: H'EFA0 or 0xEFA0
Decimal: 1234

(4) Notation for active-low

An overbar on the name indicates that a signal or pin is active-low.
[Example] $\overline{\text{WDTOVF}}$

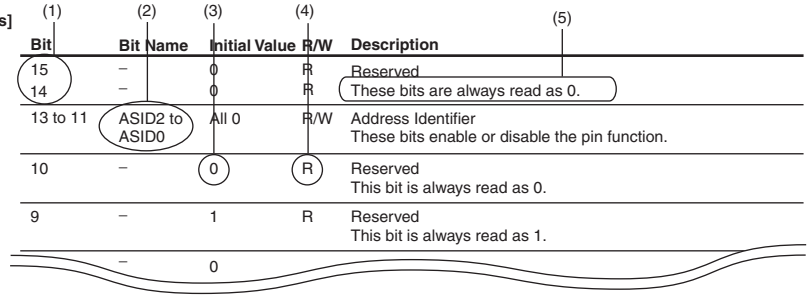



Note: The bit names and sentences in the above figure are examples and have nothing to do with the contents of this manual.

3. Description of Registers

Each register description includes a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meanings of the bit settings. The standard format and notation for bit charts and tables are described below.

[Table of Bits]




| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 15 | – | 0 | R | Reserved |
| 14 | – | 0 | R | These bits are always read as 0. |
| 13 to 11 | ASID2 to ASID0 | All 0 | R/W | Address Identifier<br>These bits enable or disable the pin function. |
| 10 | – | 0 | R | Reserved<br>This bit is always read as 0. |
| 9 | – | 1 | R | Reserved<br>This bit is always read as 1. |
| | – | 0 | | |

Note: The bit names and sentences in the above figure are examples, and have nothing to do with the contents of this manual.

(1) Bit
Indicates the bit number or numbers.
In the case of a 32-bit register, the bits are arranged in order from 31 to 0. In the case of a 16-bit register, the bits are arranged in order from 15 to 0.

(2) Bit name
Indicates the name of the bit or bit field.
When the number of bits has to be clearly indicated in the field, appropriate notation is included (e.g., ASID[3:0]).
A reserved bit is indicated by "–".
Certain kinds of bits, such as those of timer counters, are not assigned bit names. In such cases, the entry under Bit Name is blank.

(3) Initial value
Indicates the value of each bit immediately after a power-on reset, i.e., the initial value.
0: The initial value is 0
1: The initial value is 1
–: The initial value is undefined

(4) R/W
For each bit and bit field, this entry indicates whether the bit or field is readable or writable, or both writing to and reading from the bit or field are impossible.
The notation is as follows:

R/W: The bit or field is readable and writable.
R/(W): The bit or field is readable and writable.
However, writing is only performed to flag clearing.
R: The bit or field is readable.
"R" is indicated for all reserved bits. When writing to the register, write the value under Initial Value in the bit chart to reserved bits or fields.
W: The bit or field is writable.

(5) Description
Describes the function of the bit or field and specifies the values for writing.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 3 | IRQ1SCB | 0 | R/W | IRQ1 Sense Control B |
| 2 | IRQ1SCA | 0 | R/W | IRQ1 Sense Control A<br>00: Interrupt request generated at $\overline{\text{IRQ1}}$ input low level<br>01: Interrupt request generated at falling edge of $\overline{\text{IRQ1}}$ input<br>10: Interrupt request generated at rising edge of $\overline{\text{IRQ1}}$ input<br>11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ1}}$ input |
| 1 | IRQ0SCB | 0 | R/W | IRQ0 Sense Control B |
| 0 | IRQ0SCA | 0 | R/W | IRQ0 Sense Control A<br>00: Interrupt request generated at $\overline{\text{IRQ0}}$ input low level<br>01: Interrupt request generated at falling edge of $\overline{\text{IRQ0}}$ input<br>10: Interrupt request generated at rising edge of $\overline{\text{IRQ0}}$ input<br>11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ0}}$ input |

### 7.8.14 Mode Register Setting of Synchronous DRAM

To use synchronous DRAM, mode must be set after power-on. To set mode, set the RMTS2 to RMTS0 bits in DRAMCR to H'5 and enable the synchronous DRAM mode register setting. After that, access the continuous synchronous DRAM space in bytes. When the value to be set in the synchronous DRAM mode register is X, value X is set in the synchronous DRAM mode register by writing to the continuous synchronous DRAM space of address H'400000 + X for 8-bit bus configuration synchronous DRAM and by writing to the continuous synchronous DRAM space of address H'400000 + 2X for 16-bit bus configuration synchronous DRAM.

The value of the address signal is fetched at the issuance time of the MRS command as the setting value of the mode register in the synchronous DRAM. Mode of burst read/burst write in the synchronous DRAM is not supported by this LSI. For setting the mode register of the synchronous DRAM, set the burst read/single write with the burst length of 1. Figure 7.71 shows the setting timing of the mode in the synchronous DRAM.

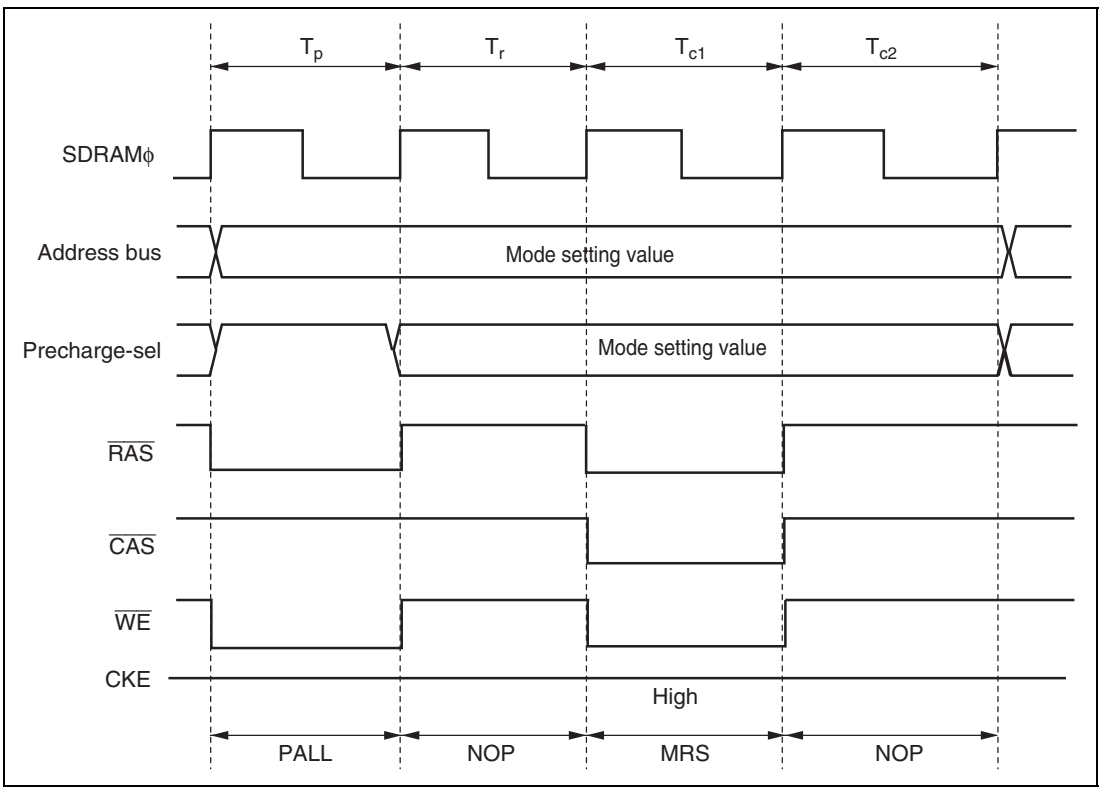



**Figure 7.71 Synchronous DRAM Mode Setting Timing**

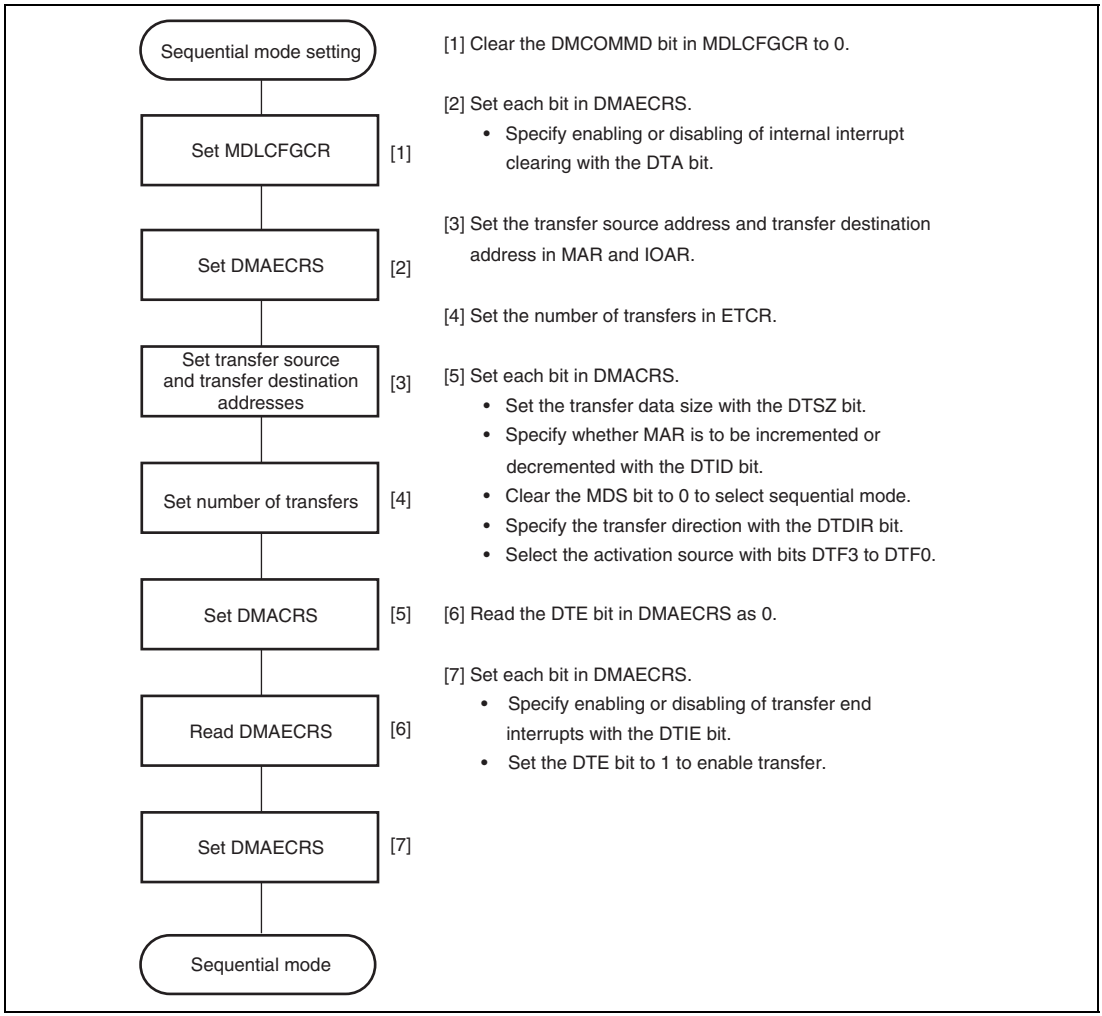



**Figure 8.4 Example of Sequential Mode Setting Procedure (Common Register Disabled Mode)**

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 6 | IRF | 0 | R/(W)* | Interrupt Request Flag<br>Flag indicating that an interrupt request has occurred and transfer has ended.<br>0: No interrupt request<br>[Clearing conditions]<br>• Writing 1 to the EDA bit<br>• Writing 0 to IRF after reading IRF = 1<br>1: Interrupt request occurrence<br>[Setting conditions]<br>• Transfer end interrupt request generated by transfer counter<br>• Source address repeat area overflow interrupt request<br>• Destination address repeat area overflow interrupt request |
| 5 | TCEIE | 0 | R/W | Transfer Counter End Interrupt Enable<br>Enables or disables transfer end interrupt requests by the transfer counter. When transfer ends according to the transfer counter while this bit is set to 1, the IRF bit is set to 1, indicating that an interrupt request has occurred.<br>0: Transfer end interrupt requests by transfer counter are disabled<br>1: Transfer end interrupt requests by transfer counter are enabled |
| 4 | SDIR | 0 | R/W | Single Address Direction<br>Specifies the data transfer direction in single address mode. In dual address mode, the specification by this bit is ignored.<br>0: Transfer direction: EDSAR → external device with $\overline{\text{DACK}}$<br>1: Transfer direction: External device with $\overline{\text{DACK}}$→ EDDAR |

| TPU channel 4 settings | (2) | (1) | (2) | (1) | (1) | (2) |
|---|---|---|---|---|---|---|
| MD3 to MD0 | B'0000, B'01xx | | B'001x | B'0010 | B'0011 | |
| IOA3 to IOA0 | B'0000, B'0100, B'1xxx | B'0001 to B'0011, B'0101 to B'0111 | B'xx00 | Other than B'xx00 | Other than B'xx00 | |
| CCLR1, CCLR0 | — | — | — | — | Other than B'01 | B'01 |
| Output function | — | Output compare output | — | PWM*2 mode 1 output | PWM mode 2 output | — |

[Legend]

x: Don't care

Notes: 1. TIOCA4-A input when MD3 to MD0 = B'0000 or B'01xx and IOA3 to IOA0 = B'10xx.
2. TIOCB4 output disabled.
3. When using as PO4-A output, set PPGS in PFCR3 to 0 before other register setting.
4. When using as TIOCA4-A input/output, set TPUS in PFCR3 to 0 before other register setting.
5. When using as TMO0-A output, set TMRS in PFCR3 to 0 before other register setting.
6. When using as RxD4-A input, set RXD4S in PFCR4 to 0 before other register setting.

- Modes 3, 5, and 7 (EXPE = 0)

| TPU channels 4 and 9 settings | (1) in table below | (2) in table below | | | | | | |
|---|---|---|---|---|---|---|---|---|
| OS3 to OS0 | — | All 0 | | | | | | Not all 0 |
| AMS | — | — | | | | | | — |
| CKE1 | — | 0 | | | | | 1 | — |
| C/$\overline{A}$ | — | 0 | | | | 1 | — | — |
| CKE0 | — | 0 | | | 1 | — | — | — |
| P85DDR | — | 0 | 1 | 1 | — | — | — | — |
| NDER5 | — | — | 0 | 1 | — | — | — | — |
| Pin function | TIOCB4-B/ TIOCA9-B output*6 | P85 input | P85 output | PO5-B output*5 | SCK3 output | SCK3 output | SCK3 input | TMO1-B output*7 |
| | | TIOCB4-B/TIOCA9-B input*2*3*6 | | | | | | |
| | | $\overline{IRQ5-B}$ interrupt input*1 | | | | | | |

| TPU channel 4 settings | (2) | (1) | (2) | (2) | (1) | (2) |
|---|---|---|---|---|---|---|
| MD3 to MD0 | B'0000, B'01xx | | B'0010 | B'0011 | | |
| IOB3 to IOB0 | B'0000, B'0100, B'1xxx | B'0001 to B'0011, B'0101 to B'0111 | — | B'xx00 | Other than B'xx00 | |
| CCLR1, CCLR0 | — | — | — | — | Other than B'10 | B'10 |
| Output function | — | Output compare output | — | — | PWM mode 2 output | — |

### 13.4.5 Sample Setup Procedure for Non-Overlapping Pulse Output

Figure 13.8 shows a sample procedure for setting up non-overlapping pulse output.

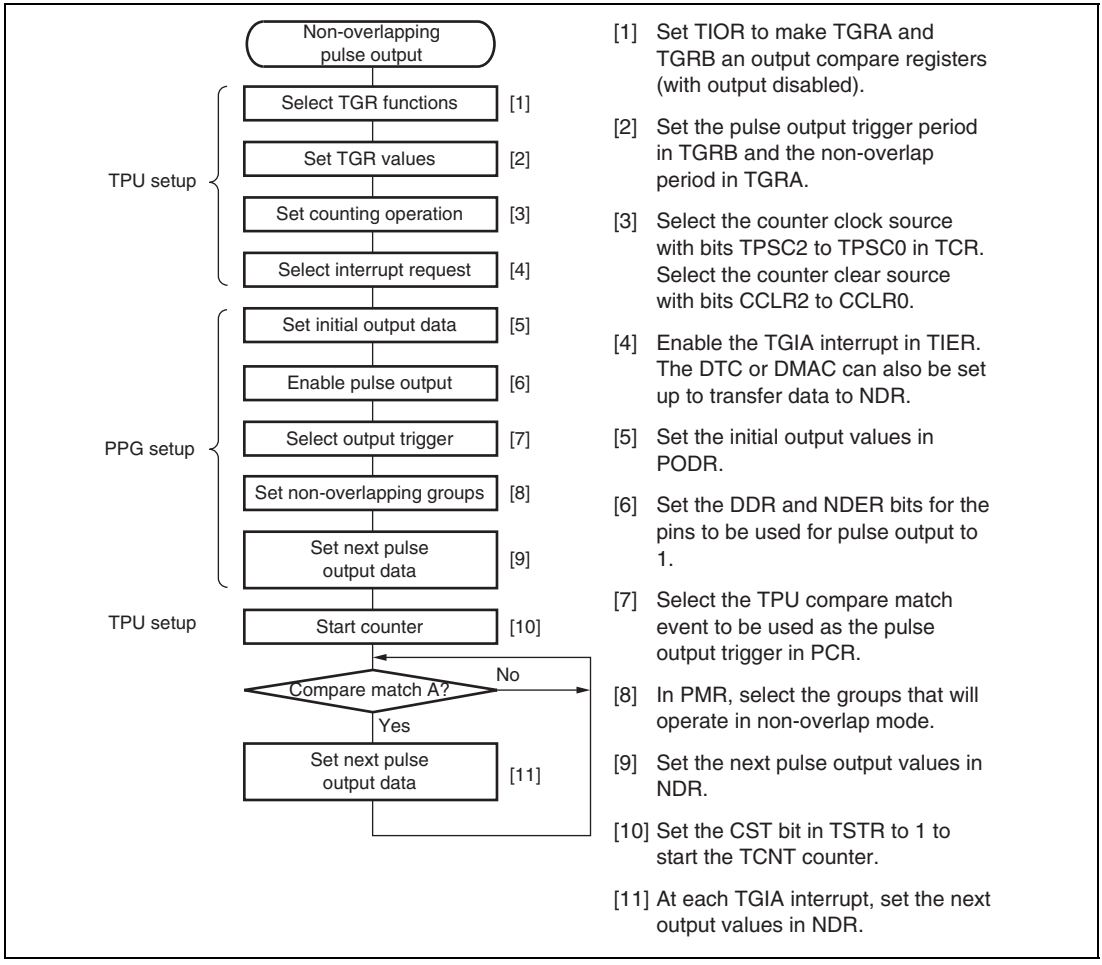



**Figure 13.8 Setup Procedure for Non-Overlapping Pulse Output (Example)**

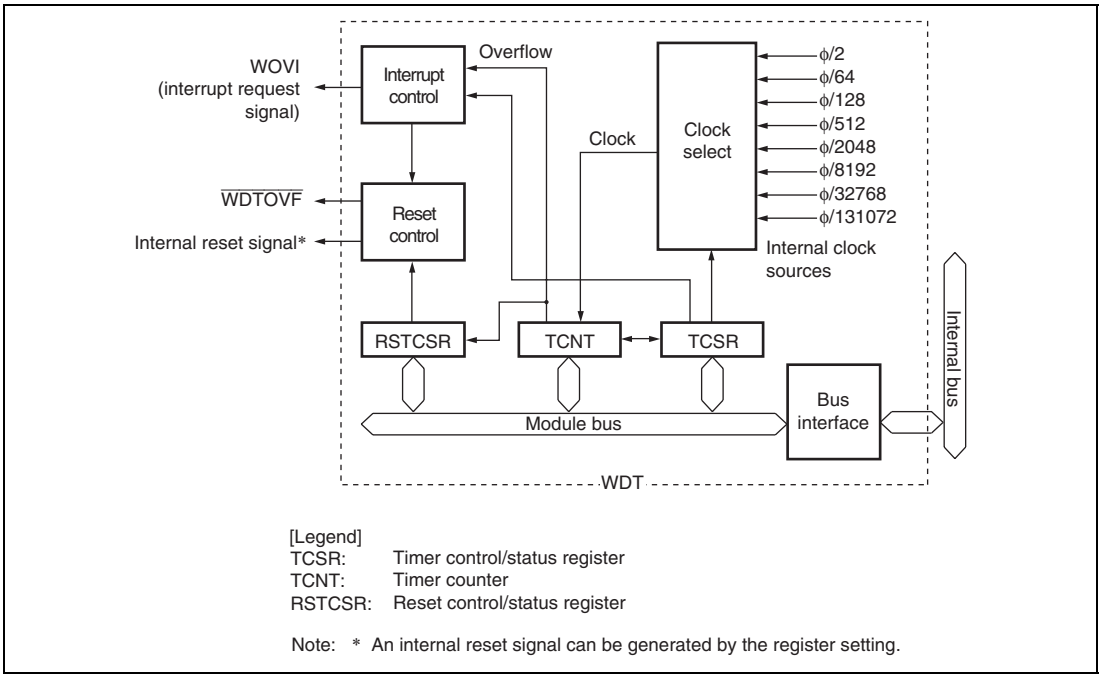



**Figure 15.1 Block Diagram of WDT**

## 15.2 Input/Output Pin

Table 15.1 shows the WDT pin configuration.

**Table 15.1 Pin Configuration**

| Name | Symbol | I/O | Function |
|---|---|---|---|
| Watchdog timer overflow | $\overline{\text{WDTOVF}}$ | Output | Outputs counter overflow signal in watchdog timer mode |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 2 | ACS2 | 0 | R/W* | Asynchronous clock source selection (valid when CKE1 = 1 in asynchronous mode) |
| 1 | ACS1 | 0 | R/W* | |
| 0 | ACS0 | 0 | R/W* | Selects the clock source for the average transfer rate.<br><br>The basic clock can be automatically set by selecting the average transfer rate in spite of the value of ABCS.<br><br>000: External clock input<br><br>001: Selects 115.152 kbps which is the average transfer rate dedicated for $\phi$= 10.667 MHz. (Operates on a basic clock with a frequency of 16 times the transfer rate.)<br><br>010: Selects 460.606 kbps which is the average transfer rate dedicated for $\phi$= 10.667 MHz. (Operates on a basic clock with a frequency of 8 times the transfer rate.)<br><br>011: Selects 720 kbps which is the average transfer rate dedicated for $\phi$ = 32 MHz. (Operates on a basic clock with a frequency of 16 times the transfer rate.)<br><br>100: Reserved<br><br>101: Selects 115.196 kbps which is the average transfer rate dedicated for $\phi$ = 16 MHz (Operates on a basic clock with a frequency of 16 times the transfer rate.)<br><br>110: Selects 460.784 kbps which is the average transfer rate dedicated for $\phi$ = 16 MHz (Operates on a basic clock with a frequency of 16 times the transfer rate.)<br><br>111: Selects 720 kbps which is the average transfer rate dedicated for $\phi$ = 16 MHz (Operates on a basic clock with a frequency of 8 times the transfer rate.)<br><br>Note that the average transfer rate does not correspond to the frequency other than 10.667, 16, or 32 MHz. |

Note: * Can be written to only when TE = RE = 0.

## 16.7 Operation in Smart Card Interface Mode

The SCI supports an IC card (Smart Card) interface conforming to ISO/IEC 7816-3 (Identification Card) as a serial communication interface extension function. Switching between the normal serial communication interface and the Smart Card interface is carried out by means of a register setting.

### 16.7.1 Connection Example and Overview of Smart Card Interface

Figure 16.21 shows an example of connection with the Smart Card. In communication with an IC card, since both transmission and reception are carried out on a single data transmission line, the TxD pin and RxD pin should be connected with the LSI pin. The data transmission line should be pulled up to the $V_{cc}$ power supply with a resistor. If an IC card is not connected, and the TE and RE bits are both set to 1, closed transmission/reception is possible, enabling self-diagnosis to be carried out. When the clock generated on the SCI is used by an IC card, the SCK pin output is input to the CLK pin of the IC card. This LSI port output is used as the reset signal.

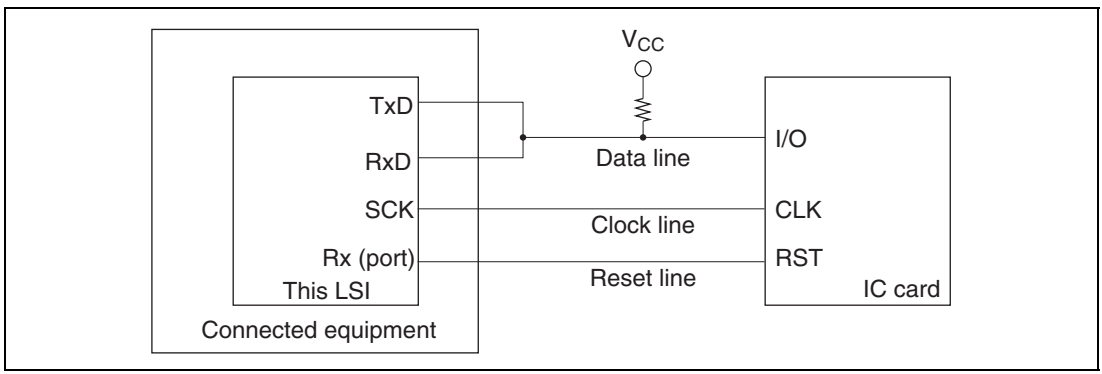



**Figure 16.21 Schematic Diagram of Smart Card Interface Pin Connections**

## 23.12 User Boot Mode

This LSI has user boot mode in which the LSI is activated with mode pin settings different from those in user program mode and boot mode. A user-arbitrary boot mode different from the boot mode using the on-chip SCI can be enabled.

Only the user ROM and data flash can be programmed/erased in user boot mode.

Programming/erasing of user boot ROM is enabled only in boot mode or programmer mode.

### (1) Initiation in User Boot Mode

When a hardware reset is issued with the mode pins set to mode 5, this LSI enters user boot mode and the built-in check routine runs. The user ROM, data flash, and user boot ROM states will be checked.

While the check routine is running, NMI and all other interrupts cannot be accepted.

Next, processing starts from the execution start address of the reset vector in user boot ROM. At this point, the FMMS bit in FLMMATS is set to 1 because user boot ROM has been selected as the execution memory MAT.

### (2) User ROM Programming in User Boot Mode

For programming the user ROM in user boot mode, additional processing made by setting the FMMS bit in FLMMATS is required: switching from the user boot ROM to the user ROM, and switching back to the user boot ROM after programming completes.

Figure 23.10 shows the procedure for programming the user ROM in user boot mode.

### (10) Erasure

Erasure is performed with the erasure selection and block erasure command.

Firstly, erasure is selected by the erasure selection command and the boot program then erases the specified block. The command should be repeatedly executed if two or more blocks are to be erased. Sending a block-erasure command from the host with the block number H'FF will stop the erasure operating. On completion of erasing, the boot program will wait for selection of programming or erasing.

The sequences of the issuing of erasure selection commands and the erasure of data are shown in figure 23.18.

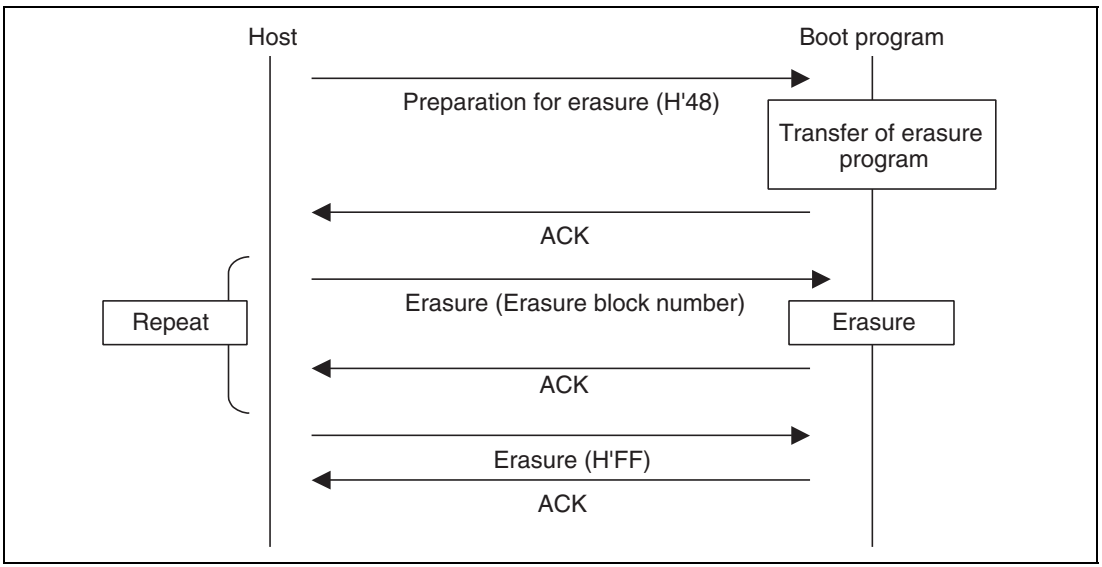



**Figure 23.18 Erasure Sequence**

| Register Abbreviation | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Module |
|---|---|---|---|---|---|---|---|---|---|
| TCNT_0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | TMR_1 |
| TCNT_1 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| TCCR0 | — | — | — | — | TMRIS | — | ICKS1 | ICKS0 | TMR_0 |
| TCCR1 | — | — | — | — | TMRIS | — | ICKS1 | ICKS0 | TMR_1 |
| TCSR | OVF | WT/IT | TME | — | — | CKS2 | CKS1 | CKS0 | WDT |
| TCNT | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| RSTCSR | WOVF | RSTE | — | — | — | — | — | — | |
| TSTR | — | — | CST5 | CST4 | CST3 | CST2 | CST1 | CST0 | TPU |
| TSYR | — | — | SYNC5 | SYNC4 | SYNC3 | SYNC2 | SYNC1 | SYNC0 | |
| CRCCR | DORCLR | — | — | — | — | LMS | G1 | G0 | |
| CRCDIR | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | |
| CRCDORH | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | |
| CRCDORL | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | |
| PFCR3 | — | PPGS | TPUS | TMRS | DMA_SEL1 | DMA_SEL0 | — | — | PORT |
| PFCR4 | WAITS | BREQS | BACKS | BREQOS | — | TXD4S | RXD4S | SCK4S | |
| PFCR5 | SSO0S1 | SSO0S0 | SSI0S1 | SSI0S0 | SSCK0S1 | SSCK0S0 | SCS0S1 | SCS0S0 | |
| TCR_0 | CCLR2 | CCLR1 | CCLR0 | CKEG1 | CKEG0 | TPSC2 | TPSC1 | TPSC0 | TPU_0 |
| TMDR_0 | — | — | BFB | BFA | MD3 | MD2 | MD1 | MD0 | |
| TIORH_0 | IOB3 | IOB2 | IOB1 | IOB0 | IOA3 | IOA2 | IOA1 | IOA0 | |
| TIORL_0 | IOD3 | IOD2 | IOD1 | IOD0 | IOC3 | IOC2 | IOC1 | IOC0 | |
| TIER_0 | TTGE | — | — | TCIEV | TGIED | TGIEC | TGIEB | TGIEA | |
| TSR_0 | — | — | — | TCFV | TGFD | TGFC | TGFB | TGFA | |
| TCNT_0 | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 | |
| | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| TGRA_0 | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 | |
| | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| TGRB_0 | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 | |
| | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| TGRC_0 | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 | |
| | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| TGRD_0 | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 | |
| | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |

**Table 27.8 Bus Timing (2)**

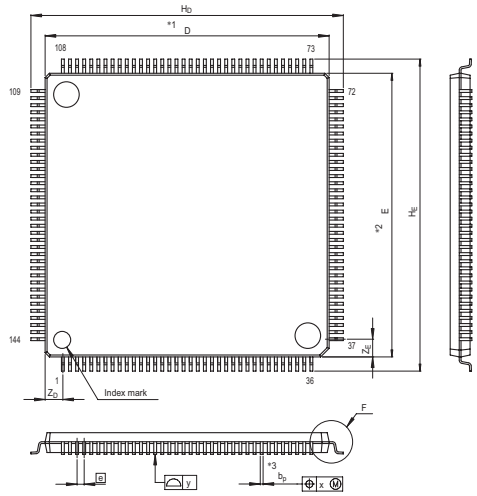
Conditions: $V_{CC}$ = 2.7 V to 3.6 V, $AV_{CC}$ = 2.7 V to 3.6 V, $V_{ref}$ = 2.7 V to $AV_{CC}$, $V_{SS} = AV_{SS}$ = 0 V, $\phi$ = 8 MHz to 25 MHz

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| $\overline{WR}$ delay time 1 | $t_{WRD1}$ | — | 15 | ns | Figures 27.10 to 27.25, 27.31 and 27.32 |
| $\overline{WR}$ delay time 2 | $t_{WRD2}$ | — | 15 | ns | |
| $\overline{WR}$ pulse width 1 | $t_{WSW1}$ | $1.0 \times t_{cyc} - 13$ | — | ns | |
| $\overline{WR}$ pulse width 2 | $t_{WSW2}$ | $1.5 \times t_{cyc} - 13$ | — | ns | |
| Write data delay time | $t_{WDD}$ | — | 23 | ns | |
| Write data setup time 1 | $t_{WDS1}$ | $0.5 \times t_{cyc} - 15$ | — | ns | |
| Write data setup time 2 | $t_{WDS2}$ | $1.0 \times t_{cyc} - 15$ | — | ns | |
| Write data setup time 3 | $t_{WDS3}$ | $1.5 \times t_{cyc} - 15$ | — | ns | |
| Write data hold time 1 | $t_{WDH1}$ | $0.5 \times t_{cyc} - 13$ | — | ns | |
| Write data hold time 2 | $t_{WDH2}$ | $1.0 \times t_{cyc} - 13$ | — | ns | |
| Write data hold time 3 | $t_{WDH3}$ | $1.5 \times t_{cyc} - 13$ | — | ns | |
| Write command setup time 1 | $t_{WCS1}$ | $0.5 \times t_{cyc} - 10$ | — | ns | |
| Write command setup time 2 | $t_{WCS2}$ | $1.0 \times t_{cyc} - 10$ | — | ns | |
| Write command hold time 1 | $t_{WCH1}$ | $0.5 \times t_{cyc} - 10$ | — | ns | |
| Write command hold time 2 | $t_{WCH2}$ | $1.0 \times t_{cyc} - 10$ | — | ns | |
| Read command setup time 1 | $t_{RCS1}$ | $1.5 \times t_{cyc} - 10$ | — | ns | |
| Read command setup time 2 | $t_{RCS2}$ | $2.0 \times t_{cyc} - 10$ | — | ns | |
| Read command hold time | $t_{RCH}$ | $0.5 \times t_{cyc} - 10$ | — | ns | |
| $\overline{CAS}$ delay time 1 | $t_{CASD1}$ | — | 15 | ns | |
| $\overline{CAS}$ delay time 2 | $t_{CASD2}$ | — | 15 | ns | |
| $\overline{CAS}$ setup time 1 | $t_{CSR1}$ | $0.5 \times t_{cyc} - 10$ | — | ns | |
| $\overline{CAS}$ setup time 2 | $t_{CSR2}$ | $1.5 \times t_{cyc} - 10$ | — | ns | |
| $\overline{CAS}$ pulse width 1 | $t_{CASW1}$ | $1.0 \times t_{cyc} - 20$ | — | ns | |
| $\overline{CAS}$ pulse width 2 | $t_{CASW2}$ | $1.5 \times t_{cyc} - 20$ | — | ns | |
| $\overline{CAS}$ precharge time 1 | $t_{CPW1}$ | $1.0 \times t_{cyc} - 20$ | — | ns | |
| $\overline{CAS}$ precharge time 2 | $t_{CPW2}$ | $1.5 \times t_{cyc} - 20$ | — | ns | |

| Port Name<br>Pin Name | MCU Operating Mode | | Reset | Hardware Standby Mode | Software Standby Mode | Bus Release State | Program Execution State<br>Sleep Mode |
|---|---|---|---|---|---|---|---|
| Port E | 1, | 8-bit bus | T | T | keep | keep | I/O port |
| | 2, 4 | 16-bit bus | T | T | T | T | D7 to D0,<br>AD7 to AD0 |
| | 3, | 8-bit bus | T | T | keep | keep | I/O port |
| | 5, 7 | 16-bit bus | T | T | [Data bus, address/data multiplexed bus]<br>T<br>[Other than the above]<br>keep | [Data bus, address/data multiplexed bus]<br>T<br>[Other than the above]<br>keep | [Data bus, address/data multiplexed bus]<br>D7 to D0, AD7 to AD0<br>[Other than the above]<br>I/O port |
| PF7/ϕ | 1, 2, 4 | | Clock output | T | [Clock output] | [Clock output] | [Clock output] |
| | 3, 5, 7 | | T | | H<br>[Other than the above]<br>keep | Clock output<br>[Other than the above]<br>keep | Clock output<br>[Other than the above]<br>Input port |
| PF6/$\overline{AS}$ | 1, 2, 4 | | H | T | [$\overline{AS}$ output, OPE = 0]<br>T<br>[$\overline{AS}$ output, OPE = 1]<br>H<br>[Other than the above]<br>keep | [$\overline{AS}$ output]<br>T<br>[Other than the above]<br>keep | [$\overline{AS}$ output]<br>$\overline{AS}$<br>[Other than the above]<br>I/O port |
| | 3, 5, 7 | | T | | | | |

# B. Package Dimensions

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP144-20x20-0.50 | PLQP0144KA-A | 144P6Q-A / FP-144L / FP-144LV | 1.2g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 19.9 | 20.0 | 20.1 |
| E | 19.9 | 20.0 | 20.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 21.8 | 22.0 | 22.2 |
| $H_E$ | 21.8 | 22.0 | 22.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.17 | 0.22 | 0.27 |
| $b_1$ | — | 0.20 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $Z_D$ | — | 1.25 | — |
| $Z_E$ | — | 1.25 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

**Figure B.1 Package Dimensions (PLQP0144KA-A)**

# Main Revisions and Additions in this Edition

| Item | Page | Revision (See Manual for Details) |
|---|---|---|
| Table 1.1 Overview of Specifications | 9 | Added |

| Module/ Type | Function | Description |
|---|---|---|
| Operating frequency/ power supply voltage | | • Operating frequency<br>2.7-V version: 8 to 25 MHz<br>3-V version: 8 to 33 MHz<br>5-V version: 8 to 33 MHz<br>• Power supply voltage<br>2.7-V version: $V_{CC}$ = 2.7 to 3.6 V, $AV_{CC}$ = 2.7 to 3.6 V<br>3-V version: $V_{CC}$ = 3.0 to 3.6 V, $AV_{CC}$ = 3.0 to 3.6 V<br>5-V version: $V_{CC}$ = 4.5 to 5.5 V, $AV_{CC}$ = 4.5 to 5.5 V<br>• Supply current<br>2.7-V version: 35 mA typ ($V_{CC}$ = 3.3 V, $AV_{CC}$ = 3.3 V, $\phi$ = 25 MHz)<br>3-V version: 45 mA typ ($V_{CC}$ = 3.3 V, $AV_{CC}$ = 3.3 V, $\phi$ = 33 MHz)<br>5-V version: 45 mA typ ($V_{CC}$ = 5.0 V, $AV_{CC}$ = 5.0 V, $\phi$ = 33 MHz) |

| Item | Page | Revision (See Manual for Details) |
|---|---|---|
| Table 16.2 Relationships between N Setting in BRR and Bit Rate B | 926 | Amended and added<br>**Bit Rate**<br>$N = \frac{\phi \times 10^6}{64 \times 2^{2n-1} \times B} - 1$<br>$N = \frac{\phi \times 10^6}{32 \times 2^{2n-1} \times B} - 1$<br>$N = \frac{\phi \times 10^6}{8 \times 2^{2n-1} \times B} - 1$<br>$N = \frac{\phi \times 10^6}{S \times 2^{2n+1} \times B} - 1$ |
| 17.7 Usage Notes | 1032, 1033 | Added<br>5. Restriction on Setting Transfer Rate in Use of Multi-Master<br>6. Restriction on Use of Bit Manipulation Instructions to Set MST and TRS in Use of Multi-Master<br>7. Note on Master Receive Mode<br>8. Notes on Changing from Master Transmit Mode to Master Receive Mode |
| 18.3.4 A/D Control Register (ADCR_0) Unit 0 | 1048, 1049 | Added<br>**Bit** / **Bit Name** / **Description**<br>7 TRGS1<br>6 TRGS0<br>0 EXTRGS<br>010: Enables A/D conversion start by external trigger from TPU (units 0 and 1)*<br>Note: * If this bit is set the same as the TRGS_1, TRGS0, and EXTRGS bits in ADCR_1, the A/D converter units 0 and 1 start A/D conversion by conversion start trigger from TPU (units 0 and 1). |