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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

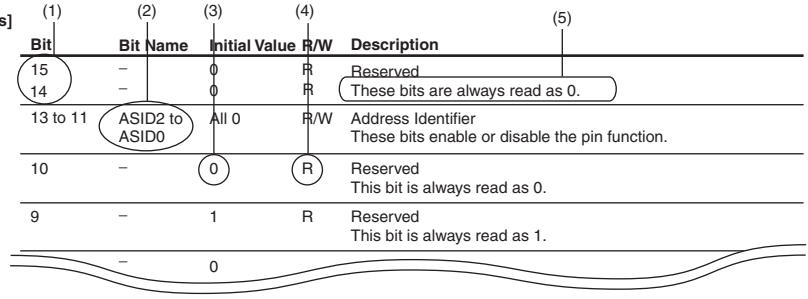
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | H8S/2600 |
| Core Size | 16-Bit |
| Speed | 33MHz |
| Connectivity | EBI/EMI, I²C, IrDA, SCI, SmartCard, SPI, SSU, UART/USART |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | 98 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 48K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 16x10b; D/A 2x8b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LFQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f24278dvrfqu |

3. Description of Registers

Each register description includes a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meanings of the bit settings. The standard format and notation for bit charts and tables are described below.

[Table of Bits]




| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 15 | – | 0 | R | Reserved |
| 14 | – | 0 | R | These bits are always read as 0. |
| 13 to 11 | ASID2 to ASID0 | All 0 | R/W | Address Identifier<br>These bits enable or disable the pin function. |
| 10 | – | 0 | R | Reserved<br>This bit is always read as 0. |
| 9 | – | 1 | R | Reserved<br>This bit is always read as 1. |
| | – | 0 | | |

Note: The bit names and sentences in the above figure are examples, and have nothing to do with the contents of this manual.

(1) Bit
Indicates the bit number or numbers.
In the case of a 32-bit register, the bits are arranged in order from 31 to 0. In the case of a 16-bit register, the bits are arranged in order from 15 to 0.

(2) Bit name
Indicates the name of the bit or bit field.
When the number of bits has to be clearly indicated in the field, appropriate notation is included (e.g., ASID[3:0]).
A reserved bit is indicated by "–".
Certain kinds of bits, such as those of timer counters, are not assigned bit names. In such cases, the entry under Bit Name is blank.

(3) Initial value
Indicates the value of each bit immediately after a power-on reset, i.e., the initial value.
0: The initial value is 0
1: The initial value is 1
–: The initial value is undefined

(4) R/W
For each bit and bit field, this entry indicates whether the bit or field is readable or writable, or both writing to and reading from the bit or field are impossible.
The notation is as follows:

R/W: The bit or field is readable and writable.
R/(W): The bit or field is readable and writable.
However, writing is only performed to flag clearing.
R: The bit or field is readable.
"R" is indicated for all reserved bits. When writing to the register, write the value under Initial Value in the bit chart to reserved bits or fields.
W: The bit or field is writable.

(5) Description
Describes the function of the bit or field and specifies the values for writing.

| Type | Module/ Function | Description |
|---|---|---|
| Timer | 16-bit timer pulse unit (TPU) | • 16-bit timer × 12 channels (general pulse timer unit)<br>• Eight counter input clocks can be selected for each channel<br>• Maximum 16-pulse input/output (when external expanded mode is set)<br>• Maximum 32-pulse input/output (when single-chip mode is set)<br>• Counter clear operation, simultaneous write to multiple timer counters (TCNT), simultaneous clearing by compare match and input capture, register simultaneous input/output possible by counter synchronous operation, and maximum of 15-phase PWM output by combination with synchronous operation<br>• Buffer operation, phase counting mode (two-phase encoder input), and cascaded operation settable for channels<br>• Input capture function<br>• Output compare function (waveform output at compare match) |
| | 8-bit timer (TMR) | • 8-bit timer × 2 channels (operation as a 16-bit timer is also possible)<br>• Selection of seven clock sources: Six internal clock signals or an external clock input<br>• Pulse output with an arbitrary duty cycle or PWM output |
| | Programmable pulse generator (PPG) | • 16-bit pulse output<br>• Pulse outputs are divided into four groups<br>Non-overlap mode is available<br>Inverted output can be specified<br>• Can operate together with the data transfer controller (DTC) and DMA controller (DMAC) |
| Watchdog timer | Watchdog timer (WDT) | • 8-bit timer × 1 channel (eight counter input clocks can be selected)<br>• Switchable between watchdog timer mode and interval timer mode |

| Product Type | Part No. | Flash Memory Size | RAM Size | Operating Voltage | Operating Environment Temperature | Package Code |
|---|---|---|---|---|---|---|
| H8S/2427 Group | R4F24279DWLPV | 512 Kbytes | 64 Kbytes | 2.7 to 3.6 V | -40 to 85°C | PTLG0145JB-A |
| | R4F24278DWLPV | 512 Kbytes | 48 Kbytes | 2.7 to 3.6 V | | |
| | R4F24276DWLPV | 384 Kbytes | 64 Kbytes | 2.7 to 3.6 V | | |
| | R4F24275DWLPV | 384 Kbytes | 48 Kbytes | 2.7 to 3.6 V | | |
| | R4F24279DVLPV | 512 Kbytes | 64 Kbytes | 3.0 to 3.6 V | | |
| | R4F24278DVLPV | 512 Kbytes | 48 Kbytes | 3.0 to 3.6 V | | |
| | R4F24276DVLPV | 384 Kbytes | 64 Kbytes | 3.0 to 3.6 V | | |
| | R4F24275DVLPV | 384 Kbytes | 48 Kbytes | 3.0 to 3.6 V | | |
| | R4F24279DLPV | 512 Kbytes | 64 Kbytes | 4.5 to 5.5 V | | |
| | R4F24278DLPV | 512 Kbytes | 48 Kbytes | 4.5 to 5.5 V | | |
| | R4F24276DLPV | 384 Kbytes | 64 Kbytes | 4.5 to 5.5 V | | |
| | R4F24275DLPV | 384 Kbytes | 48 Kbytes | 4.5 to 5.5 V | | |
| H8S/2425 Group | R4F24259NVFPU | 512 Kbytes | 64 Kbytes | 3.0 to 3.6 V | –20 to +75°C | PLQP0120LA-A |
| | R4F24258NVFPU | 512 Kbytes | 48 Kbytes | 3.0 to 3.6 V | | |
| | R4F24256NVFPU | 384 Kbytes | 64 Kbytes | 3.0 to 3.6 V | | |
| | R4F24255NVFPU | 384 Kbytes | 48 Kbytes | 3.0 to 3.6 V | | |
| | R4F24259NFPU | 512 Kbytes | 64 Kbytes | 4.5 to 5.5 V | | |
| | R4F24258NFPU | 512 Kbytes | 48 Kbytes | 4.5 to 5.5 V | | |
| | R4F24256NFPU | 384 Kbytes | 64 Kbytes | 4.5 to 5.5 V | | |
| | R4F24255NFPU | 384 Kbytes | 48 Kbytes | 4.5 to 5.5 V | | |
| | R4F24259DWFPU | 512 Kbytes | 64 Kbytes | 2.7 to 3.6 V | –40 to +85°C | |
| | R4F24258DWFPU | 512 Kbytes | 48 Kbytes | 2.7 to 3.6 V | | |
| | R4F24256DWFPU | 384 Kbytes | 64 Kbytes | 2.7 to 3.6 V | | |
| | R4F24255DWFPU | 384 Kbytes | 48 Kbytes | 2.7 to 3.6 V | | |
| | R4F24259DVFPU | 512 Kbytes | 64 Kbytes | 3.0 to 3.6 V | | |
| | R4F24258DVFPU | 512 Kbytes | 48 Kbytes | 3.0 to 3.6 V | | |
| | R4F24256DVFPU | 384 Kbytes | 64 Kbytes | 3.0 to 3.6 V | | |
| | R4F24255DVFPU | 384 Kbytes | 48 Kbytes | 3.0 to 3.6 V | | |
| | R4F24259DFPU | 512 Kbytes | 64 Kbytes | 4.5 to 5.5 V | | |
| | R4F24258DFPU | 512 Kbytes | 48 Kbytes | 4.5 to 5.5 V | | |

| Pin No. | | | Pin Name | | | |
|---|---|---|---|---|---|---|
| PLQP0120LA-A | | | | Mode 7 | | Flash Memory Programmer Mode |
| PLQP0120KA-A | Mode 1 | Mode 2 | Mode 4 | EXPE = 1 | EXPE = 0 | |
| 84 | Vcc | Vcc | Vcc | Vcc | Vcc | Vcc |
| 85 | P83/PO3-B/ TIOCD3-B/ TMCI1-B/RxD3 | P83/PO3-B/ TIOCD3-B/ TMCI1-B/RxD3 | P83/PO3-B/ TIOCD3-B/ TMCI1-B/RxD3 | P83/PO3-B/ TIOCD3-B/ TMCI1-B/RxD3 | P83/PO3-B/ TIOCD3-B/ TMCI1-B/RxD3 | NC |
| 86 | P81/PO1-B/ TIOCB3-B/ TMRI1-B/TxD3 | P81/PO1-B/ TIOCB3-B/ TMRI1-B/TxD3 | P81/PO1-B/ TIOCB3-B/ TMRI1-B/TxD3 | P81/PO1-B/ TIOCB3-B/ TMRI1-B/TxD3 | P81/PO1-B/ TIOCB3-B/ TMRI1-B/TxD3 | NC |
| 87 | Vss | Vss | Vss | Vss | Vss | Vss |
| 88 | $\overline{\text{STBY}}$ | $\overline{\text{STBY}}$ | $\overline{\text{STBY}}$ | $\overline{\text{STBY}}$ | $\overline{\text{STBY}}$ | Vcc |
| 89 | PG0/$\overline{\text{CS0}}$ | PG0/$\overline{\text{CS0}}$ | PG0/$\overline{\text{CS0}}$ | PG0/$\overline{\text{CS0}}$ | PG0 | NC |
| 90 | PG1/$\overline{\text{CS1}}$ | PG1/$\overline{\text{CS1}}$ | PG1/$\overline{\text{CS1}}$ | PG1/$\overline{\text{CS1}}$ | PG1 | NC |
| 91 | PG2/$\overline{\text{CS2}}$/$\overline{\text{RAS2}}$* | PG2/$\overline{\text{CS2}}$/$\overline{\text{RAS2}}$* | PG2/$\overline{\text{CS2}}$/$\overline{\text{RAS2}}$* | PG2/$\overline{\text{CS2}}$/$\overline{\text{RAS2}}$* | PG2 | NC |
| 92 | PG3/$\overline{\text{CS3}}$/$\overline{\text{RAS3}}$* | PG3/$\overline{\text{CS3}}$/$\overline{\text{RAS3}}$* | PG3/$\overline{\text{CS3}}$/$\overline{\text{RAS3}}$* | PG3/$\overline{\text{CS3}}$/$\overline{\text{RAS3}}$* | PG3 | NC |
| 93 | AVcc | AVcc | AVcc | AVcc | AVcc | Vcc |
| 94 | Vref | Vref | Vref | Vref | Vref | Vcc |
| 95 | P40/$\overline{\text{IRQ0-B}}$/AN0_0 | P40/$\overline{\text{IRQ0-B}}$/AN0_0 | P40/$\overline{\text{IRQ0-B}}$/AN0_0 | P40/$\overline{\text{IRQ0-B}}$/AN0_0 | P40/$\overline{\text{IRQ0-B}}$/AN0_0 | NC |
| 96 | P41/$\overline{\text{IRQ1-B}}$/AN1_0 | P41/$\overline{\text{IRQ1-B}}$/AN1_0 | P41/$\overline{\text{IRQ1-B}}$/AN1_0 | P41/$\overline{\text{IRQ1-B}}$/AN1_0 | P41/$\overline{\text{IRQ1-B}}$/AN1_0 | NC |
| 97 | P42/$\overline{\text{IRQ2-B}}$/AN2_0 | P42/$\overline{\text{IRQ2-B}}$/AN2_0 | P42/$\overline{\text{IRQ2-B}}$/AN2_0 | P42/$\overline{\text{IRQ2-B}}$/AN2_0 | P42/$\overline{\text{IRQ2-B}}$/AN2_0 | NC |
| 98 | P43/$\overline{\text{IRQ3-B}}$/AN3_0 | P43/$\overline{\text{IRQ3-B}}$/AN3_0 | P43/$\overline{\text{IRQ3-B}}$/AN3_0 | P43/$\overline{\text{IRQ3-B}}$/AN3_0 | P43/$\overline{\text{IRQ3-B}}$/AN3_0 | Vss |
| 99 | P44/$\overline{\text{IRQ4-B}}$/AN4_0 | P44/$\overline{\text{IRQ4-B}}$/AN4_0 | P44/$\overline{\text{IRQ4-B}}$/AN4_0 | P44/$\overline{\text{IRQ4-B}}$/AN4_0 | P44/$\overline{\text{IRQ4-B}}$/AN4_0 | Vcc |
| 100 | P45/$\overline{\text{IRQ5-B}}$/AN5_0 | P45/$\overline{\text{IRQ5-B}}$/AN5_0 | P45/$\overline{\text{IRQ5-B}}$/AN5_0 | P45/$\overline{\text{IRQ5-B}}$/AN5_0 | P45/$\overline{\text{IRQ5-B}}$/AN5_0 | Vss |
| 101 | P46/$\overline{\text{IRQ6-B}}$/AN6_0 | P46/$\overline{\text{IRQ6-B}}$/AN6_0 | P46/$\overline{\text{IRQ6-B}}$/AN6_0 | P46/$\overline{\text{IRQ6-B}}$/AN6_0 | P46/$\overline{\text{IRQ6-B}}$/AN6_0 | NC |
| 102 | P47/$\overline{\text{IRQ7-B}}$/AN7_0 | P47/$\overline{\text{IRQ7-B}}$/AN7_0 | P47/$\overline{\text{IRQ7-B}}$/AN7_0 | P47/$\overline{\text{IRQ7-B}}$/AN7_0 | P47/$\overline{\text{IRQ7-B}}$/AN7_0 | NC |
| 103 | P94/AN12_1/DA2 | P94/AN12_1/DA2 | P94/AN12_1/DA2 | P94/AN12_1/DA2 | P94/AN12_1/DA2 | NC |
| 104 | P95/AN13_1/DA3 | P95/AN13_1/DA3 | P95/AN13_1/DA3 | P95/AN13_1/DA3 | P95/AN13_1/DA3 | NC |
| 105 | AVss | AVss | AVss | AVss | AVss | Vss |
| 106 | PG4/$\overline{\text{BREQO-A}}$/ $\overline{\text{CS4}}$ | PG4/$\overline{\text{BREQO-A}}$/ $\overline{\text{CS4}}$ | PG4/$\overline{\text{BREQO-A}}$/ $\overline{\text{CS4}}$ | PG4/$\overline{\text{BREQO-A}}$/ $\overline{\text{CS4}}$ | PG4 | NC |
| 107 | PG5/$\overline{\text{BACK-A}}$ | PG5/$\overline{\text{BACK-A}}$ | PG5/$\overline{\text{BACK-A}}$ | PG5/$\overline{\text{BACK-A}}$ | PG5 | NC |
| 108 | PG6/$\overline{\text{BREQ-A}}$ | PG6/$\overline{\text{BREQ-A}}$ | PG6/$\overline{\text{BREQ-A}}$ | PG6/$\overline{\text{BREQ-A}}$ | PG6 | NC |

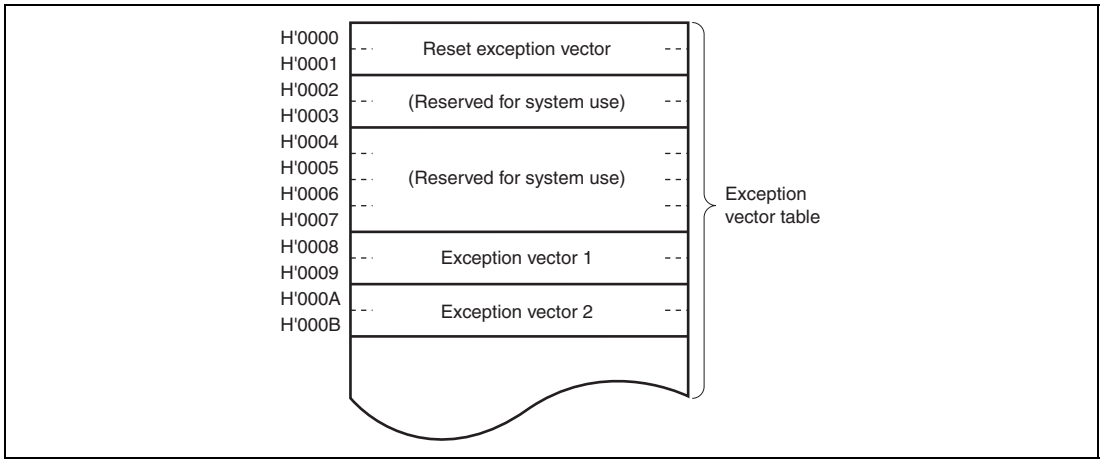



**Figure 2.1 Exception Vector Table (Normal Mode)**

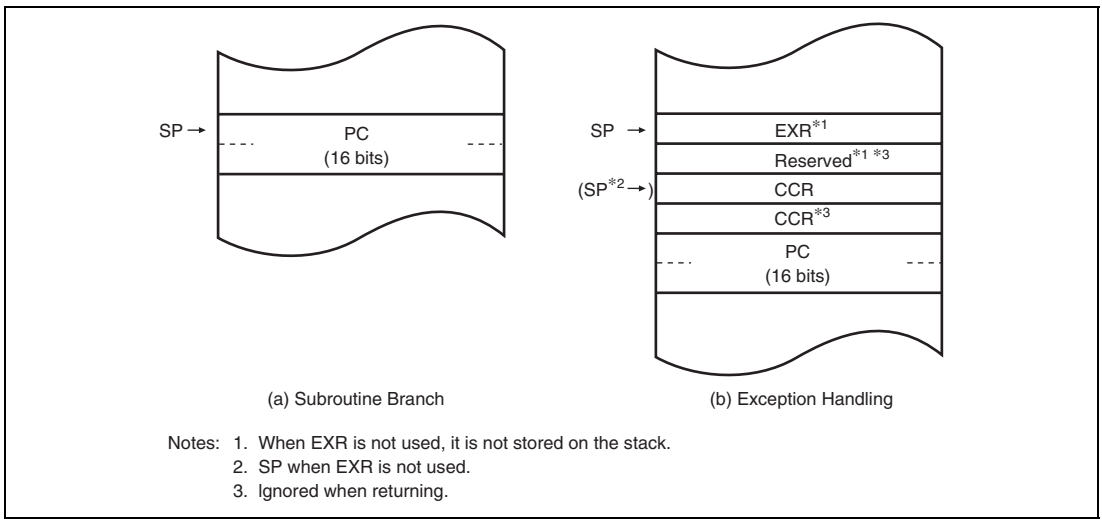



**Figure 2.2 Stack Structure in Normal Mode**

Note that some registers are not initialized by any of the resets. The following describes the CPU internal registers.

The PC, one of the CPU internal registers, is initialized by loading the start address from vector addresses with the reset exception handling. At this time, the T bit in EXR is cleared to 0 and the I bits in EXR and CCR are set to 1. The general registers and other bits in CCR are not initialized.

The initial value of the SP (ER7) is undefined. The SP should be initialized using the MOV.L instruction immediately after a reset. For details, see section 2, CPU. For other registers that are not initialized by a reset, see register descriptions in each section.

When a reset is canceled, the reset exception handling is started. For the reset exception handling, see section 5, Exception Handling.

## 4.2 Input/Output Pin

Table 4.2 shows the pin related to resets.

**Table 4.2 Pin Configuration**

| Pin Name | Symbol | I/O | Function |
|---|---|---|---|
| Reset | $\overline{\text{RES}}$ | Input | Reset input |

## 8.3 Register Descriptions

The DMAC has the following registers.

- Memory address register 0 (MAR0)
- I/O address register 0 (IOAR0)
- Transfer count register 0 (ETCR0)
- DMA control register S0 (DMACRS0)
- DMA enable control register S0 (DMAECRS0)
- DMA register control register 0 (DMARCR0)
- Memory address register 1 (MAR1)
- I/O address register 1 (IOAR1)
- Transfer count register 1 (ETCR1)
- DMA control register S1 (DMACRS1)
- DMA enable control register S1 (DMAECRS1)
- DMA register control register 1 (DMARCR1)
- Memory address register 2 (MAR2)
- I/O address register 2 (IOAR2)
- Transfer count register 2 (ETCR2)
- DMA control register S2 (DMACRS2)
- DMA enable control register S2 (DMAECRS2)
- DMA register control register 2 (DMARCR2)
- Memory address register 3 (MAR3)
- I/O address register 3 (IOAR3)
- Transfer count register 3 (ETCR3)
- DMA control register S3 (DMACRS3)
- DMA enable control register S3 (DMAECRS3)
- DMA register control register 3 (DMARCR3)
- Source address register 4 (SAR4)
- Destination address register 4 (DAR4)
- Transfer count register A4 (ETCRA4)
- Transfer count register B4 (ETCRB4)
- DMA control register F4 (DMACRF4)
- DMA enable control register F4 (DMAECRF4)
- DMA register control register 4 (DMARCR4)

Transfer requests (activation sources) consist of A/D converter conversion end interrupts, external requests, SCI transmit data empty and receive data full interrupts, and TPU channel 0 to 5 compare match/input capture A interrupts.

Figures 8.20 and 8.21 show an example of the setting procedure for block transfer mode in common register enabled mode and common register disabled mode, respectively.

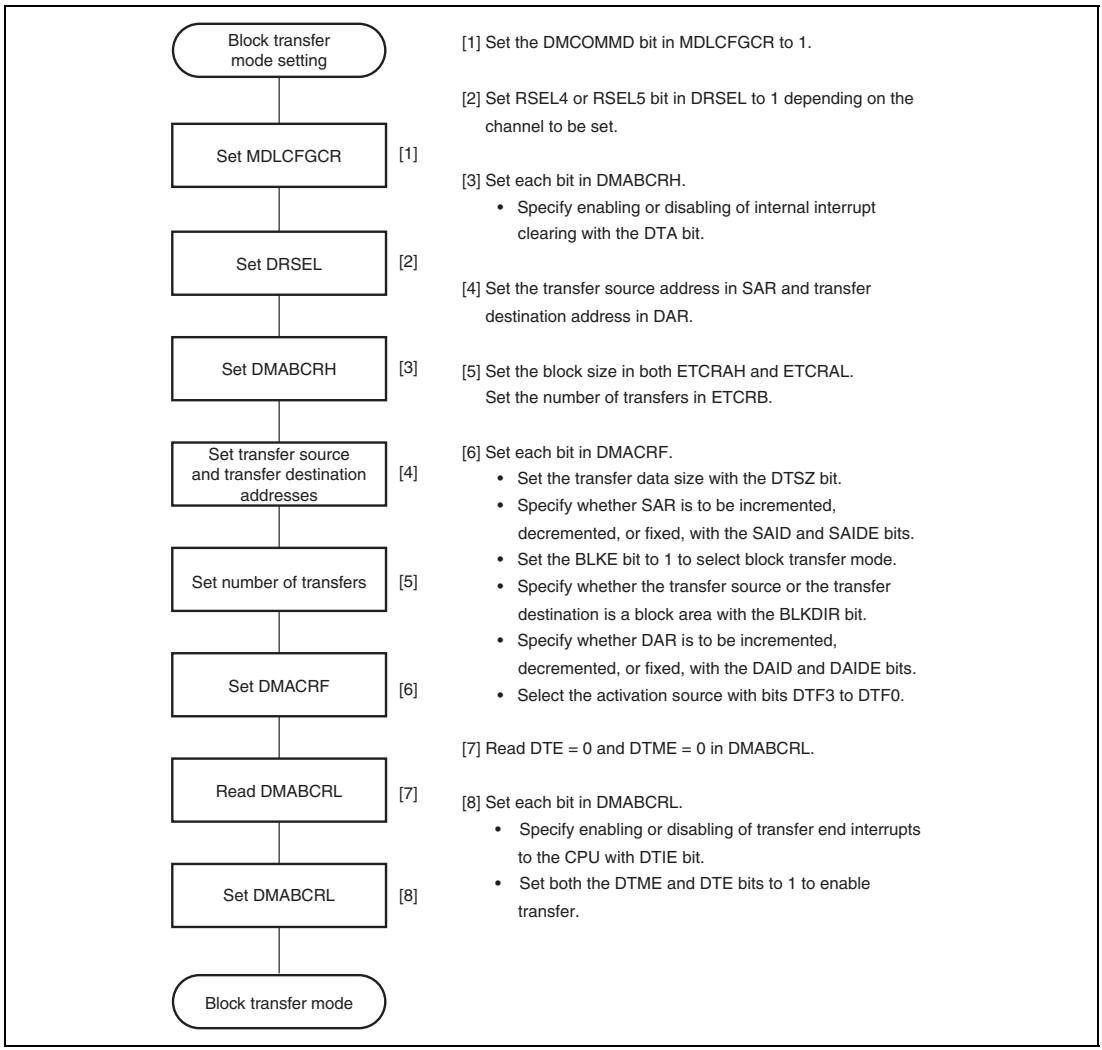



**Figure 8.20 Example of Block Transfer Mode Setting Procedure (Common Register Enabled Mode)**

Figure 9.11 shows EDTCR update operations in normal transfer mode and block transfer mode.

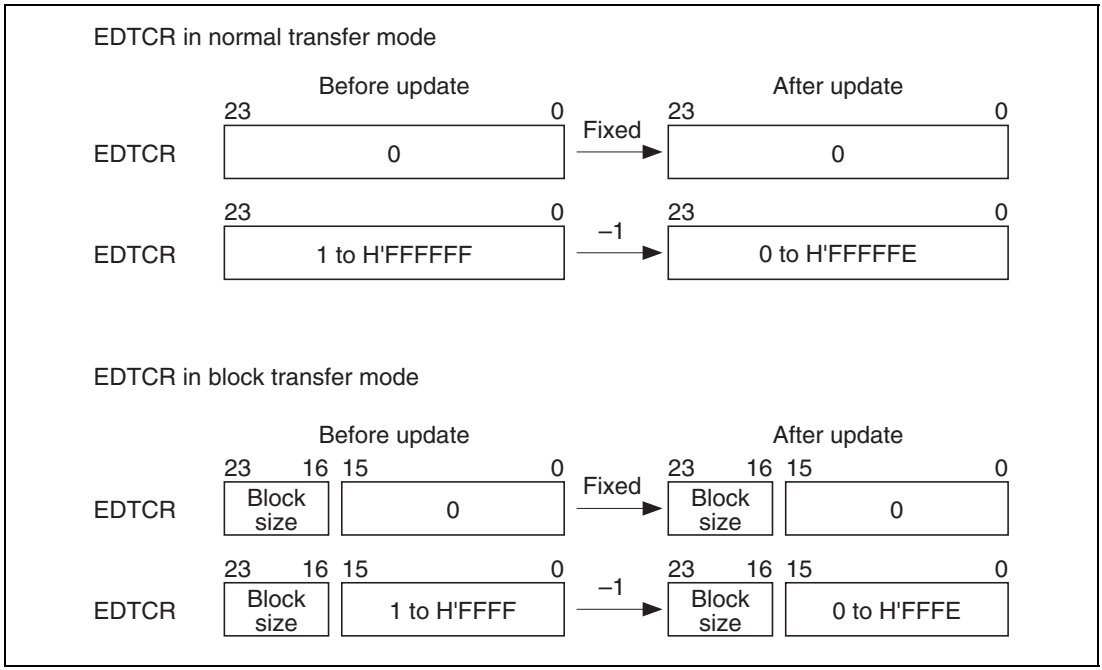



**Figure 9.11 EDTCR Update Operations in Normal Transfer Mode and Block Transfer Mode**

### (4) EDA Bit in EDMDR

The EDA bit in EDMDR is written to by the CPU to control enabling and disabling of data transfer, but may be cleared automatically by the EXDMAC due to the EXDMA transfer status. There are also periods during transfer when a 0-write to the EDA bit by the CPU is not immediately effective.

Conditions for EDA bit clearing by the EXDMAC include the following:

- When the EDTCR value changes from 1 to 0, and transfer ends
- When a repeat area overflow interrupt is requested, and transfer ends
- When an NMI interrupt is generated, and transfer halts
- A reset
- Hardware standby mode
- When 0 is written to the EDA bit, and transfer halts

### 11.1.4 Port 1 Open Drain Control Register (P1ODR)

P1ODR specifies the output type of each port 1 pin.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | P17ODR | 0 | R/W | Setting a P1ODR bit to 1 makes the corresponding pin an NMOS open-drain output pin, while clearing a P1ODR bit to 0 makes the corresponding pin a CMOS output pin. |
| 6 | P16ODR | 0 | R/W | |
| 5 | P15ODR | 0 | R/W | |
| 4 | P14ODR | 0 | R/W | |
| 3 | P13ODR | 0 | R/W | |
| 2 | P12ODR | 0 | R/W | |
| 1 | P11ODR | 0 | R/W | |
| 0 | P10ODR | 0 | R/W | |

### 11.7.2 Port 8 Data Register (P8DR)

P8DR stores output data for the port 8 pins.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7, 6 | — | All 0 | — | Reserved<br>These bits are always read as 0 and cannot be modified. |
| 5 | P85DR | 0 | R/W | Output data for a pin is stored when the pin function is specified as a general purpose I/O.<br>Bits 4, 2, and 0 are reserved in the H8S/2425 Group. |
| 4 | P84DR | 0 | R/W | |
| 3 | P83DR | 0 | R/W | |
| 2 | P82DR | 0 | R/W | |
| 1 | P81DR | 0 | R/W | |
| 0 | P80DR | 0 | R/W | |

### 11.7.3 Port 8 Register (PORT8)

PORT8 shows the pin states of port 8. PORT8 cannot be modified.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7, 6 | — | Undefined | — | Reserved<br>If these bits are read, they will return an undefined value. |
| 5 | P85 | —* | R | If this register is read while a P8DDR bit is set to 1, the corresponding P8DR value is read. If this register is read while a P8DDR bit is cleared to 0, the corresponding pin state is read.<br>Bits 4, 2, and 0 are reserved in the H8S/2425 Group. |
| 4 | P84 | —* | R | |
| 3 | P83 | —* | R | |
| 2 | P82 | —* | R | |
| 1 | P81 | —* | R | |
| 0 | P80 | —* | R | |

Note: * Determined by the states of pins P85 to P80.

### 11.17.3 Port J Register (PORTJ)

PORTJ shows the pin states of port J. PORTJ cannot be modified.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 to 3 | — | Undefined | — | Reserved<br>If these bits are read, they will return an undefined value. |
| 2 | PJ2 | —* | R | [PLQP0144KA-A package]<br>The pin states are read.<br>[PTLG0145JB-A package]<br>Reserved. If this bit is read, it will return an undefined value. |
| 1 | PJ1 | —* | R | If this register is read, the PJDR values are read for the bits with the corresponding PJDDR bits set to 1. For the bits with the corresponding PJDDR bits cleared to 0, the pin states are read. |
| 0 | PJ0 | —* | R | |

Note: * Determined by the state of pins PJ0 to PJ2.

### 11.17.4 Port J Open Drain Control Register (PJODR)

PJODR specifies the output type of each port J pin.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 to 2 | — | All 0 | — | Reserved<br>These bits are always read as 0. Only the initial values should be written to these bits. |
| 1 | PJ1ODR | 0 | R/W | Setting a PJODR bit to 1 makes the corresponding pin an NMOS open-drain output pin, while clearing a PJODR bit to 0 makes the corresponding pin a CMOS output pin. |
| 0 | PJ0ODR | 0 | R/W | |

## 16.11 CRC Operation Circuit

The cyclic redundancy check (CRC) operation circuit detects errors in data blocks.

### 16.11.1 Features

- CRC code generated for any desired data length in an 8-bit unit
- CRC operation executed on eight bits in parallel
- One of three generating polynomials selectable
- CRC code generation for LSB-first or MSB-first Communication selectable

Figure 19.40 shows a block diagram of the CRC operation circuit.

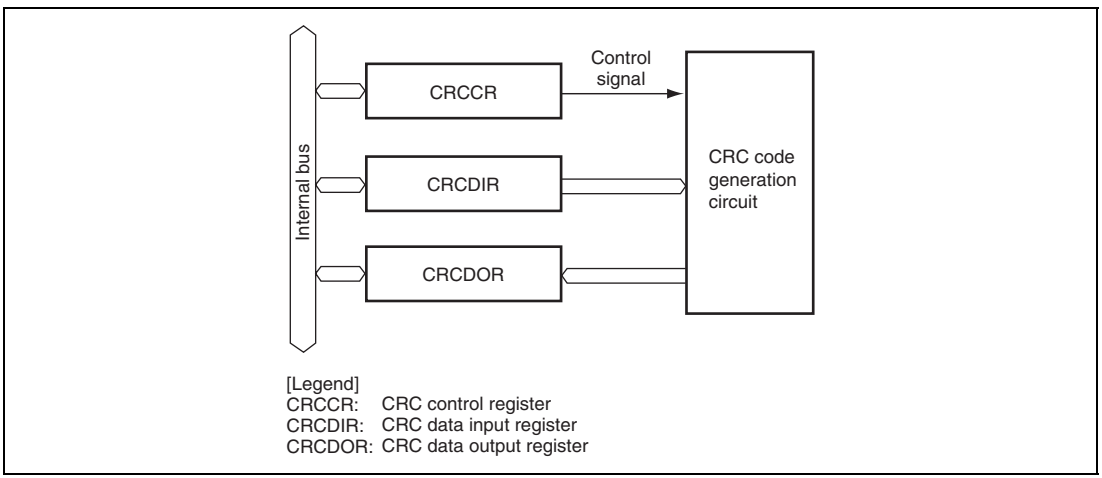



**Figure 19.40 Block Diagram of CRC Operation Circuit**

### (4) Inquiry/Selection State

The boot program returns information from the flash memory in response to the host's inquiry commands and sets the device code, clock mode, and bit rate in response to the host's selection command.

Inquiry and selection commands are listed in table 23.9.

**Table 23.9 Inquiry and Selection Commands**

| Command | Command Name | Description |
|---|---|---|
| H'20 | Supported device inquiry | Inquiry regarding device codes and product name |
| H'10 | Device selection | Selection of device code |
| H'21 | Clock mode inquiry | Inquiry regarding numbers of clock modes and values of each mode |
| H'11 | Clock mode selection | Indication of the selected clock mode |
| H'22 | Multiplication ratio inquiry | Inquiry regarding the number of frequency-multiplied clock types, the number of multiplication ratios, and the values of each multiple |
| H'23 | Operating clock frequency Inquiry | Inquiry regarding the maximum and minimum values of the main clock and peripheral clocks |
| H'24 | User boot ROM information inquiry | Inquiry regarding the number of user boot ROM areas and the start and last addresses of each user boot ROM area |
| H'25 | User ROM information inquiry | Inquiry regarding the number of user ROM areas and the start and last addresses of each user ROM area |
| H'2B | Data flash information inquiry | Inquiry regarding the number of data flash areas and the start and last addresses of each data flash area |
| H'26 | Erased block information inquiry | Inquiry regarding the number of blocks and the start and last addresses of each block |
| H'27 | Programming unit inquiry | Inquiry regarding the unit of programming data |
| H'3F | New bit rate selection | Selection of new bit rate |
| H'40 | Transition to programming/erasing state | Erasing of user ROM and entry to programming/erasing state |
| H'4F | Boot program status inquiry | Inquiry regarding the operated status of the boot program |

### (4) DMAC and EXDMAC Timing

**Table 27.60 DMAC and EXDMAC Timing**

Conditions: $V_{CC}$ = 4.5 V to 5.5 V, $AV_{CC}$ = 4.5 V to 5.5 V, $V_{ref}$ = 4.5 V to $AV_{CC}$, $V_{SS}$ = $AV_{SS}$ = 0 V, $\phi$ = 8 MHz to 33 MHz

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| $\overline{\text{DREQ}}$ setup time | $t_{DRQS}$ | 25 | — | ns | Figure 27.75 |
| $\overline{\text{DREQ}}$ hold time | $t_{DRQH}$ | 10 | — | | |
| $\overline{\text{TEND}}$ delay time | $t_{TED}$ | — | 18 | ns | Figure 27.74 |
| $\overline{\text{DACK}}$ delay time 1 | $t_{DACD1}$ | — | 18 | | Figures 27.72 and 27.73 |
| $\overline{\text{DACK}}$ delay time 2 | $t_{DACD2}$ | — | 18 | | |
| $\overline{\text{EDREQ}}$ setup time | $t_{EDRQS}$ | 25 | — | ns | Figure 27.75 |
| $\overline{\text{EDREQ}}$ hold time | $t_{EDRQH}$ | 10 | — | | |
| $\overline{\text{ETEND}}$ delay time | $t_{ETED}$ | — | 18 | ns | Figure 27.74 |
| $\overline{\text{EDACK}}$ delay time 1 | $t_{EDACD1}$ | — | 18 | ns | Figures 27.72 and 27.73 |
| $\overline{\text{EDACK}}$ delay time 2 | $t_{EDACD2}$ | — | 18 | | |
| $\overline{\text{EDRAK}}$ delay time | $t_{EDRKD}$ | — | 18 | ns | Figure 27.76 |

## (5) Timing of On-Chip Peripheral Modules

### Table 27.61 Timing of On-Chip Peripheral Modules

Conditions: $V_{CC}$ = 4.5 V to 5.5 V, $AV_{CC}$ = 4.5 V to 5.5 V, $V_{ref}$ = 4.5 V to $AV_{CC}$, $V_{SS}$ = $AV_{SS}$ = 0 V, $\phi$ = 8 MHz to 33 MHz

| Item | | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| I/O ports | Output data delay time | | $t_{PWD}$ | — | 40 | ns | Figure 27.77 |
| | Input data setup time | | $t_{PRS}$ | 25 | — | ns | |
| | Input data hold time | | $t_{PRH}$ | 25 | — | ns | |
| PPG | Pulse output delay time | | $t_{POD}$ | — | 40 | ns | Figure 27.78 |
| TPU | Timer output delay time | | $t_{TOCD}$ | — | 40 | ns | Figure 27.79 |
| | Timer input setup time | | $t_{TICS}$ | 25 | — | ns | |
| | Timer clock input setup time | | $t_{TCKS}$ | 25 | — | ns | Figure 27.80 |
| | Timer clock pulse width | Single-edge specification | $t_{TCKWH}$ | 1.5 | — | $t_{cyc}$ | |
| | | Both-edge specification | $t_{TCKWL}$ | 2.5 | — | $t_{cyc}$ | |
| 8-bit timer | Timer output delay time | | $t_{TMOD}$ | — | 40 | ns | Figure 27.81 |
| | Timer reset input setup time | | $t_{TMRS}$ | 25 | — | ns | Figure 27.83 |
| | Timer clock input setup time | | $t_{TMCS}$ | 25 | — | ns | Figure 27.82 |
| | Timer clock pulse width | Single-edge specification | $t_{TMCWH}$ | 1.5 | — | $t_{cyc}$ | |
| | | Both-edge specification | $t_{TMCWL}$ | 2.5 | — | $t_{cyc}$ | |
| WDT | Overflow output delay time | | $t_{WOVD}$ | — | 40 | ns | Figure 27.84 |
| SCI | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | $t_{cyc}$ | Figure 27.85 |
| | | Synchronous | | 6 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rising time | | $t_{SCKr}$ | — | 1.5 | $t_{cyc}$ | |
| | Input clock falling time | | $t_{SCKf}$ | — | 1.5 | | |
| | Transmit data delay time | | $t_{TXD}$ | — | 40 | ns | Figure 27.86 |
| | Receive data setup time (synchronous) | | $t_{RXS}$ | 40 | — | ns | |
| | Receive data hold time (synchronous) | | $t_{RXH}$ | 40 | — | ns | |

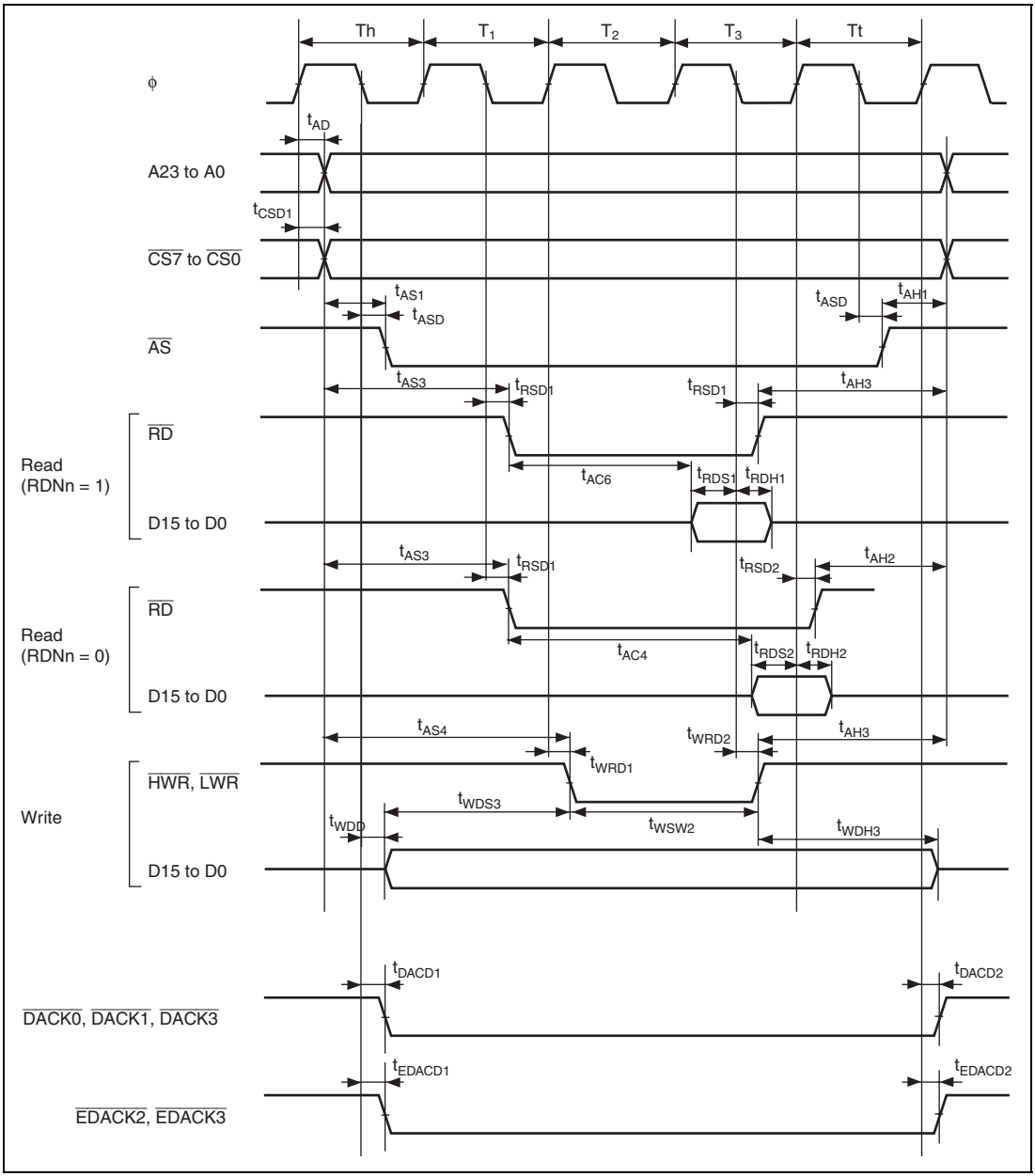



**Figure 27.65 Basic Bus Timing: Three-State Access ($\overline{CS}$ Assertion Period Extended)**

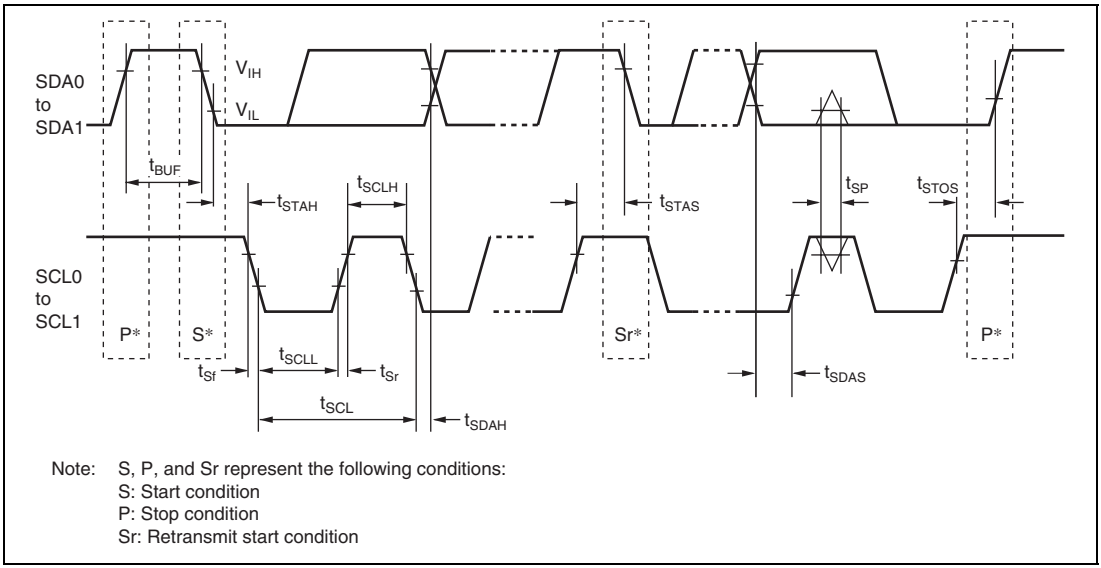



**Figure 27.88 I²C Bus Interface 2 Input/Output Timing**

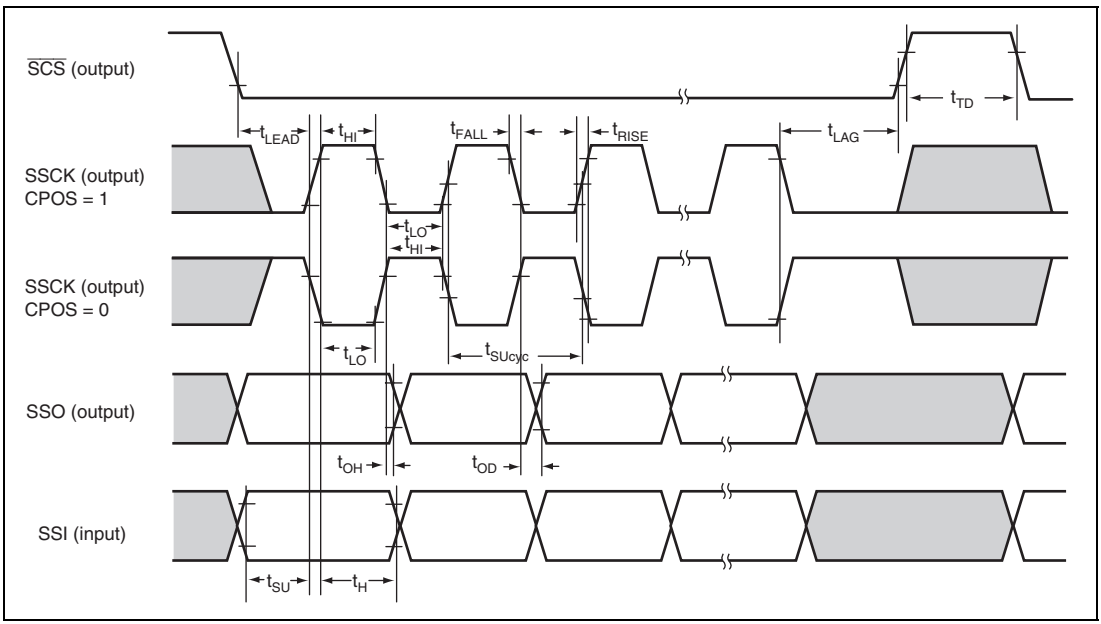



**Figure 27.89 SSU Timing (Master, CPHS = 1)**

| Item | Page | Revision (See Manual for Details) |
|---|---|---|
| • P21/PO1-A/ TIOCB3-A/ TMRI1-A | 600 | Notes amended<br>3. When using as PO1-A output, set PPGS in PFCR3 to 0 before other register setting.<br>4. When using as TIOCB3-A input/output, set TPUS in PFCR3 to 0 before other register setting.<br>5. When using as TMRI1-A input, set TMRS in PFCR3 to 0 before other register setting. |
| • P20/PO0-A/ TIOCA3-A/ TMRI0-A | 601 | Notes amended<br>4. When using as PO0-A output, set PPGS in PFCR3 to 0 before other register setting.<br>5. When using as TIOCA3-A input/output, set TPUS in PFCR3 to 0 before other register setting.<br>6. When using as TMRI0-A input, set TMRS in PFCR3 to 0 before other register setting. |
| 11.5.5 Pin Functions<br>• P52/SCK2/ $\overline{\text{IRQ2-A}}$/ $\overline{\text{BACK-B}}$/PO4-B/ TIOCA4-B/ TMO0-B<br>• Modes 3, 5, and 7 (EXPE = 0) | 614 | Notes amended<br>4. When using as PO4-B output, set PPGS in PFCR3 to 1 before other register setting.<br>5. When using as TIOCA4-B input/output, set TPUS in PFCR3 to 1 before other register setting.<br>6. When using as TMO0-B output, set TMRS in PFCR3 to 1 before other register setting. |
| • P51/RxD2/ $\overline{\text{IRQ1-A}}$/SCL3/ $\overline{\text{BREQ-B}}$/PO2-B/ TIOCC3-B/ TMCI0-B<br>• Modes 3, 5, and 7 (EXPE = 0) | 616 | Notes amended<br>6. When using as PO2-B output, set PPGS in PFCR3 to 1 before other register setting.<br>7. When using as TIOCC3-B input/output, set TPUS in PFCR3 to 1 before other register setting.<br>8. When using as TMCI0-B input, set TMRS in PFCR3 to 1 before other register setting. |
| • P50/TxD2/ $\overline{\text{IRQ0-A}}$/SDA3/ $\overline{\text{BREQO-B}}$/ PO0-B/ TIOCA3-B/ TMRI0-B<br>• Modes 3, 5, and 7 (EXPE = 0) | 618 | Notes amended<br>6. When using as PO0-B output, set PPGS in PFCR3 to 1 before other register setting.<br>7. When using as TIOCA3-B input/output, set TPUS in PFCR3 to 1 before other register setting.<br>8. When using as TMRI0-B input, set TMRS in PFCR3 to 1 before other register setting. |

| Item | Page | Revision (See Manual for Details) |
|---|---|---|
| • PF2/$\overline{\text{CS6}}$/ $\overline{\text{LCAS}}$*5/SSI0-C (H8S/2425 Group)<br>• Modes 3, 5, and 7 (EXPE = 0) | 701 | Notes amended<br>1. When using as SSI0-C input, set SSI0S1 and SSI0S0 in PFCR5 to B'10 before other register setting.<br>2. When using as SSI0-C output, set SSI0S1 and SSI0S0 in PFCR5 to B'10 before other register setting. |
| • PF1/$\overline{\text{UCAS}}$*6/ DQMU*7/ $\overline{\text{IRQ14-A}}$/ SSCK0-C (H8S/2427 Group and H8S/2426R Group)<br>• Modes 3, 5, and 7 (EXPE = 0) | 702 | Notes amended<br>2. When using as SSCK0-C input, set SSCK0S1 and SSCK0S0 in PFCR5 to B'10 before other register setting.<br>3. When using as SSCK0-C output, set SSCK0S1 and SSCK0S0 in PFCR5 to B'10 before other register setting. |
| • PF1/$\overline{\text{CS5}}$/ $\overline{\text{UCAS}}$*5/ SSCK0-C (H8S/2425 Group)<br>• Modes 3, 5, and 7 (EXPE = 0) | 704 | Notes amended<br>1. When using as SSCK0-C input, set SSCK0S1 and SSCK0S0 in PFCR5 to B'10 before other register setting.<br>2. When using as SSCK0-C output, set SSCK0S1 and SSCK0S0 in PFCR5 to B'10 before other register setting. |
| • PF0/$\overline{\text{WAIT-A}}$/ $\overline{\text{ADTRG0-B}}$/ $\overline{\text{SCS0-C}}$ (H8S/2427 Group and H8S/2427R Group)<br>• Modes 3, 5, and 7 (EXPE = 0) | 706 | Notes amended<br>2. When using as $\overline{\text{SCS0-C}}$ input, set SCS0S1 and SCS0S0 in PFCR5 to B'10 before other register setting.<br>3. When using as $\overline{\text{SCS0-C}}$ output, set SCS0S1 and SCS0S0 in PFCR5 to B'10 before other register setting.<br>4. When using as $\overline{\text{SCS0-C}}$ input/output, set SCS0S1 and SCS0S0 in PFCR5 to B'10 before other register setting. |
| • PF0/$\overline{\text{WAIT-A}}$/ $\overline{\text{ADTRG0-B}}$/ $\overline{\text{SCS0-C}}$/ $\overline{\text{OE-A}}$*8 (H8S/2425 Group)<br>• Modes 3, 5, and 7 (EXPE = 0) | 708 | Notes amended<br>3. When using as $\overline{\text{SCS0-C}}$ input, set SCS0S1 and SCS0S0 in PFCR5 to B'10 before other register setting.<br>4. When using as $\overline{\text{SCS0-C}}$ output, set SCS0S1 and SCS0S0 in PFCR5 to B'10 before other register setting.<br>5. When using as $\overline{\text{SCS0-C}}$ input/output, set SCS0S1 and SCS0S0 in PFCR5 to B'10 before other register setting. |