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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2600
Core Size	16-Bit
Speed	33MHz
Connectivity	EBI/EMI, I²C, IrDA, SCI, SmartCard, SPI, SSU, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	98
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f24278nvfqu

Bit	Bit Name	Initial Value	R/W	Description
9	IRQ4SCB	0	R/W	IRQ4 Sense Control B
8	IRQ4SCA	0	R/W	IRQ4 Sense Control A 00: Interrupt request generated at $\overline{\text{IRQ4}}$ input low level 01: Interrupt request generated at falling edge of $\overline{\text{IRQ4}}$ input 10: Interrupt request generated at rising edge of $\overline{\text{IRQ4}}$ input 11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ4}}$ input
7	IRQ3SCB	0	R/W	IRQ3 Sense Control B
6	IRQ3SCA	0	R/W	IRQ3 Sense Control A 00: Interrupt request generated at $\overline{\text{IRQ3}}$ input low level 01: Interrupt request generated at falling edge of $\overline{\text{IRQ3}}$ input 10: Interrupt request generated at rising edge of $\overline{\text{IRQ3}}$ input 11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ3}}$ input
5	IRQ2SCB	0	R/W	IRQ2 Sense Control B
4	IRQ2SCA	0	R/W	IRQ2 Sense Control A 00: Interrupt request generated at $\overline{\text{IRQ2}}$ input low level 01: Interrupt request generated at falling edge of $\overline{\text{IRQ2}}$ input 10: Interrupt request generated at rising edge of $\overline{\text{IRQ2}}$ input 11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ2}}$ input

7.7 DRAM Interface

In this LSI, external space areas 2 to 5 can be designated as DRAM space, and DRAM interfacing performed. The DRAM interface allows DRAM to be directly connected to this LSI. A DRAM space of 2, 4, or 8 Mbytes can be set by means of bits RMTS2 to RMTS0 in DRAMCR. Burst operation is also possible, using fast page mode.

Note: The DRAM interface is not supported by the 5-V version.

7.7.1 Setting DRAM Space

Areas 2 to 5 are designated as DRAM space by setting bits RMTS2 to RMTS0 in DRAMCR. The relation between the settings of bits RMTS2 to RMTS0 and DRAM space is shown in table 7.5. Possible DRAM space settings are: one area (area 2), two areas (areas 2 and 3), four areas (areas 2 to 5), and continuous area (areas 2 to 5).

Table 7.5 Relation between Settings of Bits RMTS2 to RMTS0 and DRAM Space

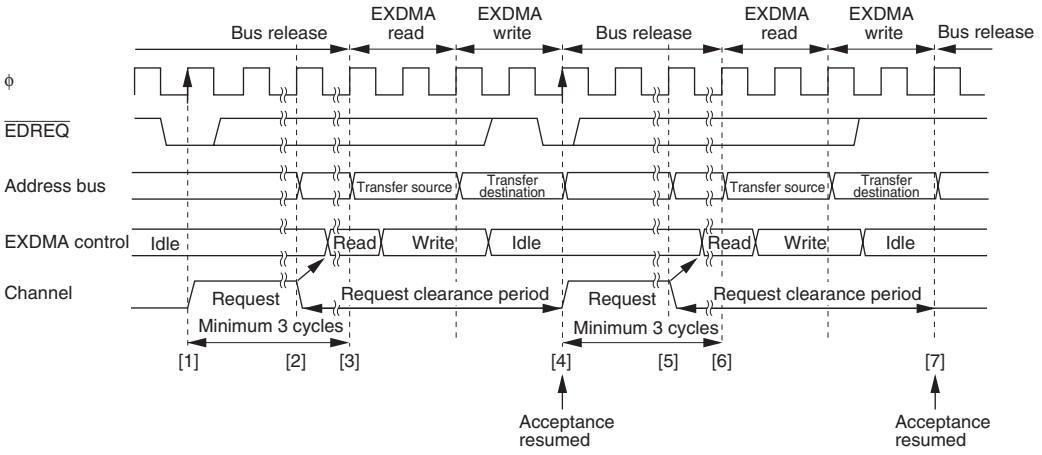
RMTS2	RMTS1	RMTS0	Area 5	Area 4	Area 3	Area 2
0	0	1	Normal space	Normal space	Normal space	DRAM space
	1	0	Normal space	Normal space	DRAM space	DRAM space
		1	DRAM space	DRAM space	DRAM space	DRAM space
1	0	0	Continuous synchronous DRAM space*			
		1	Mode register settings of synchronous DRAM*			
	1	0	Reserved (setting prohibited)			
		1	Continuous DRAM space	Continuous DRAM space	Continuous DRAM space	Continuous DRAM space

Note: * Reserved (setting prohibited) in the H8S/2427 Group and H8S/2425 Group.

With continuous DRAM space, $\overline{RAS2}$ is valid. The bus specifications (bus width, number of wait states, etc.) for continuous DRAM space conform to the settings for area 2.

(4) $\overline{\text{EDREQ}}$ Pin Falling Edge Activation Timing

Figure 9.18 shows an example of normal mode transfer activated by the $\overline{\text{EDREQ}}$ pin falling edge.



[1] Acceptance after transfer enabling; $\overline{\text{EDREQ}}$ pin low level is sampled at rise of ϕ, and request is held.
[2], [5] Request is cleared at end of next bus cycle, and activation is started in EXDMAC.
[3], [6] EXDMA cycle start; $\overline{\text{EDREQ}}$ pin high level sampling is started at rise of ϕ.
[4], [7] When $\overline{\text{EDREQ}}$ pin high level has been sampled, acceptance is resumed after completion of write cycle. (As in [1], $\overline{\text{EDREQ}}$ pin low level is sampled at rise of ϕ, and request is held.)

Figure 9.18 Example of Normal Mode Transfer Activated by $\overline{\text{EDREQ}}$ Pin Falling Edge

$\overline{\text{EDREQ}}$ pin sampling is performed in each cycle starting at the next rise of ϕ after the end of the EDMDR write cycle for setting the transfer-enabled state.

When a low level is sampled at the $\overline{\text{EDREQ}}$ pin while acceptance via the $\overline{\text{EDREQ}}$ pin is possible, the request is held within the EXDMAC. Then when activation is initiated within the EXDMAC, the request is cleared, and $\overline{\text{EDREQ}}$ pin high level sampling for edge sensing is started. If $\overline{\text{EDREQ}}$ pin high level sampling is completed by the end of the EXDMA write cycle, acceptance resumes after the end of the write cycle, and $\overline{\text{EDREQ}}$ pin low level sampling is performed again; this sequence of operations is repeated until the end of the transfer.

Figure 9.19 shows an example of block transfer mode transfer activated by the $\overline{\text{EDREQ}}$ pin falling edge.

10.3 Activation Sources

The DTC operates when activated by an interrupt or by a write to DTVECR or DTCCR by software. An interrupt request can be directed to the CPU or DTC, as designated by the corresponding DTCER bit. At the end of a data transfer (or the last consecutive transfer in the case of chain transfer), the activation source or corresponding DTCER bit is cleared. The activation source flag, in the case of RXI0, for example, is the RDRF flag of SCI_0.

When an interrupt has been designated a DTC activation source, existing CPU mask level and interrupt controller priorities have no effect. If there is more than one activation source at the same time, the DTC operates in accordance with the default priorities.

Table 10.1 shows a relationship between activation sources and DTCER clear conditions. Figure 10.2 shows a block diagram of activation source control. For details see section 6, Interrupt Controller.

Table 10.1 Relationship between Activation Sources and DTCER Clearing

Activation Source	DISEL = 0 and Specified Number of Transfers Has Not Ended	DISEL = 1 or Specified Number of Transfers Has Ended
Activation by software	SWDTIF bit remains cleared to 0	• SWDTIF bit is set to 1 • Interrupt request to CPU
Activation by an interrupt	• Corresponding DTCER bit remains set to 1. • Activation source flag is cleared to 0.	• Corresponding DTCER bit is cleared to 0. • Activation source flag remains set to 1. • Interrupt that became the activation source is requested to the CPU.

Port	Description	Mode 1	Mode 2	Mode 4	Modes 3, 5, 7 EXPE = 1	Modes 3, 5, 7 EXPE = 0	Schmitt-triggered input Pin*4	Input Pull-up MOS Capability	Open Drain Output Capability	5-V Tolerance *2
Port F	General I/O port also functioning as interrupt inputs, bus control signal I/Os, SSU I/Os, and A/D converter inputs	PF7/φ				PF7/φ	—	—	—	—
		PF6/$\overline{AS}$/$\overline{AH}$				PF6			All output pin functions other than $\overline{AS}$ and $\overline{AH}$	
		$\overline{RD}$				PF5			All output pin functions other than $\overline{RD}$	
		$\overline{HWR}$				PF4			All output pin functions other than $\overline{HWR}$	
		PF3/$\overline{LWR}$/SSO0-C				PF3/SSO0-C			All output pin functions other than $\overline{LWR}$	
		PF2/$\overline{LCAS}$*2/DQML*1/$\overline{IRQ15\text{-}A}$/SSI0-C				PF2/ $\overline{IRQ15\text{-}A}$/ SSI0-C	$\overline{IRQ15\text{-}A}$		All output pin functions other than $\overline{LCAS}$ and DQML*1	
		PF1/$\overline{UCAS}$*2/DQMU*1/$\overline{IRQ14\text{-}A}$/SSCK0-C				PF1/ $\overline{IRQ14\text{-}A}$/ SSCK0-C	$\overline{IRQ14\text{-}A}$		All output pin functions other than $\overline{UCAS}$ and DQMU*1	
		PF0/$\overline{WAIT\text{-}A}$/$\overline{ADTRG0\text{-}B}$/$\overline{SCS0\text{-}C}$				PF0/ $\overline{ADTRG0\text{-}B}$/ $\overline{SCS0\text{-}C}$	—		All output pin functions	

- When TGR is an input capture register

  When input capture occurs, the value in TCNT is transferred to TGR and the value previously held in the timer general register is transferred to the buffer register.

  This operation is illustrated in figure 12.14.

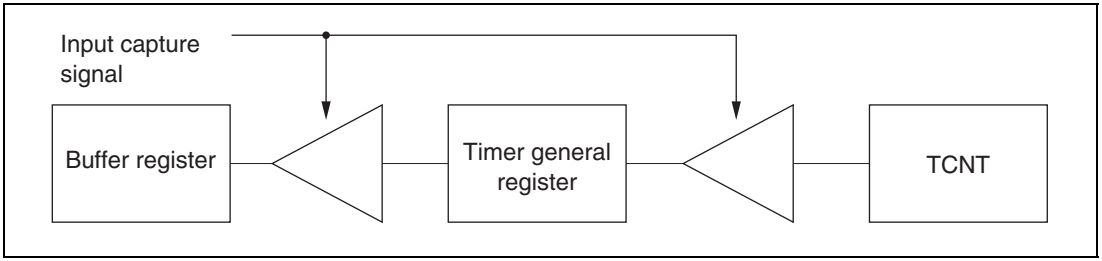


Figure 12.14 Input Capture Buffer Operation

(1) Example of Buffer Operation Setting Procedure

Figure 12.15 shows an example of the buffer operation setting procedure.

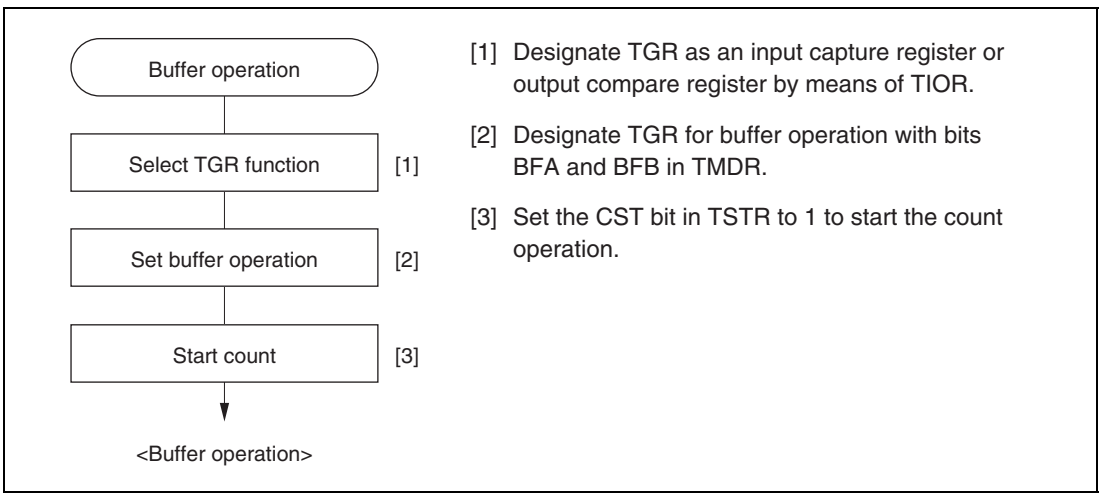


Figure 12.15 Example of Buffer Operation Setting Procedure

12.4.4 Cascaded Operation

In cascaded operation, two 16-bit counters for different channels are used together as a 32-bit counter.

This function works by counting the channel 1 (channel 4, channel 7, or channel 10) counter clock at overflow/underflow of TCNT_2 (TCNT_5, TCNT_8, or TCNT_11) as set in bits TPSC2 to TPSC0 in TCR.

Underflow occurs only when the lower 16-bit TCNT is in phase-counting mode.

Table 12.30 shows the register combinations used in cascaded operation.

Note: When phase counting mode is set for channel 1, 4, 7, or 10, the counter clock setting is invalid and the counter operates independently in phase counting mode.

Table 12.30 Cascaded Combinations

Combination	Upper 16 Bits	Lower 16 Bits
Channels 1 and 2	TCNT_1	TCNT_2
Channels 4 and 5	TCNT_4	TCNT_5
Channels 7 and 8	TCNT_7	TCNT_8
Channels 10 and 11	TCNT_10	TCNT_11

(1) Example of Cascaded Operation Setting Procedure

Figure 12.18 shows an example of the setting procedure for cascaded operation.

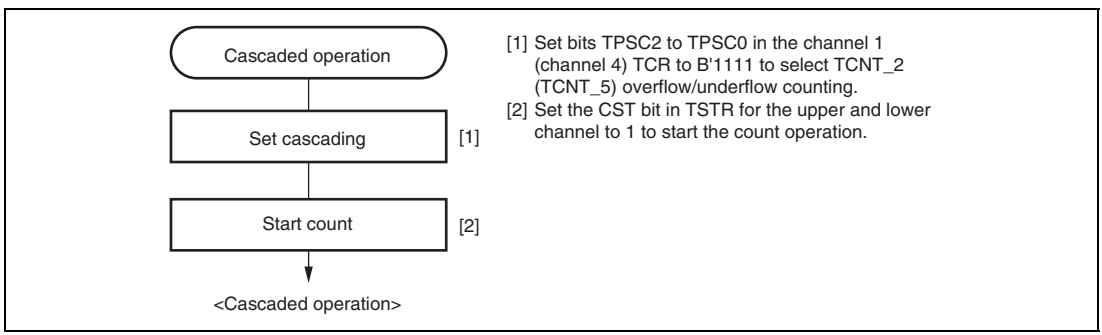


Figure 12.18 Cascaded Operation Setting Procedure

(5) Buffer Operation Timing

Figures 12.37 and 12.38 show the timings in buffer operation.

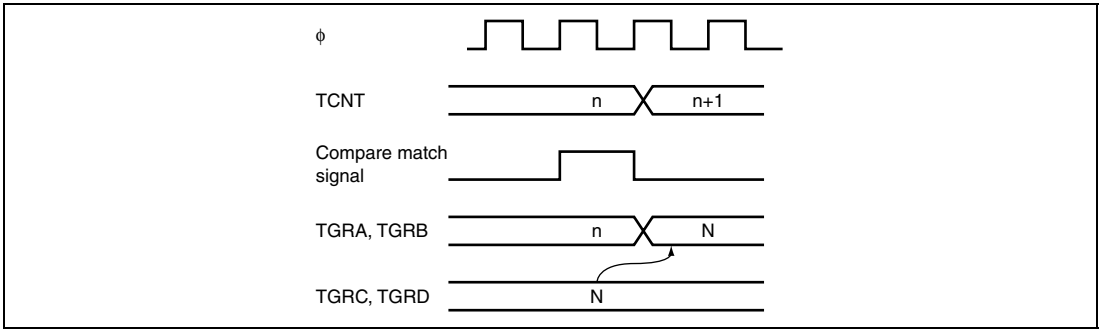


Figure 12.37 Buffer Operation Timing (Compare Match)

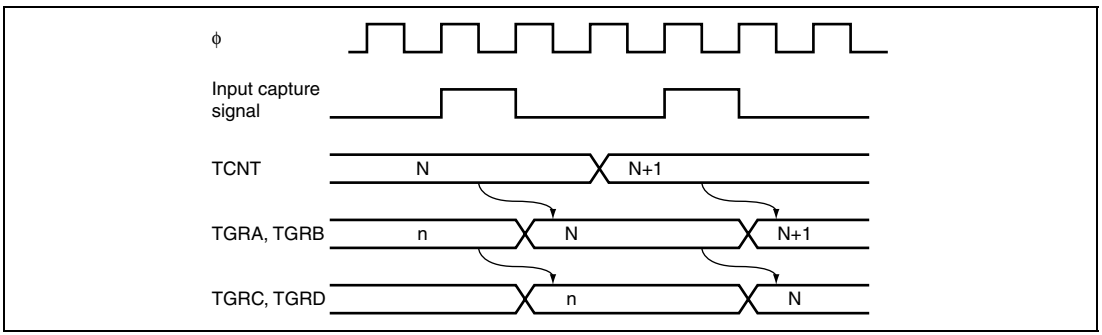


Figure 12.38 Buffer Operation Timing (Input Capture)

14.5 Operation with Cascaded Connection

If bits CKS2 to CKS0 in either TCR_0 or TCR_1 are set to B'100, the 8-bit timers of the two channels are cascaded. With this configuration, a single 16-bit timer could be used (16-bit counter mode) or compare matches of the 8-bit channel 0 could be counted by the timer of channel 1 (compare match count mode). In this case, the timer operates as below.

14.5.1 16-Bit Counter Mode

When bits CKS2 to CKS0 in TCR_0 are set to B'100, the timer functions as a single 16-bit timer with channel 0 occupying the upper 8 bits and channel 1 occupying the lower 8 bits.

[1] Setting of compare match flags

- The CMF flag in TCSR_0 is set to 1 when a 16-bit compare match event occurs.
- The CMF flag in TCSR_1 is set to 1 when a lower 8-bit compare match event occurs.

[2] Counter clear specification

- If the CCLR1 and CCLR0 bits in TCR_0 have been set for counter clear at compare match, the 16-bit counters (TCNT_0 and TCNT_1 together) are cleared when a 16-bit compare match event occurs. The 16-bit counters (TCNT0 and TCNT1 together) are cleared even if counter clear by the TMRI0 pin has also been set.
- The settings of the CCLR1 and CCLR0 bits in TCR_1 are ignored. The lower 8 bits cannot be cleared independently.

[3] Pin output

- Control of output from the TMO0 pin by bits OS3 to OS0 in TCSR_0 is in accordance with the 16-bit compare match conditions.
- Control of output from the TMO1 pin by bits OS3 to OS0 in TCSR_1 is in accordance with the lower 8-bit compare match conditions.

14.5.2 Compare Match Count Mode

When bits CKS2 to CKS0 in TCR_1 are B'100, TCNT_1 counts compare match A's for channel 0. Channels 0 and 1 are controlled independently. Conditions such as setting of the CMF flag, generation of interrupts, output from the TMO pin, and counter clear are in accordance with the settings for each channel.

Bit	Bit Name	Initial Value	R/W	Description
2	ACS2	0	R/W*	Asynchronous clock source selection (valid when CKE1 = 1 in asynchronous mode)
1	ACS1	0	R/W*	
0	ACS0	0	R/W*	Selects the clock source for the average transfer rate. The basic clock can be automatically set by selecting the average transfer rate in spite of the value of ABCS. 000: External clock input 001: Selects 115.152 kbps which is the average transfer rate dedicated for ϕ= 10.667 MHz. (Operates on a basic clock with a frequency of 16 times the transfer rate.) 010: Selects 460.606 kbps which is the average transfer rate dedicated for ϕ= 10.667 MHz. (Operates on a basic clock with a frequency of 8 times the transfer rate.) 011: Selects 720 kbps which is the average transfer rate dedicated for ϕ = 32 MHz. (Operates on a basic clock with a frequency of 16 times the transfer rate.) 100: Reserved 101: Selects 115.196 kbps which is the average transfer rate dedicated for ϕ = 16 MHz (Operates on a basic clock with a frequency of 16 times the transfer rate.) 110: Selects 460.784 kbps which is the average transfer rate dedicated for ϕ = 16 MHz (Operates on a basic clock with a frequency of 16 times the transfer rate.) 111: Selects 720 kbps which is the average transfer rate dedicated for ϕ = 16 MHz (Operates on a basic clock with a frequency of 8 times the transfer rate.) Note that the average transfer rate does not correspond to the frequency other than 10.667, 16, or 32 MHz.

Note: * Can be written to only when TE = RE = 0.

16.10.7 Operation in Case of Mode Transition

(1) Transmission

Operation should be stopped (by clearing TE, TIE, and TEIE to 0) before setting the module stop state or making a transition to software standby mode. TSR, TDR, and SSR are reset. The output pin states in the module stop state or software standby mode depend on the port settings, and become high-level output after the relevant mode is cleared. If a transition is made during transmission, the data being transmitted will be undefined.

When transmitting without changing the transmit mode after the relevant mode is cleared, transmission can be started by setting TE to 1 again, and performing the following sequence: SSR read → TDR write → TDRE clearance. To transmit with a different transmit mode after clearing the relevant mode, the procedure must be started again from initialization.

Figure 16.36 shows a sample flowchart for mode transition during transmission. Port pin states during mode transition are shown in figures 16.37 and 16.38.

Operation should also be stopped (by clearing TE, TIE, and TEIE to 0) before making a transition from transmission by DTC transfer to module stop state setting or software standby mode transition. To perform transmission with the DTC after the relevant mode is cleared, setting TE and TIE to 1 will set the TXI flag and start DTC transmission.

(2) Reception

Receive operation should be stopped (by clearing RE to 0) before setting the module stop state or making a transition to software standby mode. RSR, RDR, and SSR are reset. If a transition is made during reception, the data being received will be invalid.

To continue receiving without changing the receive mode after the relevant mode is cleared, set the RE bit to 1 before starting reception. To receive in a different receive mode after clearing the relevant mode, the procedure must be started again from initialization.

Figure 16.39 shows a sample flowchart for mode transition during reception.

(4) Data Transmission/Reception

Figure 20.17 shows a flowchart example of simultaneous transmission/reception. The data transmission/reception is performed combining the data transmission and data reception as mentioned above. The data transmission/reception is started by writing transmit data to SSTDR with TE = RE = 1.

Before switching transmission mode (TE = 1) or reception mode (RE = 1) to transmission/reception mode (TE = RE = 1), clear the TE and RE bits to 0. When starting the transfer, confirm that the TEND, RDRF, and ORER bits are cleared to 0 before setting the TE or RE bits to 1.

23.13 Switching between User ROM and User Boot ROM

It is possible to switch between user ROM and user boot ROM. However, the following procedure is required because the start addresses of these MATs are allocated to the same address 0. (Switching to the user boot ROM disables programming and erasing. Programming of the user boot ROM should take place in boot mode or programmer mode.)

1. Memory MAT switching by the FMMS bit in FLMMATS should always be executed from the on-chip RAM.
2. When accessing the memory MAT immediately after switching the memory MATs by modifying the FMMS bit in FLMMATS from the on-chip RAM, similarly execute four NOP instructions in the on-chip RAM (this prevents access to the flash memory during memory MAT switching).
3. If an interrupt request has occurred during memory MAT switching, there is no guarantee of which memory MAT is accessed. Always mask the maskable interrupts before switching memory MATs. In addition, configure the system so that NMI interrupts do not occur during memory MAT switching.
4. After the memory MATs have been switched, take care because the interrupt vector tables will also have been switched.
5. The size of the user ROM is different from that of the user boot ROM. Addresses which exceed the size of the 16-Kbyte user boot ROM area should not be accessed. If a user boot ROM area of a size greater than 16 Kbytes is accessed, data is read as an undefined value.

27.3 Electrical Characteristics for H8S/2427 Group and H8S/2427R Group (3-V Version)

27.3.1 Absolute Maximum Ratings

Table 27.26 lists the absolute maximum ratings.

Table 27.26 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC} $PLLV_{CC}$	–0.3 to +4.3	V
Input voltage (except ports 4, 9, and 2, P32 to P35, P50 and P51, and PJ0 to PJ2)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (ports 2, P50 and P51, P32 to P35, and PJ0 to PJ2)	V_{in}	–0.3 to +6.5	V
Input voltage (ports 4 and 9)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference power supply voltage	V_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +4.3	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75*	°C
		Wide-range specifications: –40 to +85*	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note: * Ranges of operating temperature when flash memory is programmed/erased:
Regular specifications: Ta = 0 to +75°C
Wide-range specifications: Ta = 0 to +85°C

(5) Timing of On-Chip Peripheral Modules

Table 27.61 Timing of On-Chip Peripheral Modules

Conditions: V_{CC} = 4.5 V to 5.5 V, AV_{CC} = 4.5 V to 5.5 V, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 8 MHz to 33 MHz

Item			Symbol	Min.	Max.	Unit	Test Conditions
I/O ports	Output data delay time		t_{PWD}	—	40	ns	Figure 27.77
	Input data setup time		t_{PRS}	25	—	ns	
	Input data hold time		t_{PRH}	25	—	ns	
PPG	Pulse output delay time		t_{POD}	—	40	ns	Figure 27.78
TPU	Timer output delay time		t_{TOCD}	—	40	ns	Figure 27.79
	Timer input setup time		t_{TICS}	25	—	ns	
	Timer clock input setup time		t_{TCKS}	25	—	ns	Figure 27.80
	Timer clock pulse width	Single-edge specification	t_{TCKWH}	1.5	—	t_{cyc}	
		Both-edge specification	t_{TCKWL}	2.5	—	t_{cyc}	
8-bit timer	Timer output delay time		t_{TMOD}	—	40	ns	Figure 27.81
	Timer reset input setup time		t_{TMRS}	25	—	ns	Figure 27.83
	Timer clock input setup time		t_{TMCS}	25	—	ns	Figure 27.82
	Timer clock pulse width	Single-edge specification	t_{TMCWH}	1.5	—	t_{cyc}	
		Both-edge specification	t_{TMCWL}	2.5	—	t_{cyc}	
WDT	Overflow output delay time		t_{WOVD}	—	40	ns	Figure 27.84
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{cyc}	Figure 27.85
		Synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rising time		t_{SCKr}	—	1.5	t_{cyc}	
	Input clock falling time		t_{SCKf}	—	1.5		
	Transmit data delay time		t_{TXD}	—	40	ns	Figure 27.86
	Receive data setup time (synchronous)		t_{RXS}	40	—	ns	
	Receive data hold time (synchronous)		t_{RXH}	40	—	ns	

27.6.6 Flash Memory Characteristics

Table 27.64 Flash Memory Characteristics

Conditions: V_{CC} = 4.5 V to 5.5 V, AV_{CC} = 4.5 V to 5.5 V, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 8 MHz to 33 MHz

		Standard Value			
Item	**Applicable Area**	**Min.**	**Typ.**	**Max.**	**Unit**
Programming and erase count*1	User ROM	1,000*2	—	—	Times
	Data flash area	10,000*2	—	—	
Programming time (per 4 bytes)	User ROM	—	150	4000	µs
	Data flash area	—	300	4000	
Erase time (per 1 block)	User ROM	—	300	3000	ms
	Data flash area	—	300	3000	
Programming and erase voltage	User ROM	4.5	—	5.5	V
	Data flash area				
Read voltage	User ROM	4.5	—	5.5	V
	Data flash area				
Access state	User ROM	1	—	—	State
	Data flash area	2	—	—	

Notes: 1. When programming is to be performed multiple times on a system, reduce the effective number of programming operations by shifting the writing addresses in sequence and so on until the remaining blank area is as small as possible and only then erasing the entire block once. For example, if sets of 16 bytes are being programmed, erasing the block once after programming the maximum number of sets (256) minimizes the effective number of programming operations.

We recommend keeping information on the number of times erasure is performed for each block, and setting up the limit on the number of times.

2. If an erase error occurs during erasure, execute the clear status command and then the erase command at least 3 times until the erase error does not occur.

*1. Determination of the number of times for programming/erasure operations.

Number of times programming/erasure is performed in each block.

When the number of times for programming/erasure operations is n (n = 100), data can be erased n times in each block.

For example, if programming of 4 bytes is done 1024 times, each at a different address in a 4-kbyte per block, and the block is then erased, this counts as programming/erasure one time.

However, programming of any location in a block multiple times is not possible (overwriting is prohibited).

*2. This is the number of times for which all electrical characteristics are guaranteed.

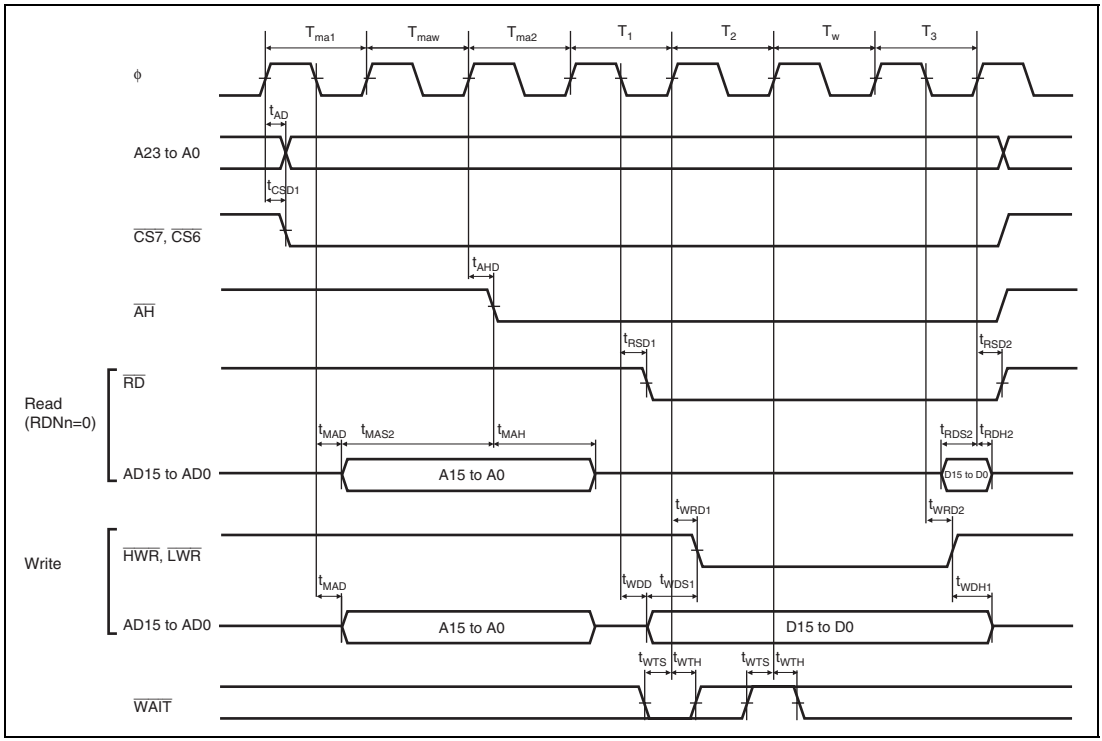


Figure 27.71 Multiplexed Bus Timing: Data Three-State Access, One Wait (With address wait: when ADDEX = 1)

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus Release State	Program Execution State Sleep Mode
Port B	1, 2	L	T	[OPE = 0] T [OPE = 1] keep	T	[Address output] A15 to A8
	4	T	T	[Address output, OPE = 0] T [Address output, OPE = 1] Keep [Other than the above] keep	[Address output] T [Other than the above] keep	[Address output] A15 to A8 [Other than the above] I/O port
	3, 5, 7	T	T	[Address output, OPE = 0] T [Address output, OPE = 1] Keep [Other than the above] keep	[Address output] T [Other than the above] keep	[Address output] A15 to A8 [Other than the above] I/O port

Item	Page	Revision (See Manual for Details)
Table 16.2 Relationships between N Setting in BRR and Bit Rate B	926	Amended and added **Bit Rate** $N = \frac{\phi \times 10^6}{64 \times 2^{2n-1} \times B} - 1$ $N = \frac{\phi \times 10^6}{32 \times 2^{2n-1} \times B} - 1$ $N = \frac{\phi \times 10^6}{8 \times 2^{2n-1} \times B} - 1$ $N = \frac{\phi \times 10^6}{S \times 2^{2n+1} \times B} - 1$
17.7 Usage Notes	1032, 1033	Added 5. Restriction on Setting Transfer Rate in Use of Multi-Master 6. Restriction on Use of Bit Manipulation Instructions to Set MST and TRS in Use of Multi-Master 7. Note on Master Receive Mode 8. Notes on Changing from Master Transmit Mode to Master Receive Mode
18.3.4 A/D Control Register (ADCR_0) Unit 0	1048, 1049	Added **Bit** / **Bit Name** / **Description** 7 TRGS1 6 TRGS0 0 EXTRGS 010: Enables A/D conversion start by external trigger from TPU (units 0 and 1)* Note: * If this bit is set the same as the TRGS_1, TRGS0, and EXTRGS bits in ADCR_1, the A/D converter units 0 and 1 start A/D conversion by conversion start trigger from TPU (units 0 and 1).