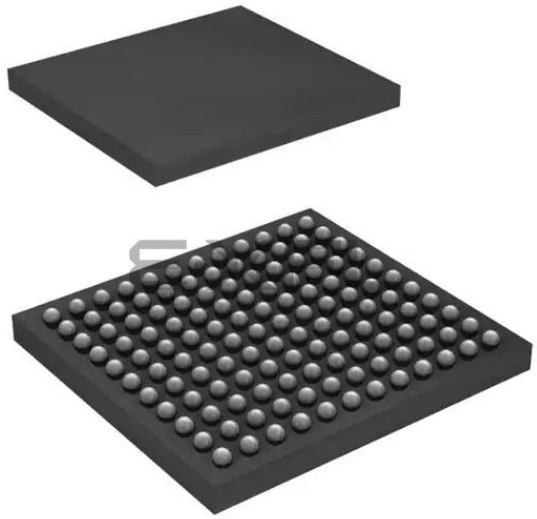
# Lattice Semiconductor Corporation - ICE40HX1K-CB132 Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 160 |
| Number of Logic Elements/Cells | 1280 |
| Total RAM Bits | 65536 |
| Number of I/O | 95 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 132-LFBGA, CSPBGA |
| Supplier Device Package | 132-CSBGA (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40hx1k-cb132 |

## Routing

There are many resources provided in the iCE40 devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

## Clock/Control Distribution Network

Each iCE40 device has eight global inputs, two pins on each side of the device. Note that not all GBINs are available in all packages.

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as GBIN[7:0] and the global buffers are identified as-GBUF[7:0]. These eight inputs may be used as general purpose I/O if they are not used to drive the clock nets. Global buffer GBUF7 in I/O Bank 3 also provides an optional direct LVDS25 or subLVDS differential clock input.

Table 2-2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input.

***Table 2-2. Global Buffer (GBUF) Connections to Programmable Logic Blocks***

| Global Buffer | LUT Inputs | Clock | Reset | Clock Enable |
|---|---|---|---|---|
| GBUF0 | Yes, any 4 of 8 GBUF Inputs | Yes | Yes | |
| GBUF1 | | Yes | | Yes |
| GBUF2 | | Yes | Yes | |
| GBUF3 | | Yes | | Yes |
| GBUF4 | | Yes | Yes | |
| GBUF5 | | Yes | | Yes |
| GBUF6 | | Yes | Yes | |
| GBUF7 | | Yes | | Yes |

The maximum frequency for the global buffers are shown in the iCE40 External Switching Characteristics tables later in this document.

### Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

*Table 2-3. PLL Signal Descriptions*

| Signal Name | Direction | Description |
|---|---|---|
| REFERENCECLK | Input | Input reference clock |
| BYPASS | Input | When FEEDBACK_PATH is set to SIMPLE, the BYPASS control selects which clock signal connects to the PLLOUT output.<br>0 = PLL generated signal<br>1 = REFERENCECLK |
| EXTFEEDBACK | Input | External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL. |
| DYNAMICDELAY[3:0] | Input | Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC. |
| LATCHINPUTVALUE | Input | When enabled, forces the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable. |
| PLLOUTGLOBAL | Output | Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5. |
| PLLOUTCORE | Output | Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port. |
| LOCK | Output | When High, indicates that the PLL output is phase aligned or locked to the input reference clock. |
| RESET | Input | Active low reset. |

## sysMEM Embedded Block RAM Memory

Larger iCE40 device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

### sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

*Table 2-4. sysMEM Block Configurations[1]*

| Block RAM Configuration | Block RAM Configuration and Size | WADDR Port Size (Bits) | WDATA Port Size (Bits) | RADDR Port Size (Bits) | RDATA Port Size (Bits) | MASK Port Size (Bits) |
|---|---|---|---|---|---|---|
| SB_RAM256x16<br>SB_RAM256x16NR<br>SB_RAM256x16NW<br>SB_RAM256x16NRNW | 256x16 (4K) | 8 [7:0] | 16 [15:0] | 8 [7:0] | 16 [15:0] | 16 [15:0] |
| SB_RAM512x8<br>SB_RAM512x8NR<br>SB_RAM512x8NW<br>SB_RAM512x8NRNW | 512x8 (4K) | 9 [8:0] | 8 [7:0] | 9 [8:0] | 8 [7:0] | No Mask Port |
| SB_RAM1024x4<br>SB_RAM1024x4NR<br>SB_RAM1024x4NW<br>SB_RAM1024x4NRNW | 1024x4 (4K) | 10 [9:0] | 4 [3:0] | 10 [9:0] | 4 [3:0] | No Mask Port |
| SB_RAM2048x2<br>SB_RAM2048x2NR<br>SB_RAM2048x2NW<br>SB_RAM2048x2NRNW | 2048x2 (4K) | 11 [10:0] | 2 [1:0] | 11 [10:0] | 2 [1:0] | No Mask Port |

1. For iCE40 EBR primitives with a negative-edged Read or Write clock, the base primitive name is appended with a 'N' and a 'R' or 'W' depending on the clock that is affected.

### RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Note the sysMEM Embedded Block RAM Memory address 0 cannot be initialized.

### Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

### RAM4k Block

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

***Figure 2-4. sysMEM Memory Primitives***

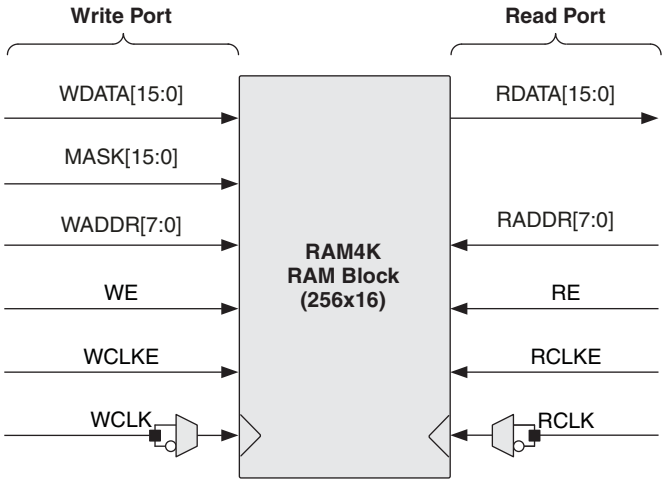



***Table 2-5. EBR Signal Descriptions***

| Signal Name | Direction | Description |
|---|---|---|
| WDATA[15:0] | Input | Write Data input. |
| MASK[15:0] | Input | Masks write operations for individual data bit-lines.<br>0 = write bit; 1 = don't write bit |
| WADDR[7:0] | Input | Write Address input. Selects one of 256 possible RAM locations. |
| WE | Input | Write Enable input. |
| WCLKE | Input | Write Clock Enable input. |
| WCLK | Input | Write Clock input. Default rising-edge, but with falling-edge option. |
| RDATA[15:0] | Output | Read Data output. |
| RADDR[7:0] | Input | Read Address input. Selects one of 256 possible RAM locations. |
| RE | Input | Read Enable input. |
| RCLKE | Input | Read Clock Enable input. |
| RCLK | Input | Read Clock input. Default rising-edge, but with falling-edge option. |

For further information on the sysMEM EBR block, please refer to TN1250, Memory Usage Guide for iCE40 Devices.

## sysIO

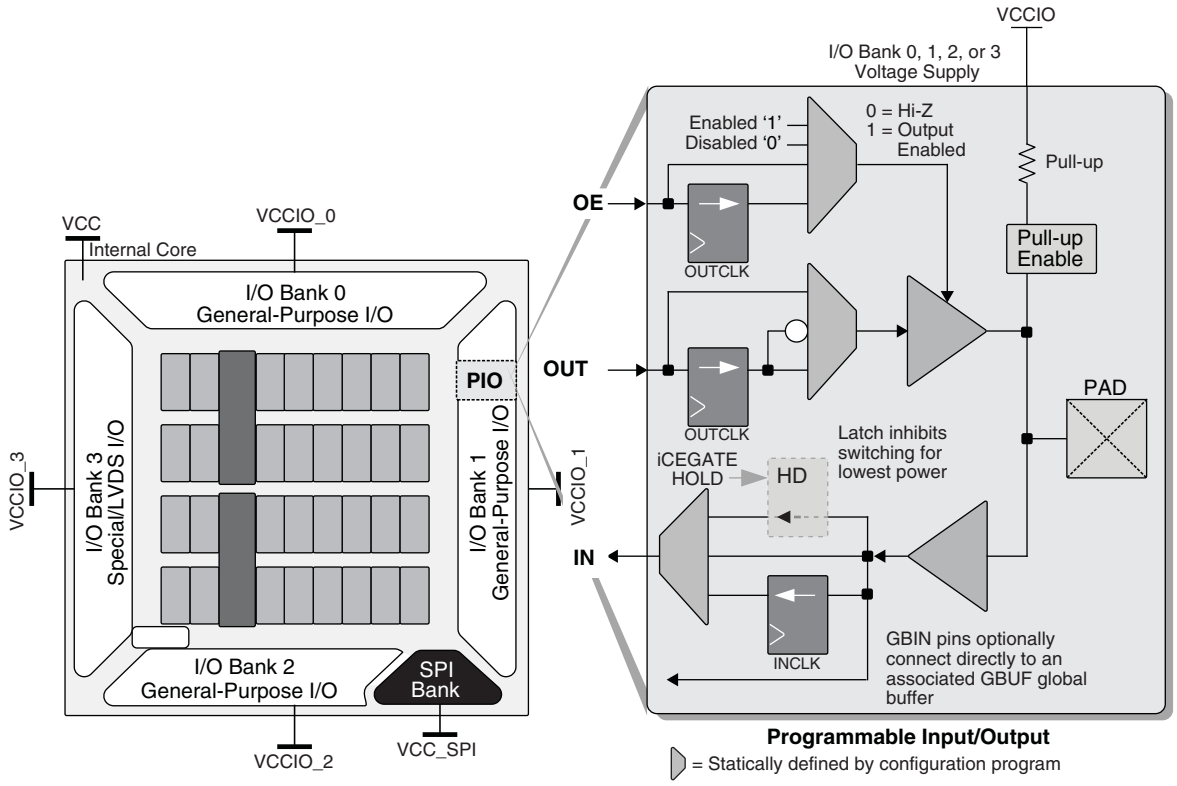
### Buffer Banks

iCE40 devices have up to four I/O banks with independent $V_{CCIO}$ rails with an additional configuration bank $V_{CC\_SPI}$ for the SPI I/Os.

### Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. The PIOs are placed on all four sides of the device.

***Figure 2-5. I/O Bank and Programmable I/O Cell***




The PIO contains three blocks: an input register block, output register block iCEgate™ and tri-state register block. To save power, the optional iCEgate™ latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

### Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock signal, creating two data streams.

### Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers. In Generic DDR mode, two registers are used to capture the data on the positive and negative edge of the system clock and then muxed creating one data stream.

Figure 2-6 shows the input/output register block for the PIOs.

fers. Bank 3 additionally supports differential LVDS25 input buffers. Each sysIO bank has its own dedicated power supply.

**Typical I/O Behavior During Power-up**

The internal power-on-reset (POR) signal is deactivated when $V_{CC}$, $V_{CCIO\_2}$, $V_{PP\_2V5}$, and $V_{CC\_SPI}$ have reached the level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all $V_{CCIO}$ banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to $V_{CCIO}$. The I/O pins will maintain the pre-configuration state until $V_{CC}$ and $V_{CCIO}$ (for I/O banks containing configuration I/Os) have reached levels, at which time the I/Os will take on the software user-configured settings only after a proper download/configuration. Unused IOs are automatically blocked and the pullup termination is disabled.

**Supported Standards**

The iCE40 sysIO buffer supports both single-ended and differential input standards. The single-ended standard supported is LVCMOS. The buffer supports the LVCMOS 1.8, 2.5, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none). The High Current output buffer have individually configurable options for drive strength.

Table 2-7 and Table 2-8 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 devices.

***Table 2-7. Supported Input Standards***

| Input Standard | $V_{CCIO}$ (Typical) | | |
|---|---|---|---|
| | 3.3 V | 2.5 V | 1.8 V |
| **Single-Ended Interfaces** | | | |
| LVCMOS33 | Yes | | |
| LVCMOS25 | | Yes | |
| LVCMOS18 | | | Yes |
| **Differential Interfaces** | | | |
| LVDS25[1] | | Yes | |
| subLVDS[1] | | | Yes |

1. Bank 3 only.

***Table 2-8. Supported Output Standards***

| Output Standard | $V_{CCIO}$ (Typical) |
|---|---|
| **Single-Ended Interfaces** | |
| LVCMOS33 | 3.3 |
| LVCMOS25 | 2.5 |
| LVCMOS18 | 1.8 |
| **Differential Interfaces** | |
| LVDS25E[1] | 2.5 |
| subLVDSE[1] | 1.8 |

1. These interfaces can be emulated with external resistors in all devices.

## Non-Volatile Configuration Memory

All iCE40 devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, please refer to TN1248, iCE40 Programming and Configuration Usage Guide.

# iCE40 LP/HX Family Data Sheet DC and Switching Characteristics

October 2015 Data Sheet DS1040

## Absolute Maximum Ratings[1, 2, 3, 4]

| | iCE40 LP/HX |
|---|---|
| Supply Voltage $V_{CC}$ | –0.5 V to 1.42 V |
| Output Supply Voltage $V_{CCIO}$, $V_{CC\_SPI}$ | –0.5 V to 3.60 V |
| NVCM Supply Voltage $V_{PP\_2V5}$ | –0.5 V to 3.60 V |
| PLL Supply Voltage $V_{CCPLL}$ | –0.5 V to 1.30 V |
| I/O Tri-state Voltage Applied | –0.5 V to 3.60 V |
| Dedicated Input Voltage Applied | –0.5 V to 3.60 V |
| Storage Temperature (Ambient) | –65 °C to 150 °C |
| Junction Temperature ($T_J$) | –55 °C to 125 °C |

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. IOs can support a 200 mV Overshoot above the Recommend Operating Conditions $V_{CCIO}$ (Max) and -200mV Undershoot below $V_{IL}$ (Min). Overshoot and Undershoot is permitted for 25% duty cycle but must not exceed 1.6 ns.

## Recommended Operating Conditions[1]

| Symbol | Parameter | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{CC}$[1] | Core Supply Voltage | | 1.14 | 1.26 | V |
| $V_{PP\_2V5}$ | $V_{PP\_2V5}$ NVCM Programming and Operating Supply Voltage | Slave SPI Configuration | 1.71 | 3.46 | V |
| | | Master SPI Configuration | 2.30 | 3.46 | V |
| | | Configure from NVCM | 2.30 | 3.46 | V |
| | | NVCM Programming | 2.30 | 3.00 | V |
| $V_{PP\_FAST}$[4] | Optional fast NVCM programming supply. Leave unconnected. | | N/A | N/A | V |
| $V_{CCPLL}$[5, 6] | PLL Supply Voltage | | 1.14 | 1.26 | V |
| $V_{CCIO}$[1, 2, 3] | I/O Driver Supply Voltage | $V_{CCIO0-3}$ | 1.71 | 3.46 | V |
| | | $V_{CC\_SPI}$ | 1.71 | 3.46 | V |
| $t_{JIND}$ | Junction Temperature Industrial Operation | | –40 | 100 | °C |
| $t_{PROG}$ | Junction Temperature NVCM Programming | | 10 | 30 | °C |

1. Like power supplies must be tied together. For example, if $V_{CCIO}$ and $V_{CC\_SPI}$ are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. $V_{CCIO}$ pins of unused I/O banks should be connected to the $V_{CC}$ power supply on boards.
4. $V_{PP\_FAST}$, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the $V_{PP\_FAST}$ ball connected to $V_{CCIO\_0}$ ball externally.
5. No PLL available on the iCE40LP384 and iCE40LP640 device.
6. $V_{CCPLL}$ is tied to $V_{CC}$ internally in packages without PLLs pins.

## Power Supply Ramp Rates[1, 2]

| Symbol | Parameter | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $t_{RAMP}$ | Power supply ramp rates for all power supplies. | All configuration modes. No power supply sequencing. | 0.40 | 10 | V/ms |
| | | Configuring from Slave SPI. No power supply sequencing, | 0.01 | 10 | V/ms |
| | | Configuring from NVCM. $V_{CC}$ and $V_{PP\_2V5}$ to be powered 0.25 ms before $V_{CC\_SPI}$. | 0.01 | 10 | V/ms |
| | | Configuring from MSPI. $V_{CC}$ and $V_{PP\_SPI}$ to be powered 0.25 ms before $V_{PP\_2V5}$. | 0.01 | 10 | V/ms |

1. Assumes monotonic ramp rates.
2. iCE40LP384 requires $V_{CC}$ to be greater than 0.7V when $V_{CCIO}$ and $V_{CC\_SPI}$ are above GND.

## Power-On-Reset Voltage Levels[1]

| Symbol | Device | Parameter | | Min. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{PORUP}$ | iCE40LP384 | Power-On-Reset ramp-up trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5) | VCC | 0.67 | 0.99 | V |
| | | | VCCIO_2 | 0.70 | 1.59 | V |
| | | | VCC_SPI | 0.70 | 1.59 | V |
| | | | VPP_2V5 | 0.70 | 1.59 | V |
| | iCE40LP640, iCE40LP/HX1K, iCE40LP/HX4K, iCE40LP/HX8K | Power-On-Reset ramp-up trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5) | VCC | 0.55 | 0.75 | V |
| | | | VCCIO_2 | 0.86 | 1.29 | V |
| | | | VCC_SPI | 0.86 | 1.29 | V |
| | | | VPP_2V5 | 0.86 | 1.33 | V |
| $V_{PORDN}$ | iCE40LP384 | Power-On-Reset ramp-down trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5) | VCC | — | 0.64 | V |
| | | | VCCIO_2 | — | 1.59 | V |
| | | | VCC_SPI | — | 1.59 | V |
| | | | VPP_2V5 | — | 1.59 | V |
| | iCE40LP640, iCE40LP/HX1K, iCE40LP/HX4K, iCE40LP/HX8K | Power-On-Reset ramp-down trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5) | VCC | — | 0.75 | V |
| | | | VCCIO_2 | — | 1.29 | V |
| | | | VCC_SPI | — | 1.29 | V |
| | | | VPP_2V5 | — | 1.33 | V |

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

## ESD Performance

Please refer to the iCE40 Product Family Qualification Summary for complete qualification data, including ESD performance.

# DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$ [1, 3, 4, 5, 6, 7] | Input or I/O Leakage | $0V < V_{IN} < V_{CCIO} + 0.2$ V | — | — | +/–10 | µA |
| $C_1$ [6, 7] | I/O Capacitance[2] | $V_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V<br>$V_{CC}$ = Typ., $V_{IO}$ = 0 to $V_{CCIO}$ + 0.2 V | — | 6 | — | pf |
| $C_2$ [6, 7] | Global Input Buffer Capacitance[2] | $V_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V<br>$V_{CC}$ = Typ., $V_{IO}$ = 0 to $V_{CCIO}$ + 0.2 V | — | 6 | — | pf |
| $V_{HYST}$ | Input Hysteresis | $V_{CCIO}$ = 1.8 V, 2.5 V, 3.3 V | — | 200 | — | mV |
| $I_{PU}$ [6, 7] | Internal PIO Pull-up Current | $V_{CCIO}$ = 1.8 V, 0=<$V_{IN}$<=0.65 $V_{CCIO}$ | –3 | — | –31 | µA |
| | | $V_{CCIO}$ = 2.5 V, 0=<$V_{IN}$<=0.65 $V_{CCIO}$ | –8 | — | –72 | µA |
| | | $V_{CCIO}$ = 3.3 V, 0=<$V_{IN}$<=0.65 $V_{CCIO}$ | –11 | — | –128 | µA |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2. $T_J$ 25°C, f = 1.0 MHz.
3. Please refer to $V_{IL}$ and $V_{IH}$ in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Only applies to IOs in the SPI bank following configuration.
5. Some products are clamped to a diode when $V_{IN}$ is larger than $V_{CCIO}$.
6. High current IOs has three sysIO buffers connected together.
7. The iCE40LP640 and iCE40LP1K SWG16 package has CDONE and a sysIO buffer are connected together.

# Static Supply Current – LP Devices[1, 2, 3, 4]

| Symbol | Parameter | Device | Typ. $V_{CC}$[4] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | iCE40LP384 | 21 | µA |
| | | iCE40LP640 | 100 | µA |
| | | iCE40LP1K | 100 | µA |
| | | iCE40LP4K | 250 | µA |
| | | iCE40LP8K | 250 | µA |
| $I_{CCPLL}$ [5, 6] | PLL Power Supply | All devices | 0.5 | µA |
| $I_{PP\_2V5}$ | NVCM Power Supply | All devices | 1.0 | µA |
| $I_{CCIO}$, $I_{CC\_SPI}$ | Bank Power Supply[4]<br>$V_{CCIO}$ = 2.5 V | All devices | 3.5 | µA |

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at $V_{CCIO}$ or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. $T_J$ = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up.
5. No PLL available on the iCE40LP384 and iCE40LP640 device.
6. $V_{CCPLL}$ is tied to $V_{CC}$ internally in packages without PLLs pins.

## Static Supply Current – HX Devices[1, 2, 3, 4]

| Symbol | Parameter | Device | Typ. $V_{CC}$[4] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | iCE40HX1K | 296 | µA |
| | | iCE40HX4K | 1140 | µA |
| | | iCE40HX8K | 1140 | µA |
| $I_{CCPLL}$[5] | PLL Power Supply | All devices | 0.5 | µA |
| $I_{PP\_2V5}$ | NVCM Power Supply | All devices | 1.0 | µA |
| $I_{CCIO}$, $I_{CC\_SPI}$ | Bank Power Supply[4] $V_{CCIO}$ = 2.5 V | All devices | 3.5 | µA |

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at $V_{CCIO}$ or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. $T_J$ = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up.
5. $V_{CCPLL}$ is tied to $V_{CC}$ internally in packages without PLLs pins.

## Programming NVCM Supply Current – LP Devices[1, 2, 3, 4]

| Symbol | Parameter | Device | Typ. $V_{CC}$[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | iCE40LP384 | 60 | µA |
| | | iCE40LP640 | 120 | µA |
| | | iCE40LP1K | 120 | µA |
| | | iCE40LP4K | 350 | µA |
| | | iCE40LP8K | 350 | µA |
| $I_{CCPLL}$[6, 7] | PLL Power Supply | All devices | 0.5 | µA |
| $I_{PP\_2V5}$ | NVCM Power Supply | All devices | 2.5 | mA |
| $I_{CCIO}$[8], $I_{CC\_SPI}$ | Bank Power Supply[5] | All devices | 3.5 | mA |

1. Assumes all inputs are held at $V_{CCIO}$ or GND and all outputs are tri-stated.
2. Typical user pattern.
3. SPI programming is at 8 MHz.
4. $T_J$ = 25 °C, power supplies at nominal voltage.
5. Per bank. $V_{CCIO}$ = 2.5 V. Does not include pull-up.
6. No PLL available on the iCE40-LP384 and iCE40-LP640 device.
7. $V_{CCPLL}$ is tied to $V_{CC}$ internally in packages without PLLs pins.
8. $V_{PP\_FAST}$, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the $V_{PP\_FAST}$ ball connected to $V_{CCIO\_0}$ ball externally.

## Programming NVCM Supply Current – HX Devices[1, 2, 3, 4]

| Symbol | Parameter | Device | Typ. $V_{CC}$[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | iCE40HX1K | 278 | µA |
| | | iCE40HX4K | 1174 | µA |
| | | iCE40HX8K | 1174 | µA |
| $I_{CCPLL}$[6] | PLL Power Supply | All devices | 0.5 | µA |
| $I_{PP\_2V5}$ | NVCM Power Supply | All devices | 2.5 | mA |
| $I_{CCIO}$[7], $I_{CC\_SPI}$ | Bank Power Supply[5] | All devices | 3.5 | mA |

1. Assumes all inputs are held at $V_{CCIO}$ or GND and all outputs are tri-stated.
2. Typical user pattern.
3. SPI programming is at 8 MHz.
4. $T_J$ = 25 °C, power supplies at nominal voltage.
5. Per bank. $V_{CCIO}$ = 2.5 V. Does not include pull-up.
6. $V_{CCPLL}$ is tied to $V_{CC}$ internally in packages without PLLs pins.
7. $V_{PP\_FAST}$, used only for fast production programming, must be left floating or unconnected in applications.

## Peak Startup Supply Current – LP Devices

| Symbol | Parameter | Device | Max | Units |
|---|---|---|---|---|
| $I_{CCPEAK}$ | Core Power Supply | iCE40LP384 | 7.7 | mA |
| | | iCELP640 | 6.4 | mA |
| | | iCE40LP1K | 6.4 | mA |
| | | iCE40LP4K | 15.7 | mA |
| | | iCE40LP8K | 15.7 | mA |
| $I_{CCPLLPEAK}$[1, 2, 4] | PLL Power Supply | iCE40LP1K | 1.5 | mA |
| | | iCELP640 | 1.5 | mA |
| | | iCE40LP4K | 8.0 | mA |
| | | iCE40LP8K | 8.0 | mA |
| $I_{PP\_2V5PEAK}$ | NVCM Power Supply | iCE40LP384 | 3.0 | mA |
| | | iCELP640 | 7.7 | mA |
| | | iCE40LP1K | 7.7 | mA |
| | | iCE40LP4K | 4.2 | mA |
| | | iCE40LP8K | 4.2 | mA |
| $I_{PP\_FASTPEAK}$[3] | NVCM Programming Supply | iCE40LP384 | 5.7 | mA |
| | | iCELP640 | 8.1 | mA |
| | | iCE40LP1K | 8.1 | mA |
| $I_{CCIOPEAK}$[5], $I_{CC\_SPIPEAK}$ | Bank Power Supply | iCE40LP384 | 8.4 | mA |
| | | iCELP640 | 3.3 | mA |
| | | iCE40LP1K | 3.3 | mA |
| | | iCE40LP4K | 8.2 | mA |
| | | iCE40LP8K | 8.2 | mA |

1. No PLL available on the iCE40LP384 and iCE40LP640 device.
2. $V_{CCPLL}$ is tied to $V_{CC}$ internally in packages without PLLs pins.
3. $V_{PP\_FAST}$, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the $V_{PP\_FAST}$ ball connected to $V_{CCIO\_0}$ ball externally.
4. While no PLL is available in the iCE40-LP640 the $I_{CCPLLPEAK}$ is additive to $I_{CCPEAK}$.
5. iCE40LP384 requires $V_{CC}$ to be greater than 0.7 V when $V_{CCIO}$ and $V_{CC\_SPI}$ are above GND.

## sysIO Differential Electrical Characteristics

The LVDS25E/subLVDSE differential output buffers are available on all banks but the LVDS/subLVDS input buffers are only available on Bank 3 of iCE40 devices.

### LVDS25

**Over Recommended Operating Conditions**

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input Voltage | $V_{CCIO}$[1] = 2.5 | 0 | — | 2.5 | V |
| $V_{THD}$ | Differential Input Threshold | | 250 | 350 | 450 | mV |
| $V_{CM}$ | Input Common Mode Voltage | $V_{CCIO}$[1] = 2.5 | ($V_{CCIO}$/2) - 0.3 | $V_{CCIO}$/2 | ($V_{CCIO}$/2) + 0.3 | V |
| $I_{IN}$ | Input Current | Power on | — | — | ±10 | µA |

1. Typical.

### subLVDS

**Over Recommended Operating Conditions**

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input Voltage | $V_{CCIO}$[1] = 1.8 | 0 | — | 1.8 | V |
| $V_{THD}$ | Differential Input Threshold | | 100 | 150 | 200 | mV |
| $V_{CM}$ | Input Common Mode Voltage | $V_{CCIO}$[1] = 1.8 | ($V_{CCIO}$/2) - 0.25 | $V_{CCIO}$/2 | ($V_{CCIO}$/2) + 0.25 | V |
| $I_{IN}$ | Input Current | Power on | — | — | ±10 | µA |

1. Typical.

## SubLVDS Emulation

The iCE40 family supports the differential subLVDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all banks of the devices. The subLVDS input standard is supported by the LVDS25 differential input buffer. The scheme shown in Figure 3-2 is one possible solution for subLVDSE output standard implementation. Use LVDS25E mode with suggested resistors for subLVDSE operation. Resistor values in Figure 3-2 are industry standard values for 1% resistors.

***Figure 3-2. subLVDSE***

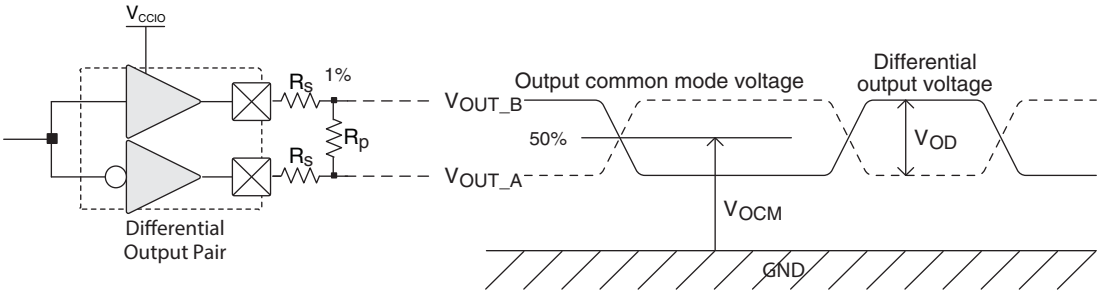



***Table 3-2. subLVDSE DC Conditions***

**Over Recommended Operating Conditions**

| Parameter | Description | Typ. | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | Ohms |
| $R_S$ | Driver series resistor | 270 | Ohms |
| $R_P$ | Driver parallel resistor | 120 | Ohms |
| $R_T$ | Receiver termination | 100 | Ohms |
| $V_{OH}$ | Output high voltage | 1.43 | V |
| $V_{OL}$ | Output low voltage | 1.07 | V |
| $V_{OD}$ | Output differential voltage | 0.35 | V |
| $V_{CM}$ | Output common mode voltage | 0.9 | V |
| $Z_{BACK}$ | Back impedance | 100.5 | Ohms |
| $I_{DC}$ | DC output current | 2.8 | mA |

## Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

## Maximum sysIO Buffer Performance[2]

| I/O Standard | Max. Speed | Units |
|---|---|---|
| **Inputs** | | |
| LVDS25[1] | 400 | MHz |
| subLVDS18[1] | 400 | MHz |
| LVCMOS33 | 250 | MHz |
| LVCMOS25 | 250 | MHz |
| LVCMOS18 | 250 | MHz |
| **Outputs** | | |
| LVDS25E | 250 | MHz |
| subLVDS18E | 155 | MHz |
| LVCMOS33 | 250 | MHz |
| LVCMOS25 | 250 | MHz |
| LVCMOS18 | 155 | MHz |

1. Supported in Bank 3 only.
2. Measured with a toggling pattern

## iCE40 Family Timing Adders

**Over Recommended Commercial Operating Conditions - LP Devices[1, 2, 3, 4, 5]**

| Buffer Type | Description | Timing | Units |
|---|---|---|---|
| **Input Adjusters** | | | |
| LVDS25 | LVDS, $V_{CCIO}$ = 2.5 V | –0.18 | ns |
| subLVDS | subLVDS, $V_{CCIO}$ = 1.8 V | 0.82 | ns |
| LVCMOS33 | LVCMOS, $V_{CCIO}$ = 3.3 V | 0.18 | ns |
| LVCMOS25 | LVCMOS, $V_{CCIO}$ = 2.5 V | 0.00 | ns |
| LVCMOS18 | LVCMOS, $V_{CCIO}$ = 1.8 V | 0.19 | ns |
| **Output Adjusters** | | | |
| LVDS25E | LVDS, Emulated, $V_{CCIO}$ = 2.5 V | 0.00 | ns |
| subLVDSE | subLVDS, Emulated, $V_{CCIO}$ = 1.8 V | 1.32 | ns |
| LVCMOS33 | LVCMOS, $V_{CCIO}$ = 3.3 V | –0.12 | ns |
| LVCMOS25 | LVCMOS, $V_{CCIO}$ = 2.5 V | 0.00 | ns |
| LVCMOS18 | LVCMOS, $V_{CCIO}$ = 1.8 V | 1.32 | ns |

1. Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Commercial timing numbers are shown.
5. Not all I/O standards are supported for all banks. See the Architecture section of this data sheet for details.

## iCE40 External Switching Characteristics – LP Devices (Continued)[1, 2]

**Over Recommended Operating Conditions**

| Parameter | Description | Device | Min. | Max. | Units |
|---|---|---|---|---|---|
| $t_{HPLL}$ | Clock to Data Hold - PIO Input Register | iCE40LP1K | –0.90 | — | ns |
| | | iCE40LP4K | –0.80 | — | ns |
| | | iCE40LP8K | –0.80 | — | ns |

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions can be extracted from the iCECube2 software.
2. General I/O timing numbers based on LVCMOS 2.5, 0pf load.
3. Supported on devices with a PLL.

# iCE40 External Switching Characteristics – HX Devices [1, 2]

**Over Recommended Operating Conditions**

| Parameter | Description | Device | Min. | Max. | Units |
|---|---|---|---|---|---|
| **Clocks** | | | | | |
| **Primary Clocks** | | | | | |
| $f_{MAX\_GBUF}$ | Frequency for Global Buffer Clock network | All iCE40HX devices | — | 275 | MHz |
| $t_{W\_GBUF}$ | Clock Pulse Width for Global Buffer | All iCE40HX devices | 0.88 | — | ns |
| $t_{SKEW\_GBUF}$ | Global Buffer Clock Skew Within a Device | iCE40HX1K | — | 727 | ps |
| | | iCE40HX4K | — | 300 | ps |
| | | iCE40HX8K | — | 300 | ps |
| **Pin-LUT-Pin Propagation Delay** | | | | | |
| $t_{PD}$ | Best case propagation delay through one LUT-4 | All iCE40 HX devices | — | 7.30 | ns |
| **General I/O Pin Parameters (Using Global Buffer Clock without PLL)** | | | | | |
| $t_{SKEW\_IO}$ | Data bus skew across a bank of IOs | iCE40HX1K | — | 696 | ps |
| | | iCE40HX4K | — | 290 | ps |
| | | iCE40HX8K | — | 290 | ps |
| $t_{CO}$ | Clock to Output - PIO Output Register | iCE40HX1K | — | 5.00 | ns |
| | | iCE40HX4K | — | 5.41 | ns |
| | | iCE40HX8K | — | 5.41 | ns |
| $t_{SU}$ | Clock to Data Setup - PIO Input Register | iCE40HX1K | –0.23 | — | ns |
| | | iCE40HX4K | –0.43 | — | ns |
| | | iCE40HX8K | –0.43 | — | ns |
| $t_{H}$ | Clock to Data Hold - PIO Input Register | iCE40HX1K | 1.92 | — | ns |
| | | iCE40HX4K | 2.38 | — | ns |
| | | iCE40HX8K | 2.38 | — | ns |
| **General I/O Pin Parameters (Using Global Buffer Clock with PLL)[3]** | | | | | |
| $t_{COPLL}$ | Clock to Output - PIO Output Register | iCE40HX1K | — | 2.96 | ns |
| | | iCE40HX4K | — | 2.51 | ns |
| | | iCE40HX8K | — | 2.51 | ns |
| $t_{SUPLL}$ | Clock to Data Setup - PIO Input Register | iCE40HX1K | 3.10 | — | ns |
| | | iCE40HX4K | 4.16 | — | ns |
| | | iCE40HX8K | 4.16 | — | ns |
| $t_{HPLL}$ | Clock to Data Hold - PIO Input Register | iCE40HX1K | –0.60 | — | ns |
| | | iCE40HX4K | –0.53 | — | ns |
| | | iCE40HX8K | –0.53 | — | ns |

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the iCECube2 software.
2. General I/O timing numbers based on LVCMOS 2.5, 0pf load.
3. Supported on devices with a PLL.

## SPI Master or NVCM Configuration Time[1, 2]

| Symbol | Parameter | Conditions | Typ. | Units |
|---|---|---|---|---|
| $t_{CONFIG}$ | POR/CRESET_B to Device I/O Active | iCE40LP384 - Low Frequency (Default) | 25 | ms |
| | | iCE40LP384 - Medium Frequency | 15 | ms |
| | | iCE40LP384 - High Frequency | 11 | ms |
| | | iCE40LP640 - Low Frequency (Default) | 53 | ms |
| | | iCE40LP640 - Medium Frequency | 25 | ms |
| | | iCE40LP640 - High Frequency | 13 | ms |
| | | iCE40LP/HX1K - Low Frequency (Default) | 53 | ms |
| | | iCE40LP/HX1K - Medium Frequency | 25 | ms |
| | | iCE40LP/HX1K - High Frequency | 13 | ms |
| | | iCE40LP/HX4K - Low Frequency (Default) | 230 | ms |
| | | iCE40LP/HX4K - Medium Frequency | 110 | ms |
| | | iCE40LP/HX4K - High Frequency | 70 | ms |
| | | iCE40LP/HX8K - Low Frequency (Default) | 230 | ms |
| | | iCE40LP/HX8K - Medium Frequency | 110 | ms |
| | | iCE40LP/HX8K - High Frequency | 70 | ms |

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

# iCE40 LP/HX Family Data Sheet Ordering Information

March 2017 Data Sheet DS1040

## iCE40 Part Number Description

### Ultra Low Power (LP) Devices

ICE40LPXXX – XXXXXXX

**Device Family**
iCE40 FPGA

**Series**
LP = Low Power Series

**Logic Cells**
384 = 384 Logic Cells
640 = 640 Logic Cells
1K = 1,280 Logic Cells
4K = 3,520 Logic Cells
8K = 7,680 Logic Cells

**Shipping Method**
TR = Tape and Reel
TR50 = Tape and Reel 50 units
TR1K = Tape and Reel 1,000 units

**Package**
SWG16 = 16-Ball WLCSP (0.35 mm Pitch)
CM36 = 36-Ball ucBGA (0.4 mm Pitch)
CM49 = 49-Ball ucBGA (0.4 mm Pitch)
CM81 = 81-Ball ucBGA (0.4 mm Pitch)
CB81 = 81-Ball csBGA (0.5 mm Pitch)
CM121 = 121-Ball ucBGA (0.4 mm Pitch)
CB121 = 121-Ball csBGA (0.5 mm Pitch)
CM225 = 225-Ball ucBGA (0.4 mm Pitch)
SG32 = 32-Pin QFN (0.5 mm Pitch)
QN84 = 84-Pin QFN (0.5 mm Pitch)

### High Performance (HX) Devices

ICE40HXXX – XXXXXXX

**Device Family**
iCE40 mobileFPGA

**Series**
HX = High-Performance Series

**Logic Cells**
1K = 1,280 Logic Cells
4K = 3,520 Logic Cells
8K = 7,680 Logic Cells

**Shipping Method**
TR = Tape and Reel

**Package**
CB132 = 132-Ball csBGA (0.5 mm Pitch)
CM225 = 225-Ball ucBGA (0.4 mm Pitch)
CT256 = 256-Ball caBGA (0.8 mm Pitch)
TQ144 = 144-Pin TQFP (0.5 mm Pitch)
VQ100 = 100-Pin VQFP (0.5 mm Pitch)
BG121 = 121-Ball caBGA (0.8 mm Pitch)

All parts shipped in trays unless noted.

## Ordering Information

iCE40 devices have top-side markings as shown below:

**Industrial**


Note: Markings are abbreviated for small packages.

## Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

| Part Number | LUTs | Supply Voltage | Package | Leads | Temp. |
|---|---|---|---|---|---|
| ICE40LP384-CM36 | 384 | 1.2 V | Halogen-Free ucBGA | 36 | IND |
| ICE40LP384-CM36TR | 384 | 1.2 V | Halogen-Free ucBGA | 36 | IND |
| ICE40LP384-CM36TR1K | 384 | 1.2 V | Halogen-Free ucBGA | 36 | IND |
| ICE40LP384-CM49 | 384 | 1.2 V | Halogen-Free ucBGA | 49 | IND |
| ICE40LP384-CM49TR | 384 | 1.2 V | Halogen-Free ucBGA | 49 | IND |
| ICE40LP384-CM49TR1K | 384 | 1.2 V | Halogen-Free ucBGA | 49 | IND |
| ICE40LP384-SG32 | 384 | 1.2 V | Halogen-Free QFN | 32 | IND |
| ICE40LP384-SG32TR | 384 | 1.2 V | Halogen-Free QFN | 32 | IND |
| ICE40LP384-SG32TR1K | 384 | 1.2 V | Halogen-Free QFN | 32 | IND |
| ICE40LP640-SWG16TR | 640 | 1.2 V | Halogen-Free WLCSP | 16 | IND |
| ICE40LP640-SWG16TR50 | 640 | 1.2 V | Halogen-Free WLCSP | 16 | IND |
| ICE40LP640-SWG16TR1K | 640 | 1.2 V | Halogen-Free WLCSP | 16 | IND |
| ICE40LP1K-SWG16TR | 1280 | 1.2 V | Halogen-Free WLCSP | 16 | IND |
| ICE40LP1K-SWG16TR50 | 1280 | 1.2 V | Halogen-Free WLCSP | 16 | IND |
| ICE40LP1K-SWG16TR1K | 1280 | 1.2 V | Halogen-Free WLCSP | 16 | IND |
| ICE40LP1K-CM36 | 1280 | 1.2 V | Halogen-Free ucBGA | 36 | IND |
| ICE40LP1K-CM36TR | 1280 | 1.2 V | Halogen-Free ucBGA | 36 | IND |
| ICE40LP1K-CM36TR1K | 1280 | 1.2 V | Halogen-Free ucBGA | 36 | IND |
| ICE40LP1K-CM49 | 1280 | 1.2 V | Halogen-Free ucBGA | 49 | IND |
| ICE40LP1K-CM49TR | 1280 | 1.2 V | Halogen-Free ucBGA | 49 | IND |
| ICE40LP1K-CM49TR1K | 1280 | 1.2 V | Halogen-Free ucBGA | 49 | IND |
| ICE40LP1K-CM81 | 1280 | 1.2 V | Halogen-Free ucBGA | 81 | IND |
| ICE40LP1K-CM81TR | 1280 | 1.2 V | Halogen-Free ucBGA | 81 | IND |
| ICE40LP1K-CM81TR1K | 1280 | 1.2 V | Halogen-Free ucBGA | 81 | IND |
| ICE40LP1K-CB81 | 1280 | 1.2 V | Halogen-Free csBGA | 81 | IND |
| ICE40LP1K-CB81TR | 1280 | 1.2 V | Halogen-Free csBGA | 81 | IND |
| ICE40LP1K-CB81TR1K | 1280 | 1.2 V | Halogen-Free csBGA | 81 | IND |
| ICE40LP1K-CM121 | 1280 | 1.2 V | Halogen-Free ucBGA | 121 | IND |
| ICE40LP1K-CM121TR | 1280 | 1.2 V | Halogen-Free ucBGA | 121 | IND |
| ICE40LP1K-CM121TR1K | 1280 | 1.2 V | Halogen-Free ucBGA | 121 | IND |
| ICE40LP1K-CB121 | 1280 | 1.2 V | Halogen-Free csBGA | 121 | IND |
| ICE40LP1K-QN84 | 1280 | 1.2 V | Halogen-Free QFN | 84 | IND |
| ICE40LP4K-CM81 | 3520 | 1.2 V | Halogen-Free ucBGA | 81 | IND |
| ICE40LP4K-CM81TR | 3520 | 1.2 V | Halogen-Free ucBGA | 81 | IND |
| ICE40LP4K-CM81TR1K | 3520 | 1.2 V | Halogen-Free ucBGA | 81 | IND |
| ICE40LP4K-CM121 | 3520 | 1.2 V | Halogen-Free ucBGA | 121 | IND |
| ICE40LP4K-CM121TR | 3520 | 1.2 V | Halogen-Free ucBGA | 121 | IND |
| ICE40LP4K-CM121TR1K | 3520 | 1.2 V | Halogen-Free ucBGA | 121 | IND |
| ICE40LP4K-CM225 | 3520 | 1.2 V | Halogen-Free ucBGA | 225 | IND |
| ICE40LP8K-CM81 | 7680 | 1.2 V | Halogen-Free ucBGA | 81 | IND |
| ICE40LP8K-CM81TR | 7680 | 1.2 V | Halogen-Free ucBGA | 81 | IND |
| ICE40LP8K-CM81TR1K | 7680 | 1.2 V | Halogen-Free ucBGA | 81 | IND |
| ICE40LP8K-CM121 | 7680 | 1.2 V | Halogen-Free ucBGA | 121 | IND |
| ICE40LP8K-CM121TR | 7680 | 1.2 V | Halogen-Free ucBGA | 121 | IND |

# iCE40 LP/HX Family Data Sheet Revision History

**March 2017** **Data Sheet DS1040**

| Date | Version | Section | Change Summary |
|---|---|---|---|
| March 2017 | 3.3 | Introduction | Updated Features section. Added 121-ball caBGA package for ICE40 HX4K/8K to Table 1-1, iCE40 Family Selection Guide. |
| | | Architecture | Updated PLB Blocks section. Changed “subtracters” to “subtractors” in the Carry Logic description. |
| | | | Updated Clock/Control Distribution Network section. Switched the “Clock Enable“ and the “Reset” headings in Table 2-2, Global Buffer (GBUF) Connections to Programmable Logic Blocks. |
| | | Pinout Information | Updated Pin Information Summary section. Added BG121information under iCE40HX4K and iCE40HX8K. |
| | | Ordering Information | Updated iCE40 Part Number Description section. Added Shipping Method and BG121 package under High Performance (HX) Devices. |
| | | | Updated Ordering Information section. Added part numbers for BG121 under High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging. |
| | | Supplemental Information | Corrected reference to “Package Diagrams Data Sheet”. |
| October 2015 | 3.2 | Introduction | Updated Features section. Added footnote to 16 WLCSP Programmable I/O: Max Inputs (LVDS25) in Table 1-1, iCE40 Family Selection Guide. |
| | | DC and Switching Characteristics | Updated sysCLOCK PLL Timing section. Changed $t_{DT}$ conditions. |
| | | | Updated Programming NVCM Supply Current – LP Devices section. Changed $I_{PP\_2V5}$ and $I_{CCIO}$, $I_{CC\_SPI}$ units. |
| March 2015 | 3.1 | DC and Switching Characteristics | Updated sysIO Single-Ended DC Electrical Characteristics section. Changed LVCMOS 3.3 and LVCMOS 2. 5 $V_{OH}$ Min. (V) from 0.5 to 0.4. |
| July 2014 | 3.0 | DC and Switching Characteristics | Revised and/or added Typ. $V_{CC}$ data in the following sections.<br>— Static Supply Current – LP Devices<br>— Static Supply Current – HX Devices<br>— Programming NVCM Supply Current – LP Devices<br>— Programming NVCM Supply Current – HX Devices<br>In each section table, the footnote indicating Advanced device status was removed. |
| | | Pinout Information | Updated Pin Information Summary section. Added footnote 1 to CM49 under iCE40LP1K. |
| April 2014 | 02.9 | Ordering Information | Changed “i” to “I” in part number description and ordering part numbers. |
| | | | Added part numbers to the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table. |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| February 2014 | 02.8 | Introduction | Updated Features section.<br>— Corrected standby power units.<br>— Included High Current LED Drivers |
| | | | Updated Table 1-1, iCE40 Family Selection Guide.<br>— Removed LP384 Programmable I/O for 81 ucBGA package. |
| | | Architecture | Updated Supported Standards section. Added information on High Current LED drivers. |
| | | DC and Switching Characteristics | Corrected typos. |
| | | | Added footnote to the Peak Startup Supply Current – LP Devices table. |
| | | Ordering Information | Updated part number description in the Ultra Low Power (LP) Devices section. |
| | | | Added part numbers to the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table. |
| October 2013 | 02.7 | Introduction | Updated Features list and iCE40 Family Selection Guide table. |
| | | Architecture | Revised iCE40-1K device to iCE40LP/HX1K device. |
| | | DC and Switching Characteristics | Added iCE40LP640 device information. |
| | | Pinout Information | Added iCE40LP640 and iCE40LP1K information. |
| | | Ordering Information | Added iCE40LP640 and iCE40LP1K information. |
| September 2013 | 02.6 | DC and Switching Characteristics | Updated Absolute Maximum Ratings section. |
| | | | Updated sysCLOCK PLL Timing – Preliminary table. |
| | | Pinout Information | Updated Pin Information Summary table. |
| August 2013 | 02.5 | Introduction | Updated the iCE40 Family Selection Guide table. |
| | | DC and Switching Characteristics | Updated the following tables:<br>— Absolute Maximum Ratings<br>— Power-On-Reset Voltage Levels<br>— Static Supply Current – LP Devices<br>— Static Supply Current – HX Devices<br>— Programming NVCM Supply Current – LP Devices<br>— Programming NVCM Supply Current – HX Devices<br>— Peak Startup Supply Current – LP Devices<br>— sysIO Recommended Operating Conditions<br>— Typical Building Block Function Performance – HX Devices<br>— iCE40 External Switching Characteristics – HX Devices<br>— sysCLOCK PLL Timing – Preliminary<br>— SPI Master or NVCM Configuration Time |
| | | Pinout Information | Updated the Pin Information Summary table. |
| July 2013 | 02.4 | Introduction | Updated the iCE40 Family Selection Guide table. |
| | | DC and Switching Characteristics | Updated the sysCONFIG Port Timing Specifications table. |
| | | | Updated footnote in DC Electrical Characteristics table. |
| | | | GDDR tables removed. Support to be provided in a technical note. |
| | | Pinout Information | Updated the Pin Information Summary table. |
| | | Ordering Information | Updated the top-side markings figure. |
| | | | Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table. |
| May 2013 | 02.3 | DC and Switching Characteristics | Added new data from Characterization. |