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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

### Details

Product Status	Active
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	96
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40hx1k-tq144">https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40hx1k-tq144</a>

## Features

- **Flexible Logic Architecture**
  - Five devices with 384 to 7,680 LUT4s and 10 to 206 I/Os
- **Ultra Low Power Devices**
  - Advanced 40 nm low power process
  - As low as 21  $\mu$ A standby power
  - Programmable low swing differential I/Os
- **Embedded and Distributed Memory**
  - Up to 128 kbits sysMEM™ Embedded Block RAM
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
- **High Current LED Drivers**
  - Three High Current Drivers used for three different LEDs or one RGB LED
- **High Performance, Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8
    - LVDS25E, subLVDS
    - Schmitt trigger inputs, to 200 mV typical hysteresis
- Programmable pull-up mode
- **Flexible On-Chip Clocking**
  - Eight low-skew global clock resources
  - Up to two analog PLLs per device
- **Flexible Device Configuration**
  - SRAM is configured through:
    - Standard SPI Interface
    - Internal Nonvolatile Configuration Memory (NVCM)
- **Broad Range of Package Options**
  - WLCSP, QFN, VQFP, TQFP, ucBGA, caBGA, and csBGA package options
  - Small footprint package options
    - As small as 1.40 mm x 1.48 mm
  - Advanced halogen-free packaging

**Table 1-1. iCE40 Family Selection Guide**

Part Number	LP384	LP640	LP1K	LP4K	LP8K	HX1K	HX4K	HX8K
Logic Cells (LUT + Flip-Flop)	384	640	1,280	3,520	7,680	1,280	3,520	7,680
RAM4K Memory Blocks	0	8	16	20	32	16	20	32
RAM4K RAM bits	0	32K	64K	80K	128K	64K	80K	128K
Phase-Locked Loops (PLLs)	0	0	1 <sup>1</sup>	2 <sup>2</sup>	2 <sup>2</sup>	1 <sup>1</sup>	2	2
Maximum Programmable I/O Pins	63	25	95	167	178	95	95	206
Maximum Differential Input Pairs	8	3	12	20	23	11	12	26
High Current LED Drivers	0	3	3	0	0	0	0	0
Package	Code	Programmable I/O: Max Inputs (LVDS25)						
16 WLCSP (1.40 mm x 1.48 mm, 0.35 mm)	SWG16		10(0) <sup>1</sup>	10(0) <sup>1</sup>				
32 QFN (5 mm x 5 mm, 0.5 mm)	SG32	21(3)						
36 ucBGA (2.5 mm x 2.5 mm, 0.4 mm)	CM36	25(3)		25(3) <sup>1</sup>				
49 ucBGA (3 mm x 3 mm, 0.4 mm)	CM49	37(6)		35(5) <sup>1</sup>				
81 ucBGA (4 mm x 4 mm, 0.4 mm)	CM81			63(8)	63(9) <sup>2</sup>	63(9) <sup>2</sup>		
81 csBGA (5 mm x 5 mm, 0.5 mm)	CB81			62(9) <sup>1</sup>				

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**Table 1-1. iCE40 Family Selection Guide (continued)**

84 QFN (7 mm x 7 mm, 0.5 mm)	QN84			67(7) <sup>1</sup>					
100 VQFP (14 mm x 14 mm, 0.5 mm)	VQ100						72(9) <sup>1</sup>		
121 ucBGA (5 mm x 5 mm, 0.4 mm)	CM121			95(12)	93(13)	93(13)			
121 csBGA (6 mm x 6 mm, 0.5 mm)	CB121			92(12)					
121 caBGA (9 mm x 9 mm, 0.8 mm)	BG121							93(13)	93(13)
132 csBGA (8 mm x 8 mm, 0.5 mm)	CB132						95(11)	95(12)	95(12)
144 TQFP (20 mm x 20 mm, 0.5 mm)	TQ144						96(12)	107(14)	
225 ucBGA (7 mm x 7 mm, 0.4 mm)	CM225				178(23)	178(23)			178(23)
256-ball caBGA (14 mm x 14 mm, 0.8 mm)	CT256								206(26)

1. No PLL available on the 16 WLCSP, 36 ucBGA, 81 csBGA, 84 QFN and 100 VQFP packages.

2. Only one PLL available on the 81 ucBGA package.

3. High Current I/Os only available on the 16 WLCSP package.

## Introduction

The iCE40 family of ultra-low power, non-volatile FPGAs has five devices with densities ranging from 384 to 7680 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic, these devices feature Embedded Block RAM (EBR), Non-volatile Configuration Memory (NVCM) and Phase Locked Loops (PLLs). These features allow the devices to be used in low-cost, high-volume consumer and system applications. Select packages offer High-Current drivers that are ideal to drive three white LEDs, or one RGB LED.

The iCE40 devices are fabricated on a 40 nm CMOS low power process. The device architecture has several features such as programmable low-swing differential I/Os and the ability to turn off on-chip PLLs dynamically. These features help manage static and dynamic power consumption, resulting in low static power for all members of the family. The iCE40 devices are available in two versions – ultra low power (LP) and high performance (HX) devices.

The iCE40 FPGAs are available in a broad range of advanced halogen-free packages ranging from the space saving 1.40x1.48 mm WLCSP to the PCB-friendly 20x20 mm TQFP. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The iCE40 devices offer enhanced I/O features such as pull-up resistors. Pull-up features are controllable on a “per-pin” basis.

The iCE40 devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash or be configured by an external master such as a CPU.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 family of devices. Popular logic synthesis tools provide synthesis library support for iCE40. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40 FPGA family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

**Global Reset Control**

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

**sysCLOCK Phase Locked Loops (PLLs)**

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 devices have one or more sysCLOCK PLLs. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 6. The PLLOUT outputs can all be used to drive the iCE40 global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the  $t_{LOCK}$  parameter has been satisfied.

For more details on the PLL, see TN1251, [iCE40 sysCLOCK PLL Design and Usage Guide](#).

**Figure 2-3. PLL Diagram**

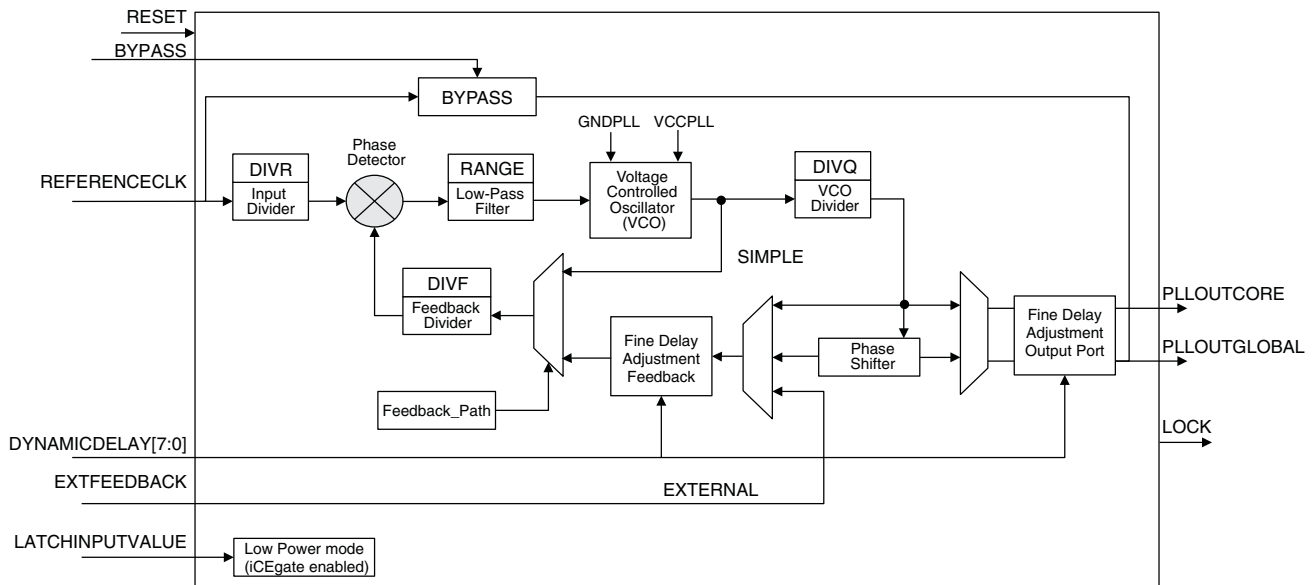


Table 2-3 provides signal descriptions of the PLL block.

**Table 2-3. PLL Signal Descriptions**

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	When FEEDBACK_PATH is set to SIMPLE, the BYPASS control selects which clock signal connects to the PLLOUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[3:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, forces the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.

### sysMEM Embedded Block RAM Memory

Larger iCE40 device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

### sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

**Table 2-4. sysMEM Block Configurations<sup>1</sup>**

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4K)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4K)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4K)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4K)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40 EBR primitives with a negative-edged Read or Write clock, the base primitive name is appended with a 'N' and a 'R' or 'W' depending on the clock that is affected.

**RAM Initialization and ROM Operation**

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Note the sysMEM Embedded Block RAM Memory address 0 cannot be initialized.

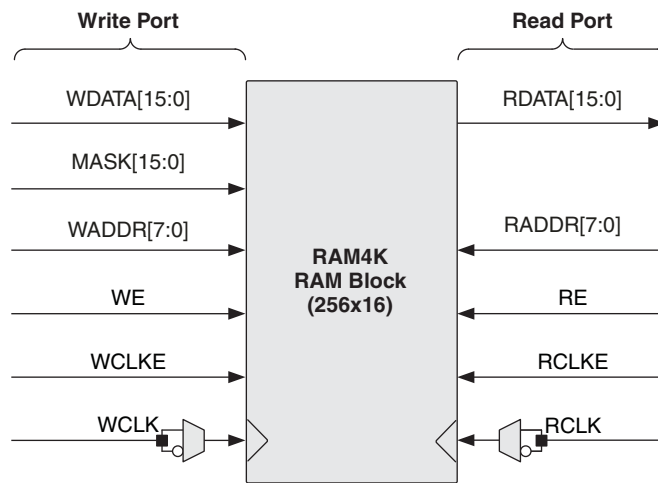
**Memory Cascading**

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

**RAM4k Block**

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

**Figure 2-4. sysMEM Memory Primitives**



**Table 2-5. EBR Signal Descriptions**

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = write bit; 1 = don't write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

For further information on the sysMEM EBR block, please refer to TN1250, [Memory Usage Guide for iCE40 Devices](#).

## sysIO

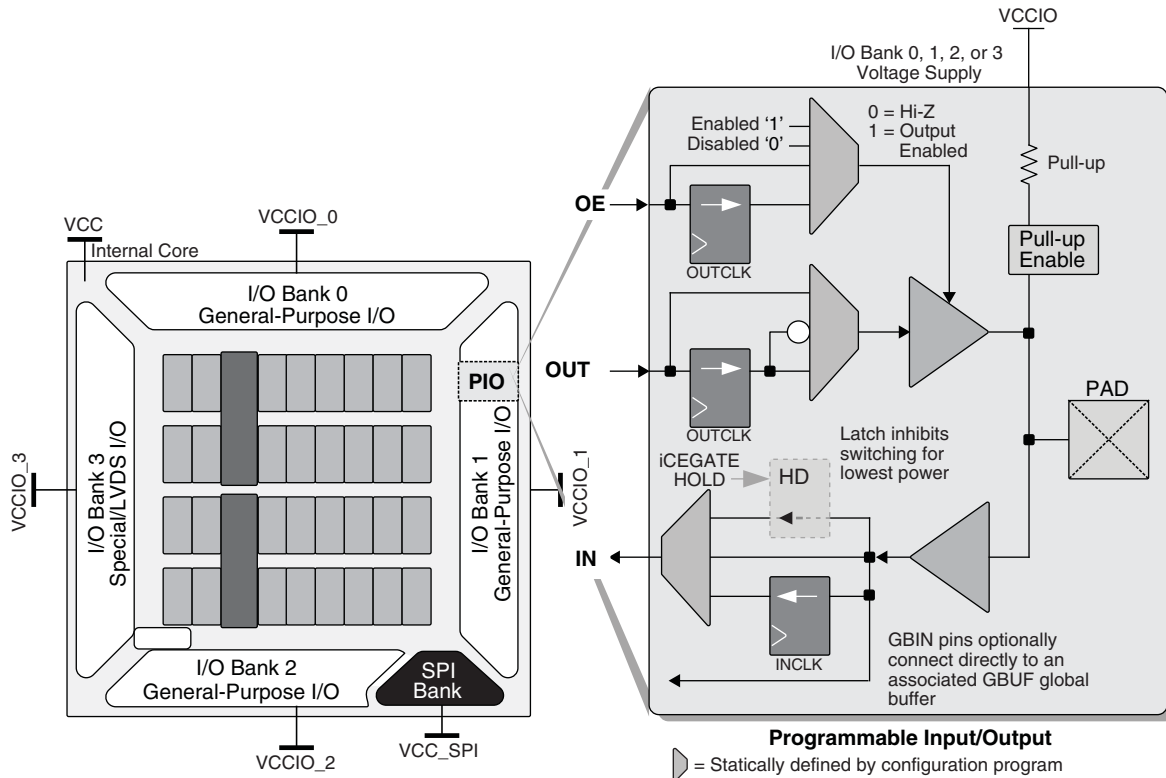
### Buffer Banks

iCE40 devices have up to four I/O banks with independent  $V_{CCIO}$  rails with an additional configuration bank  $V_{CC\_SPI}$  for the SPI I/Os.

### Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. The PIOs are placed on all four sides of the device.

**Figure 2-5. I/O Bank and Programmable I/O Cell**



The PIO contains three blocks: an input register block, output register block iCEgate™ and tri-state register block. To save power, the optional iCEgate™ latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

### Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock signal, creating two data streams.

### Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers. In Generic DDR mode, two registers are used to capture the data on the positive and negative edge of the system clock and then muxed creating one data stream.

Figure 2-6 shows the input/output register block for the PIOs.

## DC Electrical Characteristics

### Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^{1,3,4,5,6,7}$	Input or I/O Leakage	$0V < V_{IN} < V_{CCIO} + 0.2 V$	—	—	+/-10	$\mu A$
$C_1^{6,7}$	I/O Capacitance <sup>2</sup>	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V$ $V_{CC} = \text{Typ.}, V_{IO} = 0 \text{ to } V_{CCIO} + 0.2 V$	—	6	—	pf
$C_2^{6,7}$	Global Input Buffer Capacitance <sup>2</sup>	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V$ $V_{CC} = \text{Typ.}, V_{IO} = 0 \text{ to } V_{CCIO} + 0.2 V$	—	6	—	pf
$V_{HYST}$	Input Hysteresis	$V_{CCIO} = 1.8 V, 2.5 V, 3.3 V$	—	200	—	mV
$I_{PU}^{6,7}$	Internal PIO Pull-up Current	$V_{CCIO} = 1.8 V, 0 < V_{IN} <= 0.65 V_{CCIO}$	-3	—	-31	$\mu A$
		$V_{CCIO} = 2.5 V, 0 < V_{IN} <= 0.65 V_{CCIO}$	-8	—	-72	$\mu A$
		$V_{CCIO} = 3.3 V, 0 < V_{IN} <= 0.65 V_{CCIO}$	-11	—	-128	$\mu A$

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2.  $T_J = 25^\circ C$ ,  $f = 1.0 \text{ MHz}$ .
3. Please refer to  $V_{IL}$  and  $V_{IH}$  in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Only applies to IOs in the SPI bank following configuration.
5. Some products are clamped to a diode when  $V_{IN}$  is larger than  $V_{CCIO}$ .
6. High current IOs has three sysIO buffers connected together.
7. The iCE40LP640 and iCE40LP1K SWG16 package has CDONE and a sysIO buffer are connected together.

## Static Supply Current – LP Devices<sup>1, 2, 3, 4</sup>

Symbol	Parameter	Device	Typ. $V_{CC}^4$	Units
$I_{CC}$	Core Power Supply	iCE40LP384	21	$\mu A$
		iCE40LP640	100	$\mu A$
		iCE40LP1K	100	$\mu A$
		iCE40LP4K	250	$\mu A$
		iCE40LP8K	250	$\mu A$
$I_{CCPLL}^{5,6}$	PLL Power Supply	All devices	0.5	$\mu A$
$I_{PP\_2V5}$	NVCM Power Supply	All devices	1.0	$\mu A$
$I_{CCIO}, I_{CC\_SPI}$	Bank Power Supply <sup>4</sup> $V_{CCIO} = 2.5 V$	All devices	3.5	$\mu A$

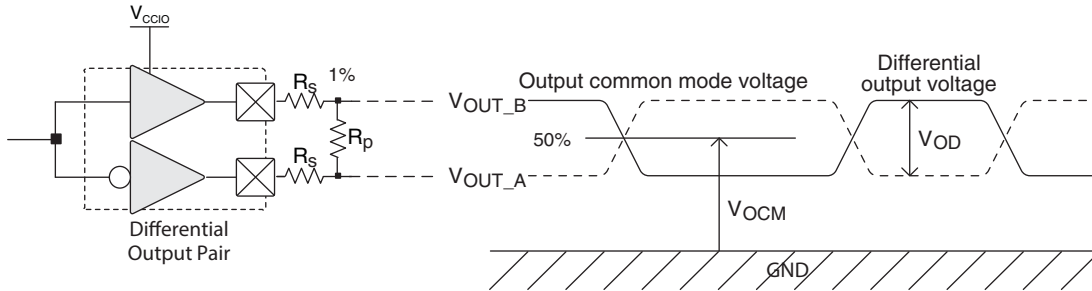
1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at  $V_{CCIO}$  or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3.  $T_J = 25^\circ C$ , power supplies at nominal voltage.
4. Does not include pull-up.
5. No PLL available on the iCE40LP384 and iCE40LP640 device.
6.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.



## LVDS25E Emulation

iCE40 devices can support LVDS25E outputs via emulation on all banks. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS25E standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

**Figure 3-1. LVDS25E Using External Resistors**



**Table 3-1. LVDS25E DC Conditions**

### Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
$Z_{OUT}$	Output impedance	20	Ohms
$R_S$	Driver series resistor	150	Ohms
$R_P$	Driver parallel resistor	140	Ohms
$R_T$	Receiver termination	100	Ohms
$V_{OH}$	Output high voltage	1.43	V
$V_{OL}$	Output low voltage	1.07	V
$V_{OD}$	Output differential voltage	0.30	V
$V_{CM}$	Output common mode voltage	1.25	V
$Z_{BACK}$	Back impedance	100.5	Ohms
$I_{DC}$	DC output current	6.03	mA

## Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

## Maximum sysIO Buffer Performance<sup>2</sup>

I/O Standard	Max. Speed	Units
<b>Inputs</b>		
LVDS25 <sup>1</sup>	400	MHz
subLVDS18 <sup>1</sup>	400	MHz
LVC MOS33	250	MHz
LVC MOS25	250	MHz
LVC MOS18	250	MHz
<b>Outputs</b>		
LVDS25E	250	MHz
subLVDS18E	155	MHz
LVC MOS33	250	MHz
LVC MOS25	250	MHz
LVC MOS18	155	MHz

1. Supported in Bank 3 only.
2. Measured with a toggling pattern

## iCE40 Family Timing Adders

Over Recommended Commercial Operating Conditions - LP Devices<sup>1, 2, 3, 4, 5</sup>

Buffer Type	Description	Timing	Units
<b>Input Adjusters</b>			
LVDS25	LVDS, $V_{CCIO} = 2.5\text{ V}$	-0.18	ns
subLVDS	subLVDS, $V_{CCIO} = 1.8\text{ V}$	0.82	ns
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3\text{ V}$	0.18	ns
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	0.00	ns
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	0.19	ns
<b>Output Adjusters</b>			
LVDS25E	LVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	0.00	ns
subLVDS25E	subLVDS, Emulated, $V_{CCIO} = 1.8\text{ V}$	1.32	ns
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3\text{ V}$	-0.12	ns
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	0.00	ns
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	1.32	ns

1. Timing adders are relative to LVC MOS25 and characterized but not tested on every device.
2. LVC MOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Commercial timing numbers are shown.
5. Not all I/O standards are supported for all banks. See the Architecture section of this data sheet for details.

**Over Recommended Commercial Operating Conditions - HX Devices<sup>1, 2, 3, 4, 5</sup>**

Buffer Type	Description	Timing	Units
<b>Input Adjusters</b>			
LVDS25	LVDS, $V_{CCIO} = 2.5\text{ V}$	0.13	ns
subLVDS	subLVDS, $V_{CCIO} = 1.8\text{ V}$	1.03	ns
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3\text{ V}$	0.16	ns
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	0.00	ns
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	0.23	ns
<b>Output Adjusters</b>			
LVDS25E	LVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	0.00	ns
subLVDS E	subLVDS, Emulated, $V_{CCIO} = 1.8\text{ V}$	1.76	ns
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3\text{ V}$	0.17	ns
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	0.00	ns
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	1.76	ns

1. Timing adders are relative to LVC MOS25 and characterized but not tested on every device.
2. LVC MOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Commercial timing numbers are shown.
5. Not all I/O standards are supported for all banks. See the Architecture section of this data sheet for details.

## iCE40 External Switching Characteristics – HX Devices <sup>1, 2</sup>

Over Recommended Operating Conditions

Parameter	Description	Device	Min.	Max.	Units
<b>Clocks</b>					
<b>Primary Clocks</b>					
$f_{MAX\_GBUF}$	Frequency for Global Buffer Clock network	All iCE40HX devices	—	275	MHz
$t_{W\_GBUF}$	Clock Pulse Width for Global Buffer	All iCE40HX devices	0.88	—	ns
$t_{SKEW\_GBUF}$	Global Buffer Clock Skew Within a Device	iCE40HX1K	—	727	ps
		iCE40HX4K	—	300	ps
		iCE40HX8K	—	300	ps
<b>Pin-LUT-Pin Propagation Delay</b>					
$t_{PD}$	Best case propagation delay through one LUT-4	All iCE40 HX devices	—	7.30	ns
<b>General I/O Pin Parameters (Using Global Buffer Clock without PLL)</b>					
$t_{SKEW\_IO}$	Data bus skew across a bank of IOs	iCE40HX1K	—	696	ps
		iCE40HX4K	—	290	ps
		iCE40HX8K	—	290	ps
$t_{CO}$	Clock to Output - PIO Output Register	iCE40HX1K	—	5.00	ns
		iCE40HX4K	—	5.41	ns
		iCE40HX8K	—	5.41	ns
$t_{SU}$	Clock to Data Setup - PIO Input Register	iCE40HX1K	-0.23	—	ns
		iCE40HX4K	-0.43	—	ns
		iCE40HX8K	-0.43	—	ns
$t_H$	Clock to Data Hold - PIO Input Register	iCE40HX1K	1.92	—	ns
		iCE40HX4K	2.38	—	ns
		iCE40HX8K	2.38	—	ns
<b>General I/O Pin Parameters (Using Global Buffer Clock with PLL)<sup>3</sup></b>					
$t_{COPLL}$	Clock to Output - PIO Output Register	iCE40HX1K	—	2.96	ns
		iCE40HX4K	—	2.51	ns
		iCE40HX8K	—	2.51	ns
$t_{SUPLL}$	Clock to Data Setup - PIO Input Register	iCE40HX1K	3.10	—	ns
		iCE40HX4K	4.16	—	ns
		iCE40HX8K	4.16	—	ns
$t_{HPLL}$	Clock to Data Hold - PIO Input Register	iCE40HX1K	-0.60	—	ns
		iCE40HX4K	-0.53	—	ns
		iCE40HX8K	-0.53	—	ns

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the iCECube2 software.

2. General I/O timing numbers based on LVCMOS 2.5, 0pf load.

3. Supported on devices with a PLL.

## sysCLOCK PLL Timing

### Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
$f_{IN}$	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)		10	133	MHz
$f_{OUT}$	Output Clock Frequency (PLLOUT)		16	275	MHz
$f_{VCO}$	PLL VCO Frequency		533	1066	MHz
$f_{PFD}$	Phase Detector Input Frequency		10	133	MHz
<b>AC Characteristics</b>					
$t_{DT}$	Output Clock Duty Cycle	$f_{OUT} < 175$ MHz	40	50	%
		$175 \text{ MHz} < f_{OUT} < 275$ MHz	35	65	"%
$t_{PH}$	Output Phase Accuracy		—	+/-12	deg
$t_{OPJIT}^{1,5}$	Output Clock Period Jitter	$f_{OUT} \leq 100$ MHz	—	450	ps p-p
		$f_{OUT} > 100$ MHz	—	0.05	UIPP
	Output Clock Cycle-to-cycle Jitter	$f_{OUT} \leq 100$ MHz	—	750	ps p-p
		$f_{OUT} > 100$ MHz	—	0.10	UIPP
	Output Clock Phase Jitter	$f_{PFD} \leq 25$ MHz	—	275	ps p-p
		$f_{PFD} > 25$ MHz	—	0.05	UIPP
$t_W$	Output Clock Pulse Width	At 90% or 10%	1.3	—	ns
$t_{LOCK}^{2,3}$	PLL Lock-in Time		—	50	us
$t_{UNLOCK}$	PLL Unlock Time		—	50	ns
$t_{IPJIT}^4$	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
$t_{FDTAP}$	Fine Delay adjustment, per Tap		147	195	ps
$t_{STABLE}^3$	LATCHINPUTVALUE LOW to PLL Stable		—	500	ns
$t_{STABLE\_PW}^3$	LATCHINPUTVALUE Pulse Width		—	100	ns
$t_{RST}$	RESET Pulse Width		10	—	ns
$t_{RSTREC}$	RESET Recovery Time		10	—	us
$t_{DYNAMIC\_WD}$	DYNAMICDELAY Pulse Width		100	—	VCO Cycles
$t_{PDBYPASS}$	Propagation delay with the PLL in bypass mode	iCE40LP	1.18	4.68	ns
		iCE40HX	1.73	4.07	ns

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after  $t_{LOCK}$  for PLL reset and dynamic delay adjustment.
3. At minimum  $f_{PFD}$ . As the  $f_{PFD}$  increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

**SPI Master or NVCM Configuration Time<sup>1, 2</sup>**

Symbol	Parameter	Conditions	Typ.	Units
t <sub>CONFIG</sub>	POR/CRESET_B to Device I/O Active	iCE40LP384 - Low Frequency (Default)	25	ms
		iCE40LP384 - Medium Frequency	15	ms
		iCE40LP384 - High Frequency	11	ms
		iCE40LP640 - Low Frequency (Default)	53	ms
		iCE40LP640 - Medium Frequency	25	ms
		iCE40LP640 - High Frequency	13	ms
		iCE40LP/HX1K - Low Frequency (Default)	53	ms
		iCE40LP/HX1K - Medium Frequency	25	ms
		iCE40LP/HX1K - High Frequency	13	ms
		iCE40LP/HX4K - Low Frequency (Default)	230	ms
		iCE40LP/HX4K - Medium Frequency	110	ms
		iCE40LP/HX4K - High Frequency	70	ms
		iCE40LP/HX8K - Low Frequency (Default)	230	ms
		iCE40LP/HX8K - Medium Frequency	110	ms
		iCE40LP/HX8K - High Frequency	70	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.

2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

### Signal Descriptions

Signal Name	I/O	Descriptions
<b>General Purpose</b>		
IO[Bank]_[Row/Column Number][A/B]	I/O	[Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number on the device.
IO[Bank]_[Row/Column Number][A/B]	I/O	[Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number on the device. [A/B] indicates the differential I/O. 'A' = negative input. 'B' = positive input.
HCIO[Bank]_[Number]	I/O	High Current IO. [Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number.
NC	—	No connect
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together.
VCC	—	VCC – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.
VCCIO_x	—	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. All VCCIOs located in the same bank are tied to the same supply.
<b>PLL and Global Functions (Used as user-programmable I/O pins when not used for PLL or clock pins)</b>		
VCCPLLx	—	PLL VCC – Power. Dedicated pins. The PLL requires a separate power and ground that is quiet and stable to reduce the output clock jitter of the PLL.
GNDPLLx	—	PLL GND – Ground. Dedicated pins. The sysCLOCK PLL has the DC ground connection made on the FPGA, so the external PLL ground connection (GNDPLL) must NOT be connected to the board's ground.
GBINx	—	Global pads. Two per side.
<b>Programming and Configuration</b>		
CBSEL[0:1]	I/O	Dual function pins. I/Os when not used as CBSEL. Optional ColdBoot configuration SElect input, if ColdBoot mode is enabled.
CRESET_B	I	Configuration Reset, active Low. Dedicated input. No internal pull-up resistor. Either actively drive externally or connect a 10 KOhm pull-up resistor to VCCIO_2.
CDONE	I/O	Configuration Done. Includes a permanent weak pull-up resistor to VCCIO_2. If driving external devices with CDONE output, an external pull-up resistor to VCCIO_2 may be required. Refer to the TN1248, <a href="#">iCE40 Programming and Configuration</a> for more details. Following device configuration the iCE40LP640 and iCE40LP1K in the SWG16 package CDONE pin can be used as a user output.
VCC_SPI	—	SPI interface voltage supply input. Must have a valid voltage even if configuring from NVCM.
SPI_SCK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA configuration modes.
SPI_SS_B	I/O	SPI Slave Select. Active Low. Includes an internal weak pull-up resistor to VCC_SPI during configuration. During configuration, the logic level sampled on this pin determines the configuration mode used by the iCE40 device. An input when sampled at the start of configuration. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in Master SPI Flash configuration mode.
SPI_SI	I/O	Slave SPI serial data input and master SPI serial data output
SPI_SO	I/O	Slave SPI serial data output and master SPI serial data input

### Pin Information Summary

	iCE40LP384			iCE40LP640	iCE40LP1K							
	SG32	CM36 <sup>2</sup>	CM49 <sup>2</sup>	SWG16	SWG16	CM36 <sup>1,2</sup>	CM49 <sup>1,2</sup>	CM81	CB81	QN84	CM121	CB121
<b>General Purpose I/O per Bank</b>												
Bank 0	6	4	10	3	3	4	10	17	17	17	24	24
Bank 1	5	7	7	0	0	7	7	15	16	17	25	21
Bank 2	0	4	4	1	1	4	4	11	8	11	18	19
Bank 3	6	6	12	2	2	6	10	16	17	18	24	24
Configuration	4	4	4	4	4	4	4	4	4	4	4	4
Total General Purpose Single Ended I/O	21	25	37	10	10	25	35	63	62	67	95	92
<b>High Current Outputs per Bank</b>												
Bank 0	0	0	0	3	3	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0	0	0	0
Bank 3	0	0	0	0	0	0	0	0	0	0	0	0
Total Current Outputs	0	0	0	3	3	0	0	0	0	0	0	0
<b>Differential Inputs per Bank</b>												
Bank 0	0	0	0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0	0	0	0
Bank 3	3	3	6	1	1	3	5	8	9	7	12	12
Total Differential Inputs	3	3	6	1	1	3	5	8	9	7	12	12
<b>Dedicated Inputs per Bank</b>												
Bank 0	0	0	0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0	0	0	0
Bank 2	2	2	2	1	1	2	2	2	2	2	2	2
Bank 3	0	0	0	0	0	0	0	0	0	0	0	0
Configuration	0	0	0	0	0	0	0	0	0	0	0	0
Total Dedicated Inputs	2	2	2	1	1	2	2	2	2	2	2	2
<b>Vccio Pins</b>												
Bank 0	1	1	1	1	1	1	1	1	1	1	2	1
Bank 1	1	1	1	0	0	0	0	1	1	1	2	1
Bank 2	1	1	1	1	1	1	1	1	1	1	2	1
Bank 3	1	0	0	0	0	0	0	1	1	1	2	2
VCC	1	1	2	1	1	1	2	3	3	4	4	4
VCC_SPI	1	1	1	0	0	1	1	1	1	1	1	1
VPP_2V5	1	1	1	0	0	1	1	1	1	1	1	1
VPP_FAST <sup>3</sup>	0	0	0	0	0	1	1	1	0	1	1	1
VCCPLL	0	0	0	0	0	0	1	1	0	0	1	1
GND	2	3	3	2	2	3	4	5	8	4	8	11
NC	0	0	0	0	0	0	0	0	0	0	0	3
Total Count of Bonded Pins	32	36	49	16	16	36	49	81	81	84	121	121

1. V<sub>CCIO0</sub> and V<sub>CCIO1</sub> are connected together.
2. V<sub>CCIO2</sub> and V<sub>CCIO3</sub> are connected together.
3. V<sub>PP\_FAST</sub>: used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the V<sub>PP\_FAST</sub> ball connected to V<sub>CCIO\_0</sub> ball externally.



**Pin Information Summary (Continued)**

	iCE40LP4K			iCE40LP8K			iCE40HX1K		
	CM81	CM121	CM225	CM81	CM121	CM225	VQ100	CB132	TQ144
<b>General Purpose I/O per Bank</b>									
Bank 0	17	23	46	17	23	46	19	24	23
Bank 1	15	21	42	15	21	42	19	25	25
Bank 2	9	19	40	9	19	40	12	20	20
Bank 3	18	26	46	18	26	46	18	22	24
Configuration	4	4	4	4	4	4	4	4	4
Total General Purpose Single Ended I/O	63	93	178	63	93	178	72	95	96
<b>High Current Outputs per Bank</b>									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0
Bank 3	0	0	0	0	0	0	0	0	0
Total Differential Inputs	0	0	0	0	0	0	0	0	0
<b>Differential Inputs per Bank</b>									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0
Bank 3	9	13	23	9	13	23	9	11	12
Total Differential Inputs	9	13	23	9	13	23	9	11	12
<b>Dedicated Inputs per Bank</b>									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	1	0	0	1	0	1	1
Bank 2	2	2	2	2	2	2	2	2	2
Bank 3	0	0	0	0	0	0	0	0	0
Configuration	0	0	0	0	0	0	0	0	0
Total Dedicated Inputs	2	2	3	2	2	3	2	3	3
<b>Vccio Pins</b>									
Bank 0	1	1	3	1	1	3	2	2	2
Bank 1	1	1	3	1	1	3	2	2	2
Bank 2	1	1	3	1	1	3	2	2	2
Bank 3	1	2	4	1	2	4	3	3	2
VCC	3	4	8	3	4	8	4	5	4
VCC_SPI	1	1	1	1	1	1	1	1	1
VPP_2V5	1	1	1	1	1	1	1	1	1
VPP_FAST <sup>1</sup>	1	1	1	1	1	1	1	1	1
VCCPLL	1	2	2	1	2	2	0	1	1
GND	5	12	18	5	12	18	10	14	10
NC	0	0	0	0	0	0	0	2	19
Total Count of Bonded Pins	81	121	225	81	121	225	100	132	144

1. VPP\_FAST: used only for fast production programming, must be left floating or unconnected in applications.

## Pin Information Summary (Continued)

	iCE40HX4K			iCE40HX8K			
	BG121	CB132	TQ144	BG121	CB132	CM225	CT256
<b>General Purpose I/O per Bank</b>							
Bank 0	23	24	27	23	24	46	52
Bank 1	21	25	29	21	25	42	52
Bank 2	19	18	19	19	18	40	46
Bank 3	26	24	28	26	24	46	52
Configuration	4	4	4	4	4	4	4
Total General Purpose Single Ended I/O	93	95	107	93	95	178	206
<b>High Current Outputs per Bank</b>							
Bank 0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0
Bank 3	0	0	0	0	0	0	0
Total Differential Inputs	0	0	0	0	0	0	0
<b>Differential Inputs per Bank</b>							
Bank 0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0
Bank 3	13	12	14	13	12	23	26
Total Differential Inputs	13	12	14	13	12	23	26
<b>Dedicated Inputs per Bank</b>							
Bank 0	0	0	0	0	0	0	0
Bank 1	0	1	1	0	1	1	1
Bank 2	2	2	2	2	2	2	2
Bank 3	0	0	0	0	0	0	0
Configuration	0	0	0	0	0	0	0
Total Dedicated Inputs	2	3	3	2	3	3	3
<b>Vccio Pins</b>							
Bank 0	1	2	2	1	2	3	4
Bank 1	1	2	2	1	2	3	4
Bank 2	1	2	2	1	2	3	4
Bank 3	2	3	2	2	3	4	4
VCC	4	5	4	4	5	8	6
VCC_SPI	1	1	1	1	1	1	1
VPP_2V5	1	1	1	1	1	1	1
VPP_FAST <sup>1</sup>	1	1	1	1	1	1	1
VCCPLL	2	2	2	2	2	2	2
GND	12	15	11	12	15	18	20
NC	0	0	6	0	0	0	0
Total Count of Bonded Pins	121	132	144	121	132	225	256

1. VPP\_FAST, used only for fast production programming, must be left floating or unconnected in applications.

## For Further Information

A variety of technical notes for the iCE40 family are available on the Lattice web site.

- [TN1248, iCE40 Programming and Configuration](#)
- [TN1250, Memory Usage Guide for iCE40 Devices](#)
- [TN1251, iCE40 sysCLOCK PLL Design and Usage Guide](#)
- [TN1252, iCE40 Hardware Checklist](#)
- [TN1253, Using Differential I/O \(LVDS, Sub-LVDS\) in iCE40 Devices](#)
- [TN1074, PCB Layout Recommendations for BGA Packages](#)
- [iCE40 Pinout Files](#)
- [Thermal Management](#) document
- [Lattice design tools](#)
- [IBIS](#)
- [Package Diagrams Data Sheet](#)
- [Schematic Symbols](#)

Date	Version	Section	Change Summary
March 2017	3.3	Introduction	Updated <a href="#">Features</a> section. Added 121-ball caBGA package for ICE40 HX4K/8K to Table 1-1, iCE40 Family Selection Guide.
		Architecture	Updated <a href="#">PLB Blocks</a> section. Changed “subtractors” to “subtractors” in the Carry Logic description.
			Updated <a href="#">Clock/Control Distribution Network</a> section. Switched the “Clock Enable” and the “Reset” headings in Table 2-2, Global Buffer (GBUF) Connections to Programmable Logic Blocks.
		Pinout Information	Updated <a href="#">Pin Information Summary</a> section. Added BG121 information under iCE40HX4K and iCE40HX8K.
		Ordering Information	Updated <a href="#">iCE40 Part Number Description</a> section. Added Shipping Method and BG121 package under High Performance (HX) Devices.
			Updated <a href="#">Ordering Information</a> section. Added part numbers for BG121 under High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging.
Supplemental Information	Corrected reference to “Package Diagrams Data Sheet”.		
October 2015	3.2	Introduction	Updated Features section. Added footnote to 16 WLCSP Programmable I/O: Max Inputs (LVDS25) in Table 1-1, iCE40 Family Selection Guide.
		DC and Switching Characteristics	Updated sysCLOCK PLL Timing section. Changed $t_{DT}$ conditions. Updated Programming NVCM Supply Current – LP Devices section. Changed $I_{PP\_2V5}$ and $I_{CCIO}$ , $I_{CC\_SPI}$ units.
March 2015	3.1	DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics section. Changed LVCMOS 3.3 and LVCMOS 2.5 $V_{OH}$ Min. (V) from 0.5 to 0.4.
July 2014	3.0	DC and Switching Characteristics	Revised and/or added Typ. $V_{CC}$ data in the following sections. — Static Supply Current – LP Devices — Static Supply Current – HX Devices — Programming NVCM Supply Current – LP Devices — Programming NVCM Supply Current – HX Devices In each section table, the footnote indicating Advanced device status was removed.
		Pinout Information	Updated Pin Information Summary section. Added footnote 1 to CM49 under iCE40LP1K.
April 2014	02.9	Ordering Information	Changed “I” to “l” in part number description and ordering part numbers.
			Added part numbers to the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table.

Date	Version	Section	Change Summary
February 2014	02.8	Introduction	Updated Features section. — Corrected standby power units. — Included High Current LED Drivers
			Updated Table 1-1, iCE40 Family Selection Guide. — Removed LP384 Programmable I/O for 81 ucBGA package.
		Architecture	Updated Supported Standards section. Added information on High Current LED drivers.
		DC and Switching Characteristics	Corrected typos.
			Added footnote to the Peak Startup Supply Current – LP Devices table.
Ordering Information	Updated part number description in the Ultra Low Power (LP) Devices section.		
	Added part numbers to the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table.		
October 2013	02.7	Introduction	Updated Features list and iCE40 Family Selection Guide table.
		Architecture	Revised iCE40-1K device to iCE40LP/HX1K device.
		DC and Switching Characteristics	Added iCE40LP640 device information.
		Pinout Information	Added iCE40LP640 and iCE40LP1K information.
		Ordering Information	Added iCE40LP640 and iCE40LP1K information.
September 2013	02.6	DC and Switching Characteristics	Updated Absolute Maximum Ratings section.
			Updated sysCLOCK PLL Timing – Preliminary table.
		Pinout Information	Updated Pin Information Summary table.
August 2013	02.5	Introduction	Updated the iCE40 Family Selection Guide table.
		DC and Switching Characteristics	Updated the following tables: — Absolute Maximum Ratings — Power-On-Reset Voltage Levels — Static Supply Current – LP Devices — Static Supply Current – HX Devices — Programming NVCM Supply Current – LP Devices — Programming NVCM Supply Current – HX Devices — Peak Startup Supply Current – LP Devices — sysIO Recommended Operating Conditions — Typical Building Block Function Performance – HX Devices — iCE40 External Switching Characteristics – HX Devices — sysCLOCK PLL Timing – Preliminary — SPI Master or NVCM Configuration Time
			Pinout Information
July 2013	02.4	Introduction	Updated the iCE40 Family Selection Guide table.
		DC and Switching Characteristics	Updated the sysCONFIG Port Timing Specifications table.
			Updated footnote in DC Electrical Characteristics table.
			GDDR tables removed. Support to be provided in a technical note.
		Pinout Information	Updated the Pin Information Summary table.
Ordering Information	Updated the top-side markings figure.		
	Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table.		
May 2013	02.3	DC and Switching Characteristics	Added new data from Characterization.