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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 960 |
| Number of Logic Elements/Cells | 7680 |
| Total RAM Bits | 131072 |
| Number of I/O | 93 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 121-TFBGA |
| Supplier Device Package | 121-caBGA (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40hx8k-bg121 |

# iCE40 LP/HX Family Data Sheet Introduction

March 2017 Data Sheet DS1040

## Features

- **Flexible Logic Architecture**
  - Five devices with 384 to 7,680 LUT4s and 10 to 206 I/Os
- **Ultra Low Power Devices**
  - Advanced 40 nm low power process
  - As low as 21 µA standby power
  - Programmable low swing differential I/Os
- **Embedded and Distributed Memory**
  - Up to 128 kbits sysMEM™ Embedded Block RAM
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
- **High Current LED Drivers**
  - Three High Current Drivers used for three different LEDs or one RGB LED
- **High Performance, Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8
    - LVDS25E, subLVDS
    - Schmitt trigger inputs, to 200 mV typical hysteresis
  - Programmable pull-up mode
- **Flexible On-Chip Clocking**
  - Eight low-skew global clock resources
  - Up to two analog PLLs per device
- **Flexible Device Configuration**
  - SRAM is configured through:
    - Standard SPI Interface
    - Internal Nonvolatile Configuration Memory (NVCM)
- **Broad Range of Package Options**
  - WLCSP, QFN, VQFP, TQFP, ucBGA, caBGA, and csBGA package options
  - Small footprint package options
    - As small as 1.40 mm x 1.48 mm
  - Advanced halogen-free packaging

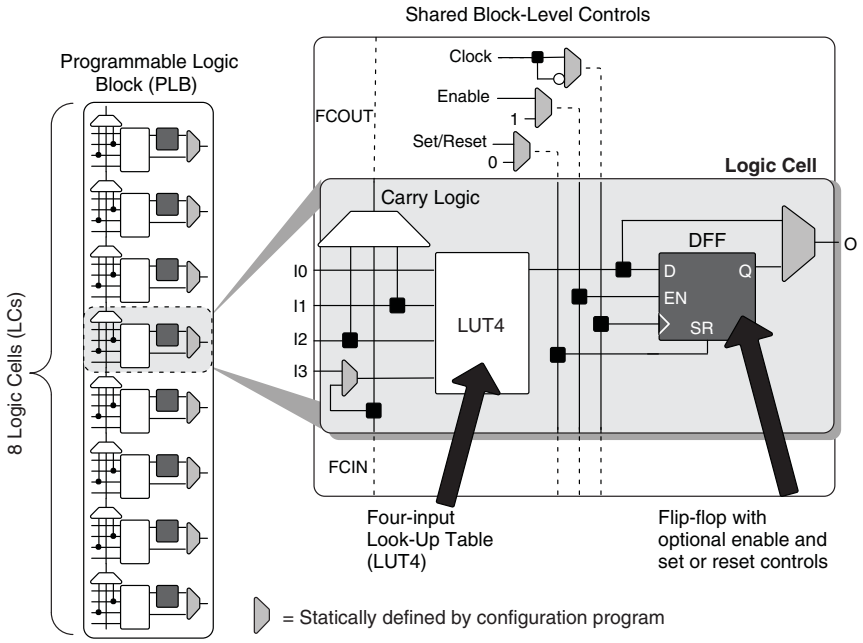
***Table 1-1. iCE40 Family Selection Guide***

| Part Number | | LP384 | LP640 | LP1K | LP4K | LP8K | HX1K | HX4K | HX8K |
|---|---|---|---|---|---|---|---|---|---|
| Logic Cells (LUT + Flip-Flop) | | 384 | 640 | 1,280 | 3,520 | 7,680 | 1,280 | 3,520 | 7,680 |
| RAM4K Memory Blocks | | 0 | 8 | 16 | 20 | 32 | 16 | 20 | 32 |
| RAM4K RAM bits | | 0 | 32K | 64K | 80K | 128K | 64K | 80K | 128K |
| Phase-Locked Loops (PLLs) | | 0 | 0 | 1[1] | 2[2] | 2[2] | 1[1] | 2 | 2 |
| Maximum Programmable I/O Pins | | 63 | 25 | 95 | 167 | 178 | 95 | 95 | 206 |
| Maximum Differential Input Pairs | | 8 | 3 | 12 | 20 | 23 | 11 | 12 | 26 |
| High Current LED Drivers | | 0 | 3 | 3 | 0 | 0 | 0 | 0 | 0 |
| **Package** | **Code** | **Programmable I/O: Max Inputs (LVDS25)** | | | | | | | |
| 16 WLCSP (1.40 mm x 1.48 mm, 0.35 mm) | SWG16 | | 10(0)[1] | 10(0)[1] | | | | | |
| 32 QFN (5 mm x 5 mm, 0.5 mm) | SG32 | 21(3) | | | | | | | |
| 36 ucBGA (2.5 mm x 2.5 mm, 0.4 mm) | CM36 | 25(3) | | 25(3)[1] | | | | | |
| 49 ucBGA (3 mm x 3 mm, 0.4 mm) | CM49 | 37(6) | | 35(5)[1] | | | | | |
| 81 ucBGA (4 mm x 4 mm, 0.4 mm) | CM81 | | | 63(8) | 63(9)[2] | 63(9)[2] | | | |
| 81 csBGA (5 mm x 5 mm, 0.5 mm) | CB81 | | | 62(9)[1] | | | | | |

## PLB Blocks

The core of the iCE40 device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

***Figure 2-2. PLB Block Diagram***




### Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT4) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT4 element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUT4s to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtractors, comparators, binary counters and some wide, cascaded logic functions.

***Table 2-1. Logic Cell Signal Descriptions***

| Function | Type | Signal Names | Description |
|---|---|---|---|
| Input | Data signal | I0, I1, I2, I3 | Inputs to LUT4 |
| Input | Control signal | Enable | Clock enable shared by all LCs in the PLB |
| Input | Control signal | Set/Reset[1] | Asynchronous or synchronous local set/reset shared by all LCs in the PLB. |
| Input | Control signal | Clock | Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB |
| Input | Inter-PLB signal | FCIN | Fast carry in |
| Output | Data signals | O | LUT4 or registered output |
| Output | Inter-PFU signal | FCOUT | Fast carry out |

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

*Table 2-3. PLL Signal Descriptions*

| Signal Name | Direction | Description |
|---|---|---|
| REFERENCECLK | Input | Input reference clock |
| BYPASS | Input | When FEEDBACK_PATH is set to SIMPLE, the BYPASS control selects which clock signal connects to the PLLOUT output.<br>0 = PLL generated signal<br>1 = REFERENCECLK |
| EXTFEEDBACK | Input | External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL. |
| DYNAMICDELAY[3:0] | Input | Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC. |
| LATCHINPUTVALUE | Input | When enabled, forces the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable. |
| PLLOUTGLOBAL | Output | Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5. |
| PLLOUTCORE | Output | Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port. |
| LOCK | Output | When High, indicates that the PLL output is phase aligned or locked to the input reference clock. |
| RESET | Input | Active low reset. |

## sysMEM Embedded Block RAM Memory

Larger iCE40 device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

### sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

*Table 2-4. sysMEM Block Configurations[1]*

| Block RAM Configuration | Block RAM Configuration and Size | WADDR Port Size (Bits) | WDATA Port Size (Bits) | RADDR Port Size (Bits) | RDATA Port Size (Bits) | MASK Port Size (Bits) |
|---|---|---|---|---|---|---|
| SB_RAM256x16<br>SB_RAM256x16NR<br>SB_RAM256x16NW<br>SB_RAM256x16NRNW | 256x16 (4K) | 8 [7:0] | 16 [15:0] | 8 [7:0] | 16 [15:0] | 16 [15:0] |
| SB_RAM512x8<br>SB_RAM512x8NR<br>SB_RAM512x8NW<br>SB_RAM512x8NRNW | 512x8 (4K) | 9 [8:0] | 8 [7:0] | 9 [8:0] | 8 [7:0] | No Mask Port |
| SB_RAM1024x4<br>SB_RAM1024x4NR<br>SB_RAM1024x4NW<br>SB_RAM1024x4NRNW | 1024x4 (4K) | 10 [9:0] | 4 [3:0] | 10 [9:0] | 4 [3:0] | No Mask Port |
| SB_RAM2048x2<br>SB_RAM2048x2NR<br>SB_RAM2048x2NW<br>SB_RAM2048x2NRNW | 2048x2 (4K) | 11 [10:0] | 2 [1:0] | 11 [10:0] | 2 [1:0] | No Mask Port |

1. For iCE40 EBR primitives with a negative-edged Read or Write clock, the base primitive name is appended with a 'N' and a 'R' or 'W' depending on the clock that is affected.

## sysIO

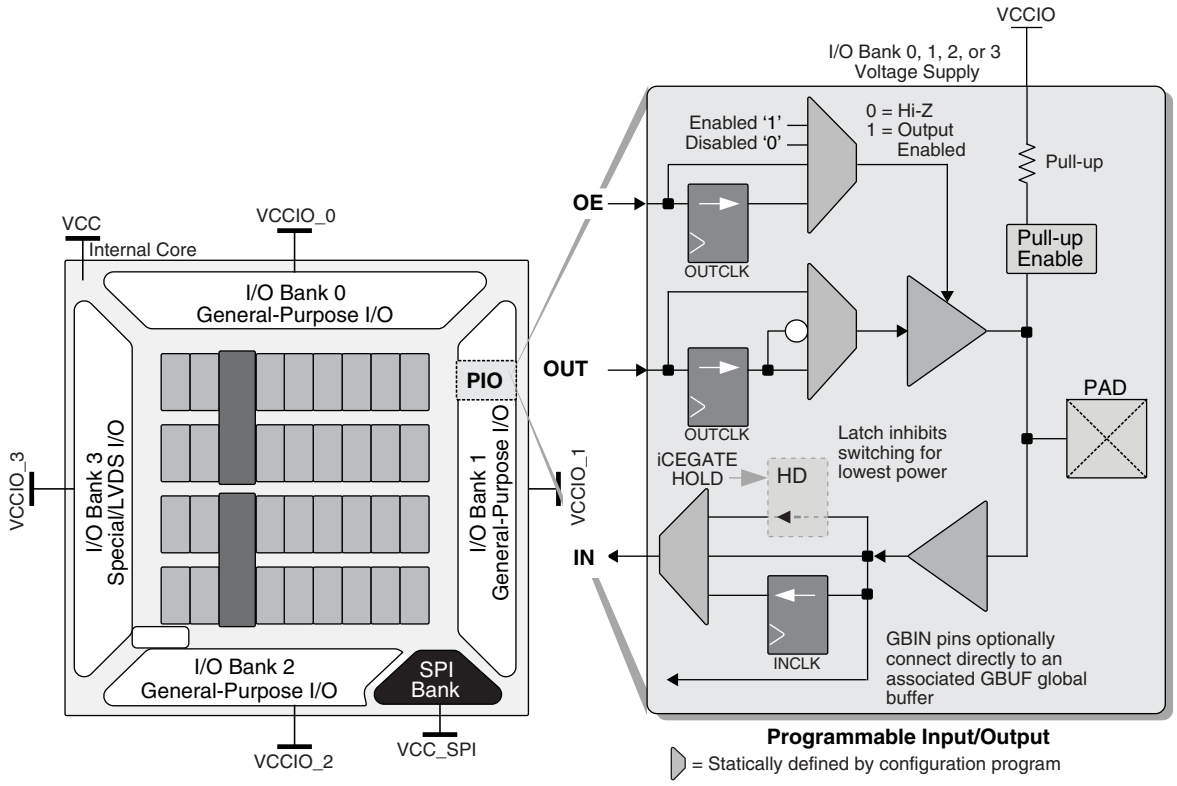
### Buffer Banks

iCE40 devices have up to four I/O banks with independent $V_{CCIO}$ rails with an additional configuration bank $V_{CC\_SPI}$ for the SPI I/Os.

### Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. The PIOs are placed on all four sides of the device.

***Figure 2-5. I/O Bank and Programmable I/O Cell***




The PIO contains three blocks: an input register block, output register block iCEgate™ and tri-state register block. To save power, the optional iCEgate™ latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

### Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock signal, creating two data streams.

### Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers. In Generic DDR mode, two registers are used to capture the data on the positive and negative edge of the system clock and then muxed creating one data stream.

Figure 2-6 shows the input/output register block for the PIOs.

*Figure 2-6. iCE I/O Register Block Diagram*

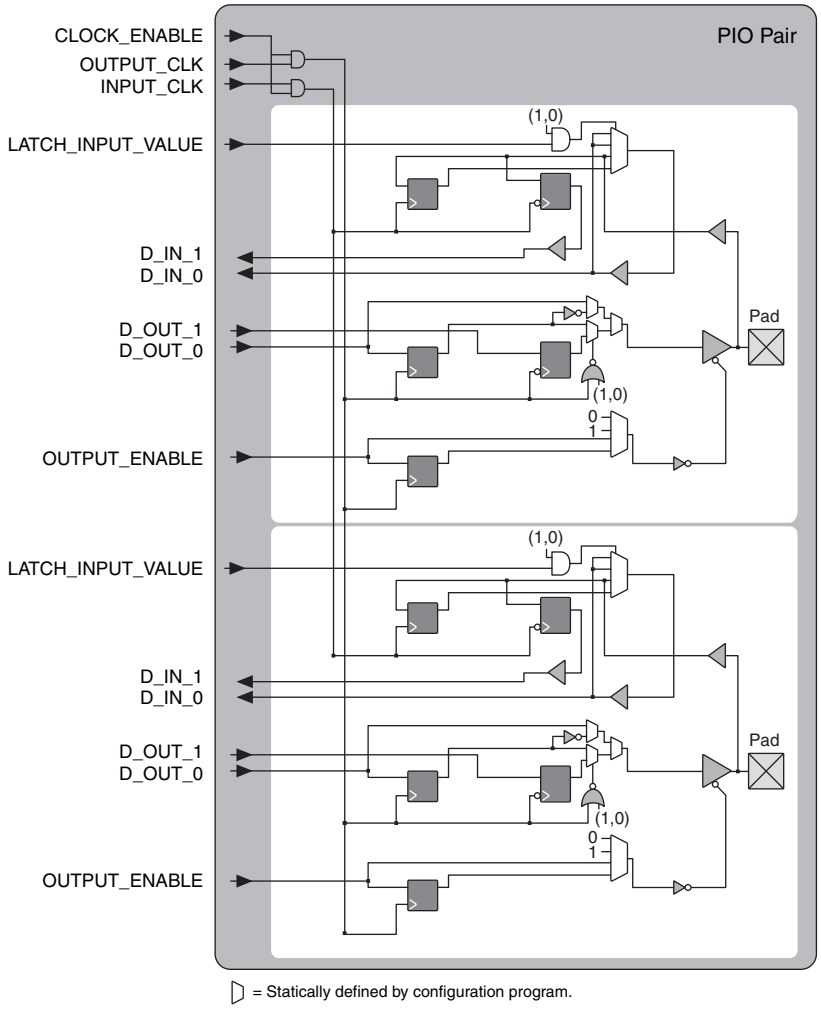



*Table 2-6. PIO Signal List*

| Pin Name | I/O Type | Description |
|---|---|---|
| OUTPUT_CLK | Input | Output register clock |
| CLOCK_ENABLE | Input | Clock enable |
| INPUT_CLK | Input | Input register clock |
| OUTPUT_ENABLE | Input | Output enable |
| D_OUT_0/1 | Input | Data from the core |
| D_IN_0/1 | Output | Data to the core |
| LATCH_INPUT_VALUE | Input | Latches/holds the Input Value |

## sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS and LVDS25.

High Current LED Drivers combine three sysIO buffers together. This allows for programmable drive strength. This also allows for high current drivers that are ideal to drive three white LEDs, or one RGB LED. Each bank is capable of supporting multiple I/O standards including single-ended LVCMOS buffers and differential LVDS25E output buf-

## Power Supply Ramp Rates[1, 2]

| Symbol | Parameter | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $t_{RAMP}$ | Power supply ramp rates for all power supplies. | All configuration modes. No power supply sequencing. | 0.40 | 10 | V/ms |
| | | Configuring from Slave SPI. No power supply sequencing, | 0.01 | 10 | V/ms |
| | | Configuring from NVCM. $V_{CC}$ and $V_{PP\_2V5}$ to be powered 0.25 ms before $V_{CC\_SPI}$. | 0.01 | 10 | V/ms |
| | | Configuring from MSPI. $V_{CC}$ and $V_{PP\_SPI}$ to be powered 0.25 ms before $V_{PP\_2V5}$. | 0.01 | 10 | V/ms |

1. Assumes monotonic ramp rates.
2. iCE40LP384 requires $V_{CC}$ to be greater than 0.7V when $V_{CCIO}$ and $V_{CC\_SPI}$ are above GND.

## Power-On-Reset Voltage Levels[1]

| Symbol | Device | Parameter | | Min. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{PORUP}$ | iCE40LP384 | Power-On-Reset ramp-up trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5) | VCC | 0.67 | 0.99 | V |
| | | | VCCIO_2 | 0.70 | 1.59 | V |
| | | | VCC_SPI | 0.70 | 1.59 | V |
| | | | VPP_2V5 | 0.70 | 1.59 | V |
| | iCE40LP640, iCE40LP/HX1K, iCE40LP/HX4K, iCE40LP/HX8K | Power-On-Reset ramp-up trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5) | VCC | 0.55 | 0.75 | V |
| | | | VCCIO_2 | 0.86 | 1.29 | V |
| | | | VCC_SPI | 0.86 | 1.29 | V |
| | | | VPP_2V5 | 0.86 | 1.33 | V |
| $V_{PORDN}$ | iCE40LP384 | Power-On-Reset ramp-down trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5) | VCC | — | 0.64 | V |
| | | | VCCIO_2 | — | 1.59 | V |
| | | | VCC_SPI | — | 1.59 | V |
| | | | VPP_2V5 | — | 1.59 | V |
| | iCE40LP640, iCE40LP/HX1K, iCE40LP/HX4K, iCE40LP/HX8K | Power-On-Reset ramp-down trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5) | VCC | — | 0.75 | V |
| | | | VCCIO_2 | — | 1.29 | V |
| | | | VCC_SPI | — | 1.29 | V |
| | | | VPP_2V5 | — | 1.33 | V |

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

## ESD Performance

Please refer to the iCE40 Product Family Qualification Summary for complete qualification data, including ESD performance.

# DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$ [1, 3, 4, 5, 6, 7] | Input or I/O Leakage | $0V < V_{IN} < V_{CCIO} + 0.2$ V | — | — | +/–10 | µA |
| $C_1$ [6, 7] | I/O Capacitance[2] | $V_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V<br>$V_{CC}$ = Typ., $V_{IO}$ = 0 to $V_{CCIO}$ + 0.2 V | — | 6 | — | pf |
| $C_2$ [6, 7] | Global Input Buffer Capacitance[2] | $V_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V<br>$V_{CC}$ = Typ., $V_{IO}$ = 0 to $V_{CCIO}$ + 0.2 V | — | 6 | — | pf |
| $V_{HYST}$ | Input Hysteresis | $V_{CCIO}$ = 1.8 V, 2.5 V, 3.3 V | — | 200 | — | mV |
| $I_{PU}$ [6, 7] | Internal PIO Pull-up Current | $V_{CCIO}$ = 1.8 V, 0=<$V_{IN}$<=0.65 $V_{CCIO}$ | –3 | — | –31 | µA |
| | | $V_{CCIO}$ = 2.5 V, 0=<$V_{IN}$<=0.65 $V_{CCIO}$ | –8 | — | –72 | µA |
| | | $V_{CCIO}$ = 3.3 V, 0=<$V_{IN}$<=0.65 $V_{CCIO}$ | –11 | — | –128 | µA |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2. $T_J$ 25°C, f = 1.0 MHz.
3. Please refer to $V_{IL}$ and $V_{IH}$ in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Only applies to IOs in the SPI bank following configuration.
5. Some products are clamped to a diode when $V_{IN}$ is larger than $V_{CCIO}$.
6. High current IOs has three sysIO buffers connected together.
7. The iCE40LP640 and iCE40LP1K SWG16 package has CDONE and a sysIO buffer are connected together.

# Static Supply Current – LP Devices[1, 2, 3, 4]

| Symbol | Parameter | Device | Typ. $V_{CC}$[4] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | iCE40LP384 | 21 | µA |
| | | iCE40LP640 | 100 | µA |
| | | iCE40LP1K | 100 | µA |
| | | iCE40LP4K | 250 | µA |
| | | iCE40LP8K | 250 | µA |
| $I_{CCPLL}$ [5, 6] | PLL Power Supply | All devices | 0.5 | µA |
| $I_{PP\_2V5}$ | NVCM Power Supply | All devices | 1.0 | µA |
| $I_{CCIO}$, $I_{CC\_SPI}$ | Bank Power Supply[4]<br>$V_{CCIO}$ = 2.5 V | All devices | 3.5 | µA |

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at $V_{CCIO}$ or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. $T_J$ = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up.
5. No PLL available on the iCE40LP384 and iCE40LP640 device.
6. $V_{CCPLL}$ is tied to $V_{CC}$ internally in packages without PLLs pins.

## Programming NVCM Supply Current – HX Devices[1, 2, 3, 4]

| Symbol | Parameter | Device | Typ. $V_{CC}$[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | iCE40HX1K | 278 | µA |
| | | iCE40HX4K | 1174 | µA |
| | | iCE40HX8K | 1174 | µA |
| $I_{CCPLL}$[6] | PLL Power Supply | All devices | 0.5 | µA |
| $I_{PP\_2V5}$ | NVCM Power Supply | All devices | 2.5 | mA |
| $I_{CCIO}$[7], $I_{CC\_SPI}$ | Bank Power Supply[5] | All devices | 3.5 | mA |

1. Assumes all inputs are held at $V_{CCIO}$ or GND and all outputs are tri-stated.
2. Typical user pattern.
3. SPI programming is at 8 MHz.
4. $T_J$ = 25 °C, power supplies at nominal voltage.
5. Per bank. $V_{CCIO}$ = 2.5 V. Does not include pull-up.
6. $V_{CCPLL}$ is tied to $V_{CC}$ internally in packages without PLLs pins.
7. $V_{PP\_FAST}$, used only for fast production programming, must be left floating or unconnected in applications.

## Peak Startup Supply Current – LP Devices

| Symbol | Parameter | Device | Max | Units |
|---|---|---|---|---|
| $I_{CCPEAK}$ | Core Power Supply | iCE40LP384 | 7.7 | mA |
| | | iCELP640 | 6.4 | mA |
| | | iCE40LP1K | 6.4 | mA |
| | | iCE40LP4K | 15.7 | mA |
| | | iCE40LP8K | 15.7 | mA |
| $I_{CCPLLPEAK}$[1, 2, 4] | PLL Power Supply | iCE40LP1K | 1.5 | mA |
| | | iCELP640 | 1.5 | mA |
| | | iCE40LP4K | 8.0 | mA |
| | | iCE40LP8K | 8.0 | mA |
| $I_{PP\_2V5PEAK}$ | NVCM Power Supply | iCE40LP384 | 3.0 | mA |
| | | iCELP640 | 7.7 | mA |
| | | iCE40LP1K | 7.7 | mA |
| | | iCE40LP4K | 4.2 | mA |
| | | iCE40LP8K | 4.2 | mA |
| $I_{PP\_FASTPEAK}$[3] | NVCM Programming Supply | iCE40LP384 | 5.7 | mA |
| | | iCELP640 | 8.1 | mA |
| | | iCE40LP1K | 8.1 | mA |
| $I_{CCIOPEAK}$[5], $I_{CC\_SPIPEAK}$ | Bank Power Supply | iCE40LP384 | 8.4 | mA |
| | | iCELP640 | 3.3 | mA |
| | | iCE40LP1K | 3.3 | mA |
| | | iCE40LP4K | 8.2 | mA |
| | | iCE40LP8K | 8.2 | mA |

1. No PLL available on the iCE40LP384 and iCE40LP640 device.
2. $V_{CCPLL}$ is tied to $V_{CC}$ internally in packages without PLLs pins.
3. $V_{PP\_FAST}$, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the $V_{PP\_FAST}$ ball connected to $V_{CCIO\_0}$ ball externally.
4. While no PLL is available in the iCE40-LP640 the $I_{CCPLLPEAK}$ is additive to $I_{CCPEAK}$.
5. iCE40LP384 requires $V_{CC}$ to be greater than 0.7 V when $V_{CCIO}$ and $V_{CC\_SPI}$ are above GND.

## Peak Startup Supply Current – HX Devices

| Symbol | Parameter | Device | Max | Units |
|---|---|---|---|---|
| $I_{CCPEAK}$ | Core Power Supply | iCE40HX1K | 6.9 | mA |
| | | iCE40HX4K | 22.3 | mA |
| | | iCE40HX8K | 22.3 | mA |
| $I_{CCPLLPEAK}$[1] | PLL Power Supply | iCE40HX1K | 1.8 | mA |
| | | iCE40HX4K | 6.4 | mA |
| | | iCE40HX8K | 6.4 | mA |
| $I_{PP\_2V5PEAK}$ | NVCM Power Supply | iCE40HX1K | 2.8 | mA |
| | | iCE40HX4K | 4.1 | mA |
| | | iCE40HX8K | 4.1 | mA |
| $I_{CCIOPEAK}$, $I_{CC\_SPIPEAK}$ | Bank Power Supply | iCE40HX1K | 6.8 | mA |
| | | iCE40HX4K | 6.8 | mA |
| | | iCE40HX8K | 6.8 | mA |

1. $V_{CCPLL}$ is tied to $V_{CC}$ internally in packages without PLLs pins.

## sysIO Recommended Operating Conditions

| Standard | $V_{CCIO}$ (V) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| LVCMOS 3.3 | 3.14 | 3.3 | 3.46 |
| LVCMOS 2.5 | 2.37 | 2.5 | 2.62 |
| LVCMOS 1.8 | 1.71 | 1.8 | 1.89 |
| LVDS25E[1, 2] | 2.37 | 2.5 | 2.62 |
| subLVDSE[1, 2] | 1.71 | 1.8 | 1.89 |

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. Does not apply to Configuration Bank $V_{CC\_SPI}$.

## sysIO Single-Ended DC Electrical Characteristics

| Input/ Output Standard | $V_{IL}$ | | $V_{IH}$[1] | | $V_{OL}$ Max. (V) | $V_{OH}$ Min. (V) | $I_{OL}$ Max. (mA) | $I_{OH}$ Max. (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min. (V) | Max. (V) | Min. (V) | Max. (V) | | | | |
| LVCMOS 3.3 | –0.3 | 0.8 | 2.0 | $V_{CCIO}$ + 0.2 V | 0.4 | $V_{CCIO}$ – 0.4 | 8, 16[2], 24[2] | –8, –16[2], –24[2] |
| | | | | | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| LVCMOS 2.5 | –0.3 | 0.7 | 1.7 | $V_{CCIO}$ + 0.2 V | 0.4 | $V_{CCIO}$ – 0.4 | 6, 12[2], 18[2] | –6, –12[2], –18[2] |
| | | | | | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| LVCMOS 1.8 | –0.3 | $0.35V_{CCIO}$ | $0.65V_{CCIO}$ | $V_{CCIO}$ + 0.2 V | 0.4 | $V_{CCIO}$ – 0.4 | 4, 8[2], 12[2] | –4, –8[2], –12[2] |
| | | | | | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |

1. Some products are clamped to a diode when $V_{IN}$ is larger than $V_{CCIO}$.
2. Only for High Drive LED outputs.

# Typical Building Block Function Performance – LP Devices[1, 2]

## Pin-to-Pin Performance (LVCMOS25)

| Function | Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit decoder | 11.0 | ns |
| 4:1 MUX | 12.0 | ns |
| 16:1 MUX | 13.0 | ns |

## Register-to-Register Performance

| Function | Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16:1 MUX | 190 | MHz |
| 16-bit adder | 160 | MHz |
| 16-bit counter | 175 | MHz |
| 64-bit counter | 65 | MHz |
| **Embedded Memory Functions** | | |
| 256x16 Pseudo-Dual Port RAM | 240 | MHz |

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a $V_{CC}$ of 1.14 V at Junction Temp 85 °C.

# Typical Building Block Function Performance – HX Devices[1, 2]

## Pin-to-Pin Performance (LVCMOS25)

| Function | Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit decoder | 10.0 | ns |
| 4:1 MUX | 9.0 | ns |
| 16:1 MUX | 9.5 | ns |

## Register-to-Register Performance

| Function | Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16:1 MUX | 305 | MHz |
| 16-bit adder | 220 | MHz |
| 16-bit counter | 255 | MHz |
| 64-bit counter | 105 | MHz |
| **Embedded Memory Functions** | | |
| 256x16 Pseudo-Dual Port RAM | 403 | MHz |

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a $V_{CC}$ of 1.14 V at Junction Temp 85 °C.

# iCE40 External Switching Characteristics – HX Devices [1, 2]

**Over Recommended Operating Conditions**

| Parameter | Description | Device | Min. | Max. | Units |
|---|---|---|---|---|---|
| **Clocks** | | | | | |
| **Primary Clocks** | | | | | |
| $f_{MAX\_GBUF}$ | Frequency for Global Buffer Clock network | All iCE40HX devices | — | 275 | MHz |
| $t_{W\_GBUF}$ | Clock Pulse Width for Global Buffer | All iCE40HX devices | 0.88 | — | ns |
| $t_{SKEW\_GBUF}$ | Global Buffer Clock Skew Within a Device | iCE40HX1K | — | 727 | ps |
| | | iCE40HX4K | — | 300 | ps |
| | | iCE40HX8K | — | 300 | ps |
| **Pin-LUT-Pin Propagation Delay** | | | | | |
| $t_{PD}$ | Best case propagation delay through one LUT-4 | All iCE40 HX devices | — | 7.30 | ns |
| **General I/O Pin Parameters (Using Global Buffer Clock without PLL)** | | | | | |
| $t_{SKEW\_IO}$ | Data bus skew across a bank of IOs | iCE40HX1K | — | 696 | ps |
| | | iCE40HX4K | — | 290 | ps |
| | | iCE40HX8K | — | 290 | ps |
| $t_{CO}$ | Clock to Output - PIO Output Register | iCE40HX1K | — | 5.00 | ns |
| | | iCE40HX4K | — | 5.41 | ns |
| | | iCE40HX8K | — | 5.41 | ns |
| $t_{SU}$ | Clock to Data Setup - PIO Input Register | iCE40HX1K | –0.23 | — | ns |
| | | iCE40HX4K | –0.43 | — | ns |
| | | iCE40HX8K | –0.43 | — | ns |
| $t_{H}$ | Clock to Data Hold - PIO Input Register | iCE40HX1K | 1.92 | — | ns |
| | | iCE40HX4K | 2.38 | — | ns |
| | | iCE40HX8K | 2.38 | — | ns |
| **General I/O Pin Parameters (Using Global Buffer Clock with PLL)[3]** | | | | | |
| $t_{COPLL}$ | Clock to Output - PIO Output Register | iCE40HX1K | — | 2.96 | ns |
| | | iCE40HX4K | — | 2.51 | ns |
| | | iCE40HX8K | — | 2.51 | ns |
| $t_{SUPLL}$ | Clock to Data Setup - PIO Input Register | iCE40HX1K | 3.10 | — | ns |
| | | iCE40HX4K | 4.16 | — | ns |
| | | iCE40HX8K | 4.16 | — | ns |
| $t_{HPLL}$ | Clock to Data Hold - PIO Input Register | iCE40HX1K | –0.60 | — | ns |
| | | iCE40HX4K | –0.53 | — | ns |
| | | iCE40HX8K | –0.53 | — | ns |

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the iCECube2 software.
2. General I/O timing numbers based on LVCMOS 2.5, 0pf load.
3. Supported on devices with a PLL.

# sysCLOCK PLL Timing

**Over Recommended Operating Conditions**

| Parameter | Descriptions | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $f_{IN}$ | Input Clock Frequency (REFERENCECLK, EXTFEEDBACK) | | 10 | 133 | MHz |
| $f_{OUT}$ | Output Clock Frequency (PLLOUT) | | 16 | 275 | MHz |
| $f_{VCO}$ | PLL VCO Frequency | | 533 | 1066 | MHz |
| $f_{PFD}$ | Phase Detector Input Frequency | | 10 | 133 | MHz |
| **AC Characteristics** | | | | | |
| $t_{DT}$ | Output Clock Duty Cycle | $f_{OUT}$ < 175 MHz | 40 | 50 | % |
| | | 175 MHz < $f_{OUT}$ < 275 MHz | 35 | 65 | "% |
| $t_{PH}$ | Output Phase Accuracy | | — | +/–12 | deg |
| $t_{OPJIT}$[1, 5] | Output Clock Period Jitter | $f_{OUT}$ <= 100 MHz | — | 450 | ps p-p |
| | | $f_{OUT}$ > 100 MHz | — | 0.05 | UIPP |
| | Output Clock Cycle-to-cycle Jitter | $f_{OUT}$ <= 100 MHz | — | 750 | ps p-p |
| | | $f_{OUT}$ > 100 MHz | — | 0.10 | UIPP |
| | Output Clock Phase Jitter | $f_{PFD}$ <= 25 MHz | — | 275 | ps p-p |
| | | $f_{PFD}$ > 25 MHz | — | 0.05 | UIPP |
| $t_W$ | Output Clock Pulse Width | At 90% or 10% | 1.3 | — | ns |
| $t_{LOCK}$[2, 3] | PLL Lock-in Time | | — | 50 | us |
| $t_{UNLOCK}$ | PLL Unlock Time | | — | 50 | ns |
| $t_{IPJIT}$[4] | Input Clock Period Jitter | $f_{PFD} \geq$ 20 MHz | — | 1000 | ps p-p |
| | | $f_{PFD}$ < 20 MHz | — | 0.02 | UIPP |
| $t_{FDTAP}$ | Fine Delay adjustment, per Tap | | 147 | 195 | ps |
| $t_{STABLE}$[3] | LATCHINPUTVALUE LOW to PLL Stable | | — | 500 | ns |
| $t_{STABLE\_PW}$[3] | LATCHINPUTVALUE Pulse Width | | — | 100 | ns |
| $t_{RST}$ | RESET Pulse Width | | 10 | — | ns |
| $t_{RSTREC}$ | RESET Recovery Time | | 10 | — | us |
| $t_{DYNAMIC\_WD}$ | DYNAMICDELAY Pulse Width | | 100 | — | VCO Cycles |
| $t_{PDBYPASS}$ | Propagation delay with the PLL in bypass mode | iCE40LP | 1.18 | 4.68 | ns |
| | | iCE40HX | 1.73 | 4.07 | ns |

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after $t_{LOCK}$ for PLL reset and dynamic delay adjustment.
3. At minimum $f_{PFD}$. As the $f_{PFD}$ increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

## Signal Descriptions

| Signal Name | I/O | Descriptions |
|---|---|---|
| **General Purpose** | | |
| IO[Bank]_[Row/Column Number][A/B] | I/O | [Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number on the device. |
| IO[Bank]_[Row/Column Number][A/B] | I/O | [Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number on the device. [A/B] indicates the differential I/O. 'A' = negative input. 'B' = positive input. |
| HCIO[Bank]_[Number] | I/O | High Current IO. [Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number. |
| NC | — | No connect |
| GND | — | GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together. |
| VCC | — | VCC – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply. |
| VCCIO_x | — | VCCIO – The power supply pins for I/O Bank x. Dedicated pins. All VCCIOs located in the same bank are tied to the same supply. |
| **PLL and Global Functions (Used as user-programmable I/O pins when not used for PLL or clock pins)** | | |
| VCCPLLx | — | PLL VCC – Power. Dedicated pins. The PLL requires a separate power and ground that is quiet and stable to reduce the output clock jitter of the PLL. |
| GNDPLLx | — | PLL GND – Ground. Dedicated pins. The sysCLOCK PLL has the DC ground connection made on the FPGA, so the external PLL ground connection (GNDPLL) must NOT be connected to the board's ground. |
| GBINx | — | Global pads. Two per side. |
| **Programming and Configuration** | | |
| CBSEL[0:1] | I/O | Dual function pins. I/Os when not used as CBSEL. Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled. |
| CRESET_B | I | Configuration Reset, active Low. Dedicated input. No internal pull-up resistor. Either actively drive externally or connect a 10 KOhm pull-up resistor to VCCIO_2. |
| CDONE | I/O | Configuration Done. Includes a permanent weak pull-up resistor to VCCIO_2. If driving external devices with CDONE output, an external pull-up resistor to VCCIO_2 may be required. Refer to the TN1248, iCE40 Programming and Configuration for more details. Following device configuration the iCE40LP640 and iCE40LP1K in the SWG16 package CDONE pin can be used as a user output. |
| VCC_SPI | — | SPI interface voltage supply input. Must have a valid voltage even if configuring from NVCM. |
| SPI_SCK | I/O | Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA configuration modes. |
| SPI_SS_B | I/O | SPI Slave Select. Active Low. Includes an internal weak pull-up resistor to VCC_SPI during configuration. During configuration, the logic level sampled on this pin determines the configuration mode used by the iCE40 device. An input when sampled at the start of configuration. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in Master SPI Flash configuration mode. |
| SPI_SI | I/O | Slave SPI serial data input and master SPI serial data output |
| SPI_SO | I/O | Slave SPI serial data output and master SPI serial data input |

## Signal Descriptions (Continued)

| Signal Name | I/O | Descriptions |
|---|---|---|
| VPP_FAST | — | Optional fast NVCM programming supply. $V_{PP\_FAST}$, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the $V_{PP\_FAST}$ ball connected to $V_{CCIO\_0}$ ball externally. |
| VPP_2V5 | — | VPP_2V5 NVCM programming and operating supply |

## Pin Information Summary (Continued)

| | iCE40LP4K | | | iCE40LP8K | | | iCE40HX1K | | |
|---|---|---|---|---|---|---|---|---|---|
| | CM81 | CM121 | CM225 | CM81 | CM121 | CM225 | VQ100 | CB132 | TQ144 |
| **General Purpose I/O per Bank** | | | | | | | | | |
| Bank 0 | 17 | 23 | 46 | 17 | 23 | 46 | 19 | 24 | 23 |
| Bank 1 | 15 | 21 | 42 | 15 | 21 | 42 | 19 | 25 | 25 |
| Bank 2 | 9 | 19 | 40 | 9 | 19 | 40 | 12 | 20 | 20 |
| Bank 3 | 18 | 26 | 46 | 18 | 26 | 46 | 18 | 22 | 24 |
| Configuration | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| Total General Purpose Single Ended I/O | 63 | 93 | 178 | 63 | 93 | 178 | 72 | 95 | 96 |
| **High Current Outputs per Bank** | | | | | | | | | |
| Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Total Differential Inputs | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Differential Inputs per Bank** | | | | | | | | | |
| Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 3 | 9 | 13 | 23 | 9 | 13 | 23 | 9 | 11 | 12 |
| Total Differential Inputs | 9 | 13 | 23 | 9 | 13 | 23 | 9 | 11 | 12 |
| **Dedicated Inputs per Bank** | | | | | | | | | |
| Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| Bank 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Bank 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Configuration | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Total Dedicated Inputs | 2 | 2 | 3 | 2 | 2 | 3 | 2 | 3 | 3 |
| **Vccio Pins** | | | | | | | | | |
| Bank 0 | 1 | 1 | 3 | 1 | 1 | 3 | 2 | 2 | 2 |
| Bank 1 | 1 | 1 | 3 | 1 | 1 | 3 | 2 | 2 | 2 |
| Bank 2 | 1 | 1 | 3 | 1 | 1 | 3 | 2 | 2 | 2 |
| Bank 3 | 1 | 2 | 4 | 1 | 2 | 4 | 3 | 3 | 2 |
| VCC | 3 | 4 | 8 | 3 | 4 | 8 | 4 | 5 | 4 |
| VCC_SPI | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| VPP_2V5 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| VPP_FAST[1] | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| VCCPLL | 1 | 2 | 2 | 1 | 2 | 2 | 0 | 1 | 1 |
| GND | 5 | 12 | 18 | 5 | 12 | 18 | 10 | 14 | 10 |
| NC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2 | 19 |
| Total Count of Bonded Pins | 81 | 121 | 225 | 81 | 121 | 225 | 100 | 132 | 144 |

1. $V_{PP\_FAST}$, used only for fast production programming, must be left floating or unconnected in applications.

## Pin Information Summary (Continued)

| | iCE40HX4K | | | iCE40HX8K | | | |
|---|---|---|---|---|---|---|---|
| | BG121 | CB132 | TQ144 | BG121 | CB132 | CM225 | CT256 |
| **General Purpose I/O per Bank** | | | | | | | |
| Bank 0 | 23 | 24 | 27 | 23 | 24 | 46 | 52 |
| Bank 1 | 21 | 25 | 29 | 21 | 25 | 42 | 52 |
| Bank 2 | 19 | 18 | 19 | 19 | 18 | 40 | 46 |
| Bank 3 | 26 | 24 | 28 | 26 | 24 | 46 | 52 |
| Configuration | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| Total General Purpose Single Ended I/O | 93 | 95 | 107 | 93 | 95 | 178 | 206 |
| **High Current Outputs per Bank** | | | | | | | |
| Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Total Differential Inputs | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Differential Inputs per Bank** | | | | | | | |
| Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 3 | 13 | 12 | 14 | 13 | 12 | 23 | 26 |
| Total Differential Inputs | 13 | 12 | 14 | 13 | 12 | 23 | 26 |
| **Dedicated Inputs per Bank** | | | | | | | |
| Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| Bank 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Bank 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Configuration | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Total Dedicated Inputs | 2 | 3 | 3 | 2 | 3 | 3 | 3 |
| **Vccio Pins** | | | | | | | |
| Bank 0 | 1 | 2 | 2 | 1 | 2 | 3 | 4 |
| Bank 1 | 1 | 2 | 2 | 1 | 2 | 3 | 4 |
| Bank 2 | 1 | 2 | 2 | 1 | 2 | 3 | 4 |
| Bank 3 | 2 | 3 | 2 | 2 | 3 | 4 | 4 |
| VCC | 4 | 5 | 4 | 4 | 5 | 8 | 6 |
| VCC_SPI | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| VPP_2V5 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| VPP_FAST[1] | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| VCCPLL | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| GND | 12 | 15 | 11 | 12 | 15 | 18 | 20 |
| NC | 0 | 0 | 6 | 0 | 0 | 0 | 0 |
| Total Count of Bonded Pins | 121 | 132 | 144 | 121 | 132 | 225 | 256 |

1. $V_{PP\_FAST}$, used only for fast production programming, must be left floating or unconnected in applications.

| Part Number | LUTs | Supply Voltage | Package | Leads | Temp. |
|---|---|---|---|---|---|
| ICE40LP8K-CM121TR1K | 7680 | 1.2 V | Halogen-Free ucBGA | 121 | IND |
| ICE40LP8K-CM225 | 7680 | 1.2 V | Halogen-Free ucBGA | 225 | IND |

## High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging

| Part Number | LUTs | Supply Voltage | Package | Leads | Temp. |
|---|---|---|---|---|---|
| ICE40HX1K-CB132 | 1280 | 1.2 V | Halogen-Free csBGA | 132 | IND |
| ICE40HX1K-VQ100 | 1280 | 1.2 V | Halogen-Free VQFP | 100 | IND |
| ICE40HX1K-TQ144 | 1280 | 1.2 V | Halogen-Free TQFP | 144 | IND |
| ICE40HX4K-BG121 | 3520 | 1.2 V | Halogen-Free caBGA | 121 | IND |
| ICE40HX4K-BG121TR | 3520 | 1.2 V | Halogen-Free caBGA | 121 | IND |
| ICE40HX4K-CB132 | 3520 | 1.2 V | Halogen-Free csBGA | 132 | IND |
| ICE40HX4K-TQ144 | 3520 | 1.2 V | Halogen-Free TQFP | 144 | IND |
| ICE40HX8K-BG121 | 7680 | 1.2 V | Halogen-Free caBGA | 121 | IND |
| ICE40HX8K-BG121TR | 7680 | 1.2 V | Halogen-Free caBGA | 121 | IND |
| ICE40HX8K-CB132 | 7680 | 1.2 V | Halogen-Free csBGA | 132 | IND |
| ICE40HX8K-CM225 | 7680 | 1.2 V | Halogen-Free ucBGA | 225 | IND |
| ICE40HX8K-CT256 | 7680 | 1.2 V | Halogen-Free caBGA | 256 | IND |

# iCE40 LP/HX Family Data Sheet Supplemental Information



## For Further Information

A variety of technical notes for the iCE40 family are available on the Lattice web site.

- TN1248, iCE40 Programming and Configuration
- TN1250, Memory Usage Guide for iCE40 Devices
- TN1251, iCE40 sysCLOCK PLL Design and Usage Guide
- TN1252, iCE40 Hardware Checklist
- TN1253, Using Differential I/O (LVDS, Sub-LVDS) in iCE40 Devices
- TN1074, PCB Layout Recommendations for BGA Packages
- iCE40 Pinout Files
- Thermal Management document
- Lattice design tools
- IBIS
- Package Diagrams Data Sheet
- Schematic Symbols

# iCE40 LP/HX Family Data Sheet Revision History

**March 2017** **Data Sheet DS1040**

| Date | Version | Section | Change Summary |
|---|---|---|---|
| March 2017 | 3.3 | Introduction | Updated Features section. Added 121-ball caBGA package for ICE40 HX4K/8K to Table 1-1, iCE40 Family Selection Guide. |
| | | Architecture | Updated PLB Blocks section. Changed “subtracters” to “subtractors” in the Carry Logic description. |
| | | | Updated Clock/Control Distribution Network section. Switched the “Clock Enable“ and the “Reset” headings in Table 2-2, Global Buffer (GBUF) Connections to Programmable Logic Blocks. |
| | | Pinout Information | Updated Pin Information Summary section. Added BG121information under iCE40HX4K and iCE40HX8K. |
| | | Ordering Information | Updated iCE40 Part Number Description section. Added Shipping Method and BG121 package under High Performance (HX) Devices. |
| | | | Updated Ordering Information section. Added part numbers for BG121 under High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging. |
| | | Supplemental Information | Corrected reference to “Package Diagrams Data Sheet”. |
| October 2015 | 3.2 | Introduction | Updated Features section. Added footnote to 16 WLCSP Programmable I/O: Max Inputs (LVDS25) in Table 1-1, iCE40 Family Selection Guide. |
| | | DC and Switching Characteristics | Updated sysCLOCK PLL Timing section. Changed $t_{DT}$ conditions. |
| | | | Updated Programming NVCM Supply Current – LP Devices section. Changed $I_{PP\_2V5}$ and $I_{CCIO}$, $I_{CC\_SPI}$ units. |
| March 2015 | 3.1 | DC and Switching Characteristics | Updated sysIO Single-Ended DC Electrical Characteristics section. Changed LVCMOS 3.3 and LVCMOS 2. 5 $V_{OH}$ Min. (V) from 0.5 to 0.4. |
| July 2014 | 3.0 | DC and Switching Characteristics | Revised and/or added Typ. $V_{CC}$ data in the following sections.<br>— Static Supply Current – LP Devices<br>— Static Supply Current – HX Devices<br>— Programming NVCM Supply Current – LP Devices<br>— Programming NVCM Supply Current – HX Devices<br>In each section table, the footnote indicating Advanced device status was removed. |
| | | Pinout Information | Updated Pin Information Summary section. Added footnote 1 to CM49 under iCE40LP1K. |
| April 2014 | 02.9 | Ordering Information | Changed “i” to “I” in part number description and ordering part numbers. |
| | | | Added part numbers to the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table. |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| February 2014 | 02.8 | Introduction | Updated Features section.<br>— Corrected standby power units.<br>— Included High Current LED Drivers |
| | | | Updated Table 1-1, iCE40 Family Selection Guide.<br>— Removed LP384 Programmable I/O for 81 ucBGA package. |
| | | Architecture | Updated Supported Standards section. Added information on High Current LED drivers. |
| | | DC and Switching Characteristics | Corrected typos. |
| | | | Added footnote to the Peak Startup Supply Current – LP Devices table. |
| | | Ordering Information | Updated part number description in the Ultra Low Power (LP) Devices section. |
| | | | Added part numbers to the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table. |
| October 2013 | 02.7 | Introduction | Updated Features list and iCE40 Family Selection Guide table. |
| | | Architecture | Revised iCE40-1K device to iCE40LP/HX1K device. |
| | | DC and Switching Characteristics | Added iCE40LP640 device information. |
| | | Pinout Information | Added iCE40LP640 and iCE40LP1K information. |
| | | Ordering Information | Added iCE40LP640 and iCE40LP1K information. |
| September 2013 | 02.6 | DC and Switching Characteristics | Updated Absolute Maximum Ratings section. |
| | | | Updated sysCLOCK PLL Timing – Preliminary table. |
| | | Pinout Information | Updated Pin Information Summary table. |
| August 2013 | 02.5 | Introduction | Updated the iCE40 Family Selection Guide table. |
| | | DC and Switching Characteristics | Updated the following tables:<br>— Absolute Maximum Ratings<br>— Power-On-Reset Voltage Levels<br>— Static Supply Current – LP Devices<br>— Static Supply Current – HX Devices<br>— Programming NVCM Supply Current – LP Devices<br>— Programming NVCM Supply Current – HX Devices<br>— Peak Startup Supply Current – LP Devices<br>— sysIO Recommended Operating Conditions<br>— Typical Building Block Function Performance – HX Devices<br>— iCE40 External Switching Characteristics – HX Devices<br>— sysCLOCK PLL Timing – Preliminary<br>— SPI Master or NVCM Configuration Time |
| | | Pinout Information | Updated the Pin Information Summary table. |
| July 2013 | 02.4 | Introduction | Updated the iCE40 Family Selection Guide table. |
| | | DC and Switching Characteristics | Updated the sysCONFIG Port Timing Specifications table. |
| | | | Updated footnote in DC Electrical Characteristics table. |
| | | | GDDR tables removed. Support to be provided in a technical note. |
| | | Pinout Information | Updated the Pin Information Summary table. |
| | | Ordering Information | Updated the top-side markings figure. |
| | | | Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table. |
| May 2013 | 02.3 | DC and Switching Characteristics | Added new data from Characterization. |