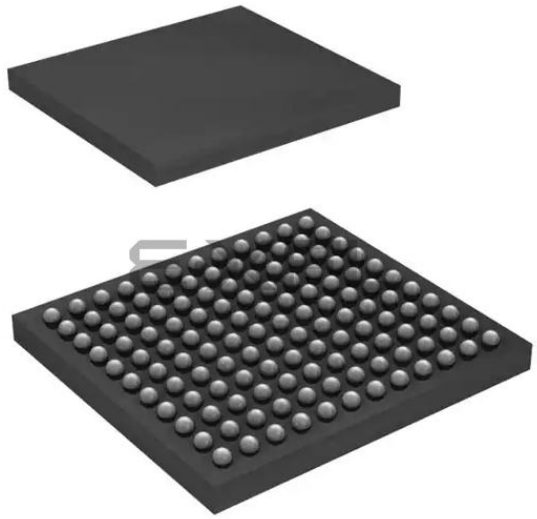
Lattice Semiconductor Corporation - ICE40HX8K-CB132 Datasheet



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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	960
Number of Logic Elements/Cells	7680
Total RAM Bits	131072
Number of I/O	95
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	132-LFBGA, CSPBGA
Supplier Device Package	132-CSBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40hx8k-cb132

iCE40 LP/HX Family Data Sheet Introduction

March 2017 Data Sheet DS1040

Features

- **Flexible Logic Architecture**
  - Five devices with 384 to 7,680 LUT4s and 10 to 206 I/Os
- **Ultra Low Power Devices**
  - Advanced 40 nm low power process
  - As low as 21 µA standby power
  - Programmable low swing differential I/Os
- **Embedded and Distributed Memory**
  - Up to 128 kbits sysMEM™ Embedded Block RAM
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
- **High Current LED Drivers**
  - Three High Current Drivers used for three different LEDs or one RGB LED
- **High Performance, Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8
    - LVDS25E, subLVDS
    - Schmitt trigger inputs, to 200 mV typical hysteresis
  - Programmable pull-up mode
- **Flexible On-Chip Clocking**
  - Eight low-skew global clock resources
  - Up to two analog PLLs per device
- **Flexible Device Configuration**
  - SRAM is configured through:
    - Standard SPI Interface
    - Internal Nonvolatile Configuration Memory (NVCM)
- **Broad Range of Package Options**
  - WLCSP, QFN, VQFP, TQFP, ucBGA, caBGA, and csBGA package options
  - Small footprint package options
    - As small as 1.40 mm x 1.48 mm
  - Advanced halogen-free packaging

Table 1-1. iCE40 Family Selection Guide

Part Number		LP384	LP640	LP1K	LP4K	LP8K	HX1K	HX4K	HX8K
Logic Cells (LUT + Flip-Flop)		384	640	1,280	3,520	7,680	1,280	3,520	7,680
RAM4K Memory Blocks		0	8	16	20	32	16	20	32
RAM4K RAM bits		0	32K	64K	80K	128K	64K	80K	128K
Phase-Locked Loops (PLLs)		0	0	1[1]	2[2]	2[2]	1[1]	2	2
Maximum Programmable I/O Pins		63	25	95	167	178	95	95	206
Maximum Differential Input Pairs		8	3	12	20	23	11	12	26
High Current LED Drivers		0	3	3	0	0	0	0	0
Package	**Code**	**Programmable I/O: Max Inputs (LVDS25)**							
16 WLCSP (1.40 mm x 1.48 mm, 0.35 mm)	SWG16		10(0)[1]	10(0)[1]					
32 QFN (5 mm x 5 mm, 0.5 mm)	SG32	21(3)							
36 ucBGA (2.5 mm x 2.5 mm, 0.4 mm)	CM36	25(3)		25(3)[1]					
49 ucBGA (3 mm x 3 mm, 0.4 mm)	CM49	37(6)		35(5)[1]					
81 ucBGA (4 mm x 4 mm, 0.4 mm)	CM81			63(8)	63(9)[2]	63(9)[2]			
81 csBGA (5 mm x 5 mm, 0.5 mm)	CB81			62(9)[1]					

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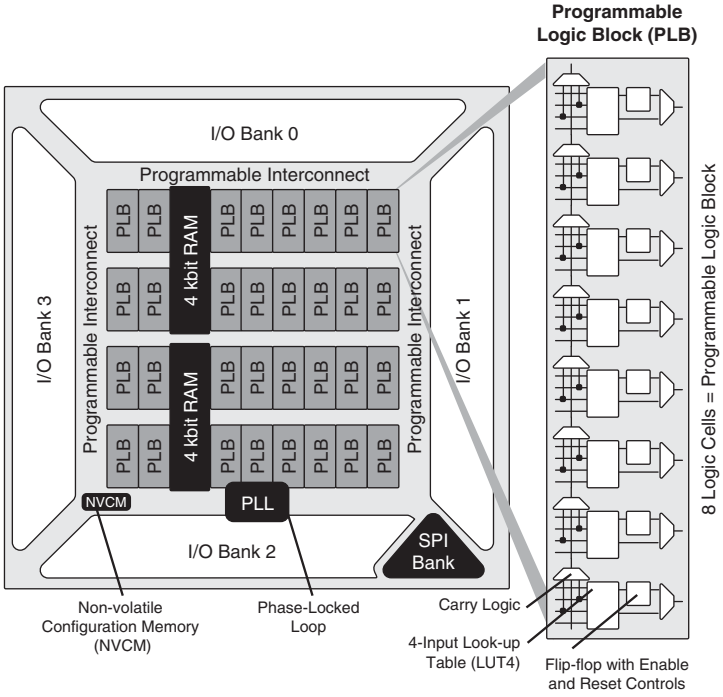
iCE40 LP/HX Family Data Sheet Architecture

March 2017 Data Sheet DS1040

Architecture Overview

The iCE40 family architecture contains an array of Programmable Logic Blocks (PLB), sysCLOCK™ PLLs, Non-volatile Programmable Configuration Memory (NVCM) and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 2-1 shows the block diagram of the iCE40LP/HX1K device.

Figure 2-1. iCE40LP/HX1K Device, Top View



The logic blocks, Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either logic blocks or EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40 family, there are up to four independent sysIO banks. Note on some packages V_{CCIO} banks are tied together. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large 4 kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO.

The iCE40 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

Every device in the family has a SPI port that supports programming and configuration of the device. The iCE40 includes on-chip, Nonvolatile Configuration Memory (NVCM).

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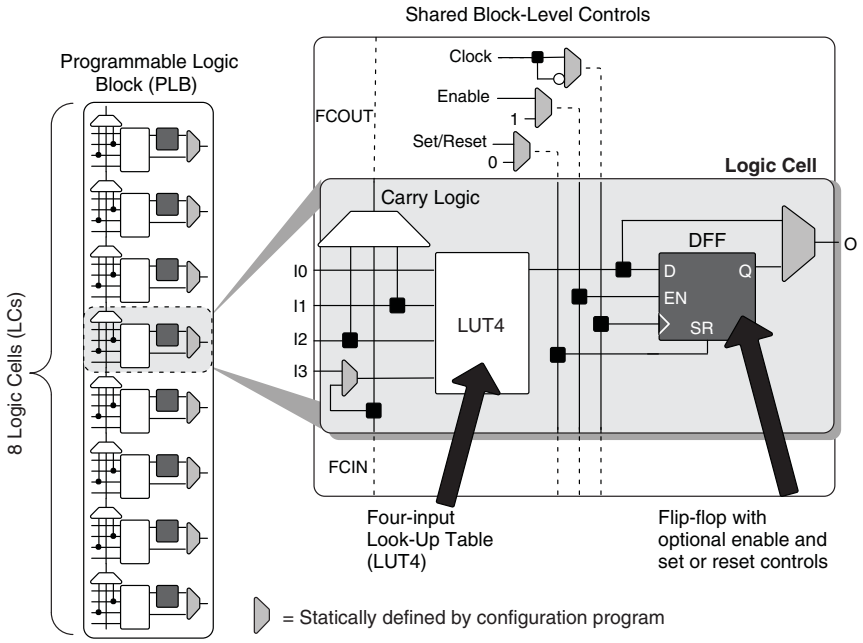
PLB Blocks

The core of the iCE40 device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

Figure 2-2. PLB Block Diagram



Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT4) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT4 element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUT4s to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtractors, comparators, binary counters and some wide, cascaded logic functions.

Table 2-1. Logic Cell Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	I0, I1, I2, I3	Inputs to LUT4
Input	Control signal	Enable	Clock enable shared by all LCs in the PLB
Input	Control signal	Set/Reset[1]	Asynchronous or synchronous local set/reset shared by all LCs in the PLB.
Input	Control signal	Clock	Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB
Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT4 or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

Table 2-3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	When FEEDBACK_PATH is set to SIMPLE, the BYPASS control selects which clock signal connects to the PLLOUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[3:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, forces the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.

sysMEM Embedded Block RAM Memory

Larger iCE40 device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

Table 2-4. sysMEM Block Configurations[1]

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4K)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4K)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4K)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4K)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40 EBR primitives with a negative-edged Read or Write clock, the base primitive name is appended with a 'N' and a 'R' or 'W' depending on the clock that is affected.

fers. Bank 3 additionally supports differential LVDS25 input buffers. Each sysIO bank has its own dedicated power supply.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, V_{CCIO_2}, V_{PP_2V5}, and V_{CC_SPI} have reached the level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to V_{CCIO}. The I/O pins will maintain the pre-configuration state until V_{CC} and V_{CCIO} (for I/O banks containing configuration I/Os) have reached levels, at which time the I/Os will take on the software user-configured settings only after a proper download/configuration. Unused IOs are automatically blocked and the pullup termination is disabled.

Supported Standards

The iCE40 sysIO buffer supports both single-ended and differential input standards. The single-ended standard supported is LVCMOS. The buffer supports the LVCMOS 1.8, 2.5, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none). The High Current output buffer have individually configurable options for drive strength.

Table 2-7 and Table 2-8 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 devices.

Table 2-7. Supported Input Standards

Input Standard	V_{CCIO} (Typical)		
	3.3 V	2.5 V	1.8 V
Single-Ended Interfaces			
LVCMOS33	Yes		
LVCMOS25		Yes	
LVCMOS18			Yes
Differential Interfaces			
LVDS25[1]		Yes	
subLVDS[1]			Yes

1. Bank 3 only.

Table 2-8. Supported Output Standards

Output Standard	V_{CCIO} (Typical)
Single-Ended Interfaces	
LVCMOS33	3.3
LVCMOS25	2.5
LVCMOS18	1.8
Differential Interfaces	
LVDS25E[1]	2.5
subLVDSE[1]	1.8

1. These interfaces can be emulated with external resistors in all devices.

Non-Volatile Configuration Memory

All iCE40 devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, please refer to TN1248, iCE40 Programming and Configuration Usage Guide.

Static Supply Current – HX Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ. V_{CC}[4]	Units
I_{CC}	Core Power Supply	iCE40HX1K	296	µA
		iCE40HX4K	1140	µA
		iCE40HX8K	1140	µA
I_{CCPLL}[5]	PLL Power Supply	All devices	0.5	µA
I_{PP_2V5}	NVCM Power Supply	All devices	1.0	µA
I_{CCIO}, I_{CC_SPI}	Bank Power Supply[4] V_{CCIO} = 2.5 V	All devices	3.5	µA

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. T_J = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up.
5. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.

Programming NVCM Supply Current – LP Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ. V_{CC}[5]	Units
I_{CC}	Core Power Supply	iCE40LP384	60	µA
		iCE40LP640	120	µA
		iCE40LP1K	120	µA
		iCE40LP4K	350	µA
		iCE40LP8K	350	µA
I_{CCPLL}[6, 7]	PLL Power Supply	All devices	0.5	µA
I_{PP_2V5}	NVCM Power Supply	All devices	2.5	mA
I_{CCIO}[8], I_{CC_SPI}	Bank Power Supply[5]	All devices	3.5	mA

1. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
2. Typical user pattern.
3. SPI programming is at 8 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up.
6. No PLL available on the iCE40-LP384 and iCE40-LP640 device.
7. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.
8. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the V_{PP_FAST} ball connected to V_{CCIO_0} ball externally.

Peak Startup Supply Current – HX Devices

Symbol	Parameter	Device	Max	Units
I_{CCPEAK}	Core Power Supply	iCE40HX1K	6.9	mA
		iCE40HX4K	22.3	mA
		iCE40HX8K	22.3	mA
$I_{CCPLLPEAK}$[1]	PLL Power Supply	iCE40HX1K	1.8	mA
		iCE40HX4K	6.4	mA
		iCE40HX8K	6.4	mA
$I_{PP_2V5PEAK}$	NVCM Power Supply	iCE40HX1K	2.8	mA
		iCE40HX4K	4.1	mA
		iCE40HX8K	4.1	mA
$I_{CCIOPEAK}$, $I_{CC_SPIPEAK}$	Bank Power Supply	iCE40HX1K	6.8	mA
		iCE40HX4K	6.8	mA
		iCE40HX8K	6.8	mA

1. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.

sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)		
	Min.	Typ.	Max.
LVCMOS 3.3	3.14	3.3	3.46
LVCMOS 2.5	2.37	2.5	2.62
LVCMOS 1.8	1.71	1.8	1.89
LVDS25E[1, 2]	2.37	2.5	2.62
subLVDSE[1, 2]	1.71	1.8	1.89

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. Does not apply to Configuration Bank V_{CC_SPI}.

sysIO Single-Ended DC Electrical Characteristics

Input/ Output Standard	V_{IL}		V_{IH}[1]		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max. (mA)	I_{OH} Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	–0.3	0.8	2.0	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	8, 16[2], 24[2]	–8, –16[2], –24[2]
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	6, 12[2], 18[2]	–6, –12[2], –18[2]
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	4, 8[2], 12[2]	–4, –8[2], –12[2]
					0.2	V_{CCIO} – 0.2	0.1	–0.1

1. Some products are clamped to a diode when V_{IN} is larger than V_{CCIO}.
2. Only for High Drive LED outputs.

sysIO Differential Electrical Characteristics

The LVDS25E/subLVDSE differential output buffers are available on all banks but the LVDS/subLVDS input buffers are only available on Bank 3 of iCE40 devices.

LVDS25

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage	V_{CCIO}[1] = 2.5	0	—	2.5	V
V_{THD}	Differential Input Threshold		250	350	450	mV
V_{CM}	Input Common Mode Voltage	V_{CCIO}[1] = 2.5	(V_{CCIO}/2) - 0.3	V_{CCIO}/2	(V_{CCIO}/2) + 0.3	V
I_{IN}	Input Current	Power on	—	—	±10	µA

1. Typical.

subLVDS

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage	V_{CCIO}[1] = 1.8	0	—	1.8	V
V_{THD}	Differential Input Threshold		100	150	200	mV
V_{CM}	Input Common Mode Voltage	V_{CCIO}[1] = 1.8	(V_{CCIO}/2) - 0.25	V_{CCIO}/2	(V_{CCIO}/2) + 0.25	V
I_{IN}	Input Current	Power on	—	—	±10	µA

1. Typical.

LVDS25E Emulation

iCE40 devices can support LVDSE outputs via emulation on all banks. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS25E standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

Figure 3-1. LVDS25E Using External Resistors

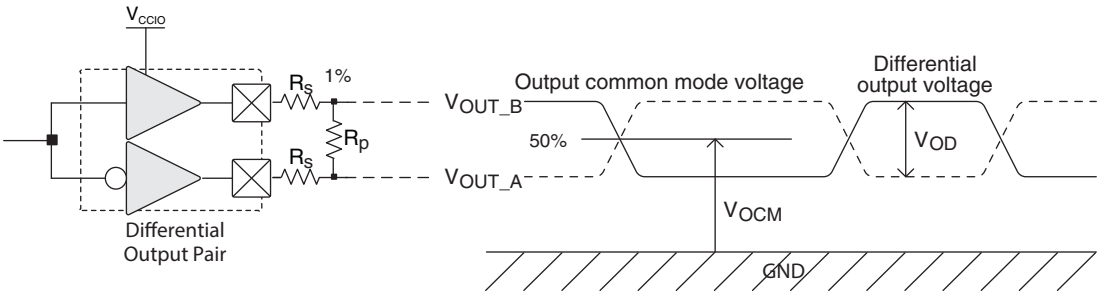


Table 3-1. LVDS25E DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	150	Ohms
R_P	Driver parallel resistor	140	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.30	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	6.03	mA

SubLVDS Emulation

The iCE40 family supports the differential subLVDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all banks of the devices. The subLVDS input standard is supported by the LVDS25 differential input buffer. The scheme shown in Figure 3-2 is one possible solution for subLVDSE output standard implementation. Use LVDS25E mode with suggested resistors for subLVDSE operation. Resistor values in Figure 3-2 are industry standard values for 1% resistors.

Figure 3-2. subLVDSE

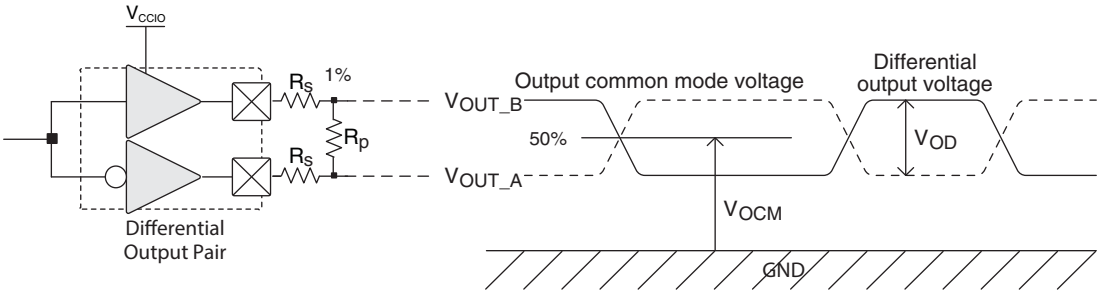


Table 3-2. subLVDSE DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	270	Ohms
R_P	Driver parallel resistor	120	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	0.9	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	2.8	mA