Lattice Semiconductor Corporation - ICE40LP1K-CM121 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	95
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	121-VFBGA, CSBGA
Supplier Device Package	121-UCBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lp1k-cm121

iCE40 LP/HX Family Data Sheet Introduction

March 2017 Data Sheet DS1040

Features

- **Flexible Logic Architecture**
  - Five devices with 384 to 7,680 LUT4s and 10 to 206 I/Os
- **Ultra Low Power Devices**
  - Advanced 40 nm low power process
  - As low as 21 µA standby power
  - Programmable low swing differential I/Os
- **Embedded and Distributed Memory**
  - Up to 128 kbits sysMEM™ Embedded Block RAM
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
- **High Current LED Drivers**
  - Three High Current Drivers used for three different LEDs or one RGB LED
- **High Performance, Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8
    - LVDS25E, subLVDS
    - Schmitt trigger inputs, to 200 mV typical hysteresis
  - Programmable pull-up mode
- **Flexible On-Chip Clocking**
  - Eight low-skew global clock resources
  - Up to two analog PLLs per device
- **Flexible Device Configuration**
  - SRAM is configured through:
    - Standard SPI Interface
    - Internal Nonvolatile Configuration Memory (NVCM)
- **Broad Range of Package Options**
  - WLCSP, QFN, VQFP, TQFP, ucBGA, caBGA, and csBGA package options
  - Small footprint package options
    - As small as 1.40 mm x 1.48 mm
  - Advanced halogen-free packaging

Table 1-1. iCE40 Family Selection Guide

Part Number		LP384	LP640	LP1K	LP4K	LP8K	HX1K	HX4K	HX8K
Logic Cells (LUT + Flip-Flop)		384	640	1,280	3,520	7,680	1,280	3,520	7,680
RAM4K Memory Blocks		0	8	16	20	32	16	20	32
RAM4K RAM bits		0	32K	64K	80K	128K	64K	80K	128K
Phase-Locked Loops (PLLs)		0	0	1[1]	2[2]	2[2]	1[1]	2	2
Maximum Programmable I/O Pins		63	25	95	167	178	95	95	206
Maximum Differential Input Pairs		8	3	12	20	23	11	12	26
High Current LED Drivers		0	3	3	0	0	0	0	0
Package	**Code**	**Programmable I/O: Max Inputs (LVDS25)**							
16 WLCSP (1.40 mm x 1.48 mm, 0.35 mm)	SWG16		10(0)[1]	10(0)[1]					
32 QFN (5 mm x 5 mm, 0.5 mm)	SG32	21(3)							
36 ucBGA (2.5 mm x 2.5 mm, 0.4 mm)	CM36	25(3)		25(3)[1]					
49 ucBGA (3 mm x 3 mm, 0.4 mm)	CM49	37(6)		35(5)[1]					
81 ucBGA (4 mm x 4 mm, 0.4 mm)	CM81			63(8)	63(9)[2]	63(9)[2]			
81 csBGA (5 mm x 5 mm, 0.5 mm)	CB81			62(9)[1]					

Table 1-1. iCE40 Family Selection Guide (continued)

84 QFN (7 mm x 7 mm, 0.5 mm)	QN84			67(7)[1]					
100 VQFP (14 mm x 14 mm, 0.5 mm)	VQ100						72(9)[1]		
121 ucBGA (5 mm x 5 mm, 0.4 mm)	CM121			95(12)	93(13)	93(13)			
121 csBGA (6 mm x 6 mm, 0.5 mm)	CB121			92(12)					
121 caBGA (9 mm x 9 mm, 0.8 mm)	BG121							93(13)	93(13)
132 csBGA (8 mm x 8 mm, 0.5 mm)	CB132						95(11)	95(12)	95(12)
144 TQFP (20 mm x 20 mm, 0.5 mm)	TQ144						96(12)	107(14)	
225 ucBGA (7 mm x 7 mm, 0.4 mm)	CM225				178(23)	178(23)			178(23)
256-ball caBGA (14 mm x 14 mm, 0.8 mm)	CT256								206(26)

1. No PLL available on the 16 WLCSP, 36 ucBGA, 81 csBGA, 84 QFN and 100 VQFP packages.
2. Only one PLL available on the 81 ucBGA package.
3. High Current I/Os only available on the 16 WLCSP package.

Introduction

The iCE40 family of ultra-low power, non-volatile FPGAs has five devices with densities ranging from 384 to 7680 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic, these devices feature Embedded Block RAM (EBR), Non-volatile Configuration Memory (NVCM) and Phase Locked Loops (PLLs). These features allow the devices to be used in low-cost, high-volume consumer and system applications. Select packages offer High-Current drivers that are ideal to drive three white LEDs, or one RGB LED.

The iCE40 devices are fabricated on a 40 nm CMOS low power process. The device architecture has several features such as programmable low-swing differential I/Os and the ability to turn off on-chip PLLs dynamically. These features help manage static and dynamic power consumption, resulting in low static power for all members of the family. The iCE40 devices are available in two versions – ultra low power (LP) and high performance (HX) devices.

The iCE40 FPGAs are available in a broad range of advanced halogen-free packages ranging from the space saving 1.40x1.48 mm WLCSP to the PCB-friendly 20x20 mm TQFP. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The iCE40 devices offer enhanced I/O features such as pull-up resistors. Pull-up features are controllable on a “per-pin” basis.

The iCE40 devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash or be configured by an external master such as a CPU.

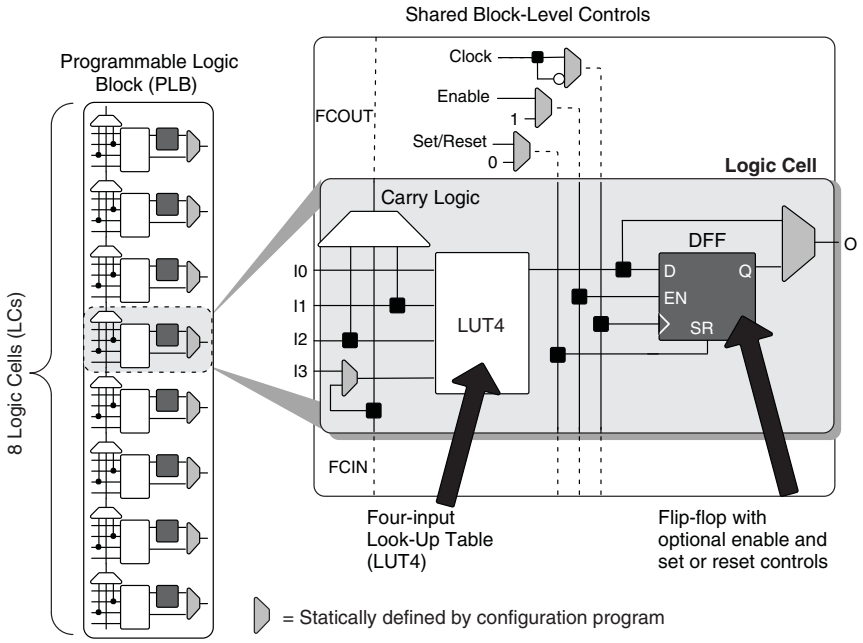
Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 family of devices. Popular logic synthesis tools provide synthesis library support for iCE40. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40 FPGA family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

PLB Blocks

The core of the iCE40 device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

Figure 2-2. PLB Block Diagram



Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT4) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT4 element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUT4s to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtractors, comparators, binary counters and some wide, cascaded logic functions.

Table 2-1. Logic Cell Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	I0, I1, I2, I3	Inputs to LUT4
Input	Control signal	Enable	Clock enable shared by all LCs in the PLB
Input	Control signal	Set/Reset[1]	Asynchronous or synchronous local set/reset shared by all LCs in the PLB.
Input	Control signal	Clock	Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB
Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT4 or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

Table 2-3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	When FEEDBACK_PATH is set to SIMPLE, the BYPASS control selects which clock signal connects to the PLLOUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[3:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, forces the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.

sysMEM Embedded Block RAM Memory

Larger iCE40 device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

Table 2-4. sysMEM Block Configurations[1]

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4K)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4K)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4K)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4K)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40 EBR primitives with a negative-edged Read or Write clock, the base primitive name is appended with a 'N' and a 'R' or 'W' depending on the clock that is affected.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Note the sysMEM Embedded Block RAM Memory address 0 cannot be initialized.

Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

RAM4k Block

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

Figure 2-4. sysMEM Memory Primitives

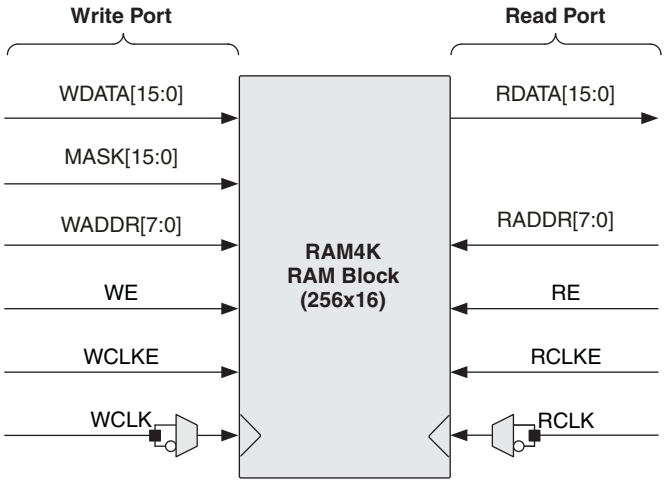


Table 2-5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = write bit; 1 = don't write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

For further information on the sysMEM EBR block, please refer to TN1250, Memory Usage Guide for iCE40 Devices.

Power Supply Ramp Rates[1, 2]

Symbol	Parameter		Min.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	All configuration modes. No power supply sequencing.	0.40	10	V/ms
		Configuring from Slave SPI. No power supply sequencing,	0.01	10	V/ms
		Configuring from NVCM. V_{CC} and V_{PP_2V5} to be powered 0.25 ms before V_{CC_SPI}.	0.01	10	V/ms
		Configuring from MSPI. V_{CC} and V_{PP_SPI} to be powered 0.25 ms before V_{PP_2V5}.	0.01	10	V/ms

1. Assumes monotonic ramp rates.
2. iCE40LP384 requires V_{CC} to be greater than 0.7V when V_{CCIO} and V_{CC_SPI} are above GND.

Power-On-Reset Voltage Levels[1]

Symbol	Device	Parameter		Min.	Max.	Units
V_{PORUP}	iCE40LP384	Power-On-Reset ramp-up trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5)	VCC	0.67	0.99	V
			VCCIO_2	0.70	1.59	V
			VCC_SPI	0.70	1.59	V
			VPP_2V5	0.70	1.59	V
	iCE40LP640, iCE40LP/HX1K, iCE40LP/HX4K, iCE40LP/HX8K	Power-On-Reset ramp-up trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5)	VCC	0.55	0.75	V
			VCCIO_2	0.86	1.29	V
			VCC_SPI	0.86	1.29	V
			VPP_2V5	0.86	1.33	V
V_{PORDN}	iCE40LP384	Power-On-Reset ramp-down trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5)	VCC	—	0.64	V
			VCCIO_2	—	1.59	V
			VCC_SPI	—	1.59	V
			VPP_2V5	—	1.59	V
	iCE40LP640, iCE40LP/HX1K, iCE40LP/HX4K, iCE40LP/HX8K	Power-On-Reset ramp-down trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5)	VCC	—	0.75	V
			VCCIO_2	—	1.29	V
			VCC_SPI	—	1.29	V
			VPP_2V5	—	1.33	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

ESD Performance

Please refer to the iCE40 Product Family Qualification Summary for complete qualification data, including ESD performance.

sysIO Differential Electrical Characteristics

The LVDS25E/subLVDSE differential output buffers are available on all banks but the LVDS/subLVDS input buffers are only available on Bank 3 of iCE40 devices.

LVDS25

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage	V_{CCIO}[1] = 2.5	0	—	2.5	V
V_{THD}	Differential Input Threshold		250	350	450	mV
V_{CM}	Input Common Mode Voltage	V_{CCIO}[1] = 2.5	(V_{CCIO}/2) - 0.3	V_{CCIO}/2	(V_{CCIO}/2) + 0.3	V
I_{IN}	Input Current	Power on	—	—	±10	µA

1. Typical.

subLVDS

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage	V_{CCIO}[1] = 1.8	0	—	1.8	V
V_{THD}	Differential Input Threshold		100	150	200	mV
V_{CM}	Input Common Mode Voltage	V_{CCIO}[1] = 1.8	(V_{CCIO}/2) - 0.25	V_{CCIO}/2	(V_{CCIO}/2) + 0.25	V
I_{IN}	Input Current	Power on	—	—	±10	µA

1. Typical.

Typical Building Block Function Performance – LP Devices[1, 2]

Pin-to-Pin Performance (LVCMOS25)

Function	Timing	Units
Basic Functions		
16-bit decoder	11.0	ns
4:1 MUX	12.0	ns
16:1 MUX	13.0	ns

Register-to-Register Performance

Function	Timing	Units
Basic Functions		
16:1 MUX	190	MHz
16-bit adder	160	MHz
16-bit counter	175	MHz
64-bit counter	65	MHz
Embedded Memory Functions		
256x16 Pseudo-Dual Port RAM	240	MHz

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a V_{CC} of 1.14 V at Junction Temp 85 °C.

Typical Building Block Function Performance – HX Devices[1, 2]

Pin-to-Pin Performance (LVCMOS25)

Function	Timing	Units
Basic Functions		
16-bit decoder	10.0	ns
4:1 MUX	9.0	ns
16:1 MUX	9.5	ns

Register-to-Register Performance

Function	Timing	Units
Basic Functions		
16:1 MUX	305	MHz
16-bit adder	220	MHz
16-bit counter	255	MHz
64-bit counter	105	MHz
Embedded Memory Functions		
256x16 Pseudo-Dual Port RAM	403	MHz

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a V_{CC} of 1.14 V at Junction Temp 85 °C.

iCE40 External Switching Characteristics – LP Devices [1, 2]

Over Recommended Operating Conditions

Parameter	Description	Device	Min.	Max.	Units
Clocks					
Global Clocks					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All iCE40LP devices	—	275	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All iCE40LP devices	0.92	—	ns
t_{SKEW_GBUF}	Global Buffer Clock Skew Within a Device	iCE40LP384	—	370	ps
		iCE40LP640	—	230	ps
		iCE40LP1K	—	230	ps
		iCE40LP4K	—	340	ps
		iCE40LP8K	—	340	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT-4	All iCE40LP devices	—	9.36	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)[3]					
t_{SKEW_IO}	Data bus skew across a bank of IOs	iCE40LP384	—	300	ps
		iCE40LP640	—	200	ps
		iCE40LP1K	—	200	ps
		iCE40LP4K	—	280	ps
		iCE40LP8K	—	280	ps
t_{CO}	Clock to Output - PIO Output Register	iCE40LP384	—	6.33	ns
		iCE40LP640	—	5.91	ns
		iCE40LP1K	—	5.91	ns
		iCE40LP4K	—	6.58	ns
		iCE40LP8K	—	6.58	ns
t_{SU}	Clock to Data Setup - PIO Input Register	iCE40LP384	–0.08	—	ns
		iCE40LP640	–0.33	—	ns
		iCE40LP1K	–0.33	—	ns
		iCE40LP4K	–0.63	—	ns
		iCE40LP8K	–0.63	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	iCE40LP384	1.99	—	ns
		iCE40LP640	2.81	—	ns
		iCE40LP1K	2.81	—	ns
		iCE40LP4K	3.48	—	ns
		iCE40LP8K	3.48	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL)[3]					
t_{COPLL}	Clock to Output - PIO Output Register	iCE40LP1K	—	2.20	ns
		iCE40LP4K	—	2.30	ns
		iCE40LP8K	—	2.30	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	iCE40LP1K	5.23	—	ns
		iCE40LP4K	6.13	—	ns
		iCE40LP8K	6.13	—	ns

iCE40 External Switching Characteristics – HX Devices [1, 2]

Over Recommended Operating Conditions

Parameter	Description	Device	Min.	Max.	Units
Clocks					
Primary Clocks					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All iCE40HX devices	—	275	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All iCE40HX devices	0.88	—	ns
t_{SKEW_GBUF}	Global Buffer Clock Skew Within a Device	iCE40HX1K	—	727	ps
		iCE40HX4K	—	300	ps
		iCE40HX8K	—	300	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT-4	All iCE40 HX devices	—	7.30	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)					
t_{SKEW_IO}	Data bus skew across a bank of IOs	iCE40HX1K	—	696	ps
		iCE40HX4K	—	290	ps
		iCE40HX8K	—	290	ps
t_{CO}	Clock to Output - PIO Output Register	iCE40HX1K	—	5.00	ns
		iCE40HX4K	—	5.41	ns
		iCE40HX8K	—	5.41	ns
t_{SU}	Clock to Data Setup - PIO Input Register	iCE40HX1K	–0.23	—	ns
		iCE40HX4K	–0.43	—	ns
		iCE40HX8K	–0.43	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	iCE40HX1K	1.92	—	ns
		iCE40HX4K	2.38	—	ns
		iCE40HX8K	2.38	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL)[3]					
t_{COPLL}	Clock to Output - PIO Output Register	iCE40HX1K	—	2.96	ns
		iCE40HX4K	—	2.51	ns
		iCE40HX8K	—	2.51	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	iCE40HX1K	3.10	—	ns
		iCE40HX4K	4.16	—	ns
		iCE40HX8K	4.16	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	iCE40HX1K	–0.60	—	ns
		iCE40HX4K	–0.53	—	ns
		iCE40HX8K	–0.53	—	ns

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the iCECube2 software.
2. General I/O timing numbers based on LVCMOS 2.5, 0pf load.
3. Supported on devices with a PLL.

SPI Master or NVCM Configuration Time[1, 2]

Symbol	Parameter	Conditions	Typ.	Units
t_{CONFIG}	POR/CRESET_B to Device I/O Active	iCE40LP384 - Low Frequency (Default)	25	ms
		iCE40LP384 - Medium Frequency	15	ms
		iCE40LP384 - High Frequency	11	ms
		iCE40LP640 - Low Frequency (Default)	53	ms
		iCE40LP640 - Medium Frequency	25	ms
		iCE40LP640 - High Frequency	13	ms
		iCE40LP/HX1K - Low Frequency (Default)	53	ms
		iCE40LP/HX1K - Medium Frequency	25	ms
		iCE40LP/HX1K - High Frequency	13	ms
		iCE40LP/HX4K - Low Frequency (Default)	230	ms
		iCE40LP/HX4K - Medium Frequency	110	ms
		iCE40LP/HX4K - High Frequency	70	ms
		iCE40LP/HX8K - Low Frequency (Default)	230	ms
		iCE40LP/HX8K - Medium Frequency	110	ms
		iCE40LP/HX8K - High Frequency	70	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

Signal Descriptions (Continued)

Signal Name	I/O	Descriptions
VPP_FAST	—	Optional fast NVCM programming supply. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the V_{PP_FAST} ball connected to V_{CCIO_0} ball externally.
VPP_2V5	—	VPP_2V5 NVCM programming and operating supply

Pin Information Summary

	iCE40LP384			iCE40LP640	iCE40LP1K							
	SG32	CM36[2]	CM49[2]	SWG16	SWG16	CM36[1, 2]	CM49[1, 2]	CM81	CB81	QN84	CM121	CB121
General Purpose I/O per Bank												
Bank 0	6	4	10	3	3	4	10	17	17	17	24	24
Bank 1	5	7	7	0	0	7	7	15	16	17	25	21
Bank 2	0	4	4	1	1	4	4	11	8	11	18	19
Bank 3	6	6	12	2	2	6	10	16	17	18	24	24
Configuration	4	4	4	4	4	4	4	4	4	4	4	4
Total General Purpose Single Ended I/O	21	25	37	10	10	25	35	63	62	67	95	92
High Current Outputs per Bank												
Bank 0	0	0	0	3	3	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0	0	0	0
Bank 3	0	0	0	0	0	0	0	0	0	0	0	0
Total Current Outputs	0	0	0	3	3	0	0	0	0	0	0	0
Differential Inputs per Bank												
Bank 0	0	0	0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0	0	0	0
Bank 3	3	3	6	1	1	3	5	8	9	7	12	12
Total Differential Inputs	3	3	6	1	1	3	5	8	9	7	12	12
Dedicated Inputs per Bank												
Bank 0	0	0	0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0	0	0	0
Bank 2	2	2	2	1	1	2	2	2	2	2	2	2
Bank 3	0	0	0	0	0	0	0	0	0	0	0	0
Configuration	0	0	0	0	0	0	0	0	0	0	0	0
Total Dedicated Inputs	2	2	2	1	1	2	2	2	2	2	2	2
Vccio Pins												
Bank 0	1	1	1	1	1	1	1	1	1	1	2	1
Bank 1	1	1	1	0	0	0	0	1	1	1	2	1
Bank 2	1	1	1	1	1	1	1	1	1	1	2	1
Bank 3	1	0	0	0	0	0	0	1	1	1	2	2
VCC	1	1	2	1	1	1	2	3	3	4	4	4
VCC_SPI	1	1	1	0	0	1	1	1	1	1	1	1
VPP_2V5	1	1	1	0	0	1	1	1	1	1	1	1
VPP_FAST[3]	0	0	0	0	0	1	1	1	0	1	1	1
VCCPLL	0	0	0	0	0	0	1	1	0	0	1	1
GND	2	3	3	2	2	3	4	5	8	4	8	11
NC	0	0	0	0	0	0	0	0	0	0	0	3
Total Count of Bonded Pins	32	36	49	16	16	36	49	81	81	84	121	121

1. V_{CCIO0} and V_{CCIO1} are connected together.
2. V_{CCIO2} and V_{CCIO3} are connected together.
3. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the V_{PP_FAST} ball connected to V_{CCIO_0} ball externally.

Pin Information Summary (Continued)

	iCE40LP4K			iCE40LP8K			iCE40HX1K		
	CM81	CM121	CM225	CM81	CM121	CM225	VQ100	CB132	TQ144
General Purpose I/O per Bank									
Bank 0	17	23	46	17	23	46	19	24	23
Bank 1	15	21	42	15	21	42	19	25	25
Bank 2	9	19	40	9	19	40	12	20	20
Bank 3	18	26	46	18	26	46	18	22	24
Configuration	4	4	4	4	4	4	4	4	4
Total General Purpose Single Ended I/O	63	93	178	63	93	178	72	95	96
High Current Outputs per Bank									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0
Bank 3	0	0	0	0	0	0	0	0	0
Total Differential Inputs	0	0	0	0	0	0	0	0	0
Differential Inputs per Bank									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0
Bank 3	9	13	23	9	13	23	9	11	12
Total Differential Inputs	9	13	23	9	13	23	9	11	12
Dedicated Inputs per Bank									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	1	0	0	1	0	1	1
Bank 2	2	2	2	2	2	2	2	2	2
Bank 3	0	0	0	0	0	0	0	0	0
Configuration	0	0	0	0	0	0	0	0	0
Total Dedicated Inputs	2	2	3	2	2	3	2	3	3
Vccio Pins									
Bank 0	1	1	3	1	1	3	2	2	2
Bank 1	1	1	3	1	1	3	2	2	2
Bank 2	1	1	3	1	1	3	2	2	2
Bank 3	1	2	4	1	2	4	3	3	2
VCC	3	4	8	3	4	8	4	5	4
VCC_SPI	1	1	1	1	1	1	1	1	1
VPP_2V5	1	1	1	1	1	1	1	1	1
VPP_FAST[1]	1	1	1	1	1	1	1	1	1
VCCPLL	1	2	2	1	2	2	0	1	1
GND	5	12	18	5	12	18	10	14	10
NC	0	0	0	0	0	0	0	2	19
Total Count of Bonded Pins	81	121	225	81	121	225	100	132	144

1. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications.

Pin Information Summary (Continued)

	iCE40HX4K			iCE40HX8K			
	BG121	CB132	TQ144	BG121	CB132	CM225	CT256
General Purpose I/O per Bank							
Bank 0	23	24	27	23	24	46	52
Bank 1	21	25	29	21	25	42	52
Bank 2	19	18	19	19	18	40	46
Bank 3	26	24	28	26	24	46	52
Configuration	4	4	4	4	4	4	4
Total General Purpose Single Ended I/O	93	95	107	93	95	178	206
High Current Outputs per Bank							
Bank 0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0
Bank 3	0	0	0	0	0	0	0
Total Differential Inputs	0	0	0	0	0	0	0
Differential Inputs per Bank							
Bank 0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0
Bank 3	13	12	14	13	12	23	26
Total Differential Inputs	13	12	14	13	12	23	26
Dedicated Inputs per Bank							
Bank 0	0	0	0	0	0	0	0
Bank 1	0	1	1	0	1	1	1
Bank 2	2	2	2	2	2	2	2
Bank 3	0	0	0	0	0	0	0
Configuration	0	0	0	0	0	0	0
Total Dedicated Inputs	2	3	3	2	3	3	3
Vccio Pins							
Bank 0	1	2	2	1	2	3	4
Bank 1	1	2	2	1	2	3	4
Bank 2	1	2	2	1	2	3	4
Bank 3	2	3	2	2	3	4	4
VCC	4	5	4	4	5	8	6
VCC_SPI	1	1	1	1	1	1	1
VPP_2V5	1	1	1	1	1	1	1
VPP_FAST[1]	1	1	1	1	1	1	1
VCCPLL	2	2	2	2	2	2	2
GND	12	15	11	12	15	18	20
NC	0	0	6	0	0	0	0
Total Count of Bonded Pins	121	132	144	121	132	225	256

1. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications.

Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40LP384-CM36	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM36TR	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM36TR1K	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM49	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-CM49TR	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-CM49TR1K	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-SG32	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP384-SG32TR	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP384-SG32TR1K	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP640-SWG16TR	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP640-SWG16TR50	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP640-SWG16TR1K	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR50	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR1K	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-CM36	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM36TR	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM36TR1K	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM49	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM49TR	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM49TR1K	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM81	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CM81TR	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CM81TR1K	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CB81	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CB81TR	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CB81TR1K	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CM121	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CM121TR	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CM121TR1K	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CB121	1280	1.2 V	Halogen-Free csBGA	121	IND
ICE40LP1K-QN84	1280	1.2 V	Halogen-Free QFN	84	IND
ICE40LP4K-CM81	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM81TR	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM81TR1K	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM121	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM121TR	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM121TR1K	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM225	3520	1.2 V	Halogen-Free ucBGA	225	IND
ICE40LP8K-CM81	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM81TR	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM81TR1K	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM121	7680	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP8K-CM121TR	7680	1.2 V	Halogen-Free ucBGA	121	IND

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40LP8K-CM121TR1K	7680	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP8K-CM225	7680	1.2 V	Halogen-Free ucBGA	225	IND

High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40HX1K-CB132	1280	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX1K-VQ100	1280	1.2 V	Halogen-Free VQFP	100	IND
ICE40HX1K-TQ144	1280	1.2 V	Halogen-Free TQFP	144	IND
ICE40HX4K-BG121	3520	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX4K-BG121TR	3520	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX4K-CB132	3520	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX4K-TQ144	3520	1.2 V	Halogen-Free TQFP	144	IND
ICE40HX8K-BG121	7680	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX8K-BG121TR	7680	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX8K-CB132	7680	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX8K-CM225	7680	1.2 V	Halogen-Free ucBGA	225	IND
ICE40HX8K-CT256	7680	1.2 V	Halogen-Free caBGA	256	IND

iCE40 LP/HX Family Data Sheet Supplemental Information

For Further Information

A variety of technical notes for the iCE40 family are available on the Lattice web site.

- TN1248, iCE40 Programming and Configuration
- TN1250, Memory Usage Guide for iCE40 Devices
- TN1251, iCE40 sysCLOCK PLL Design and Usage Guide
- TN1252, iCE40 Hardware Checklist
- TN1253, Using Differential I/O (LVDS, Sub-LVDS) in iCE40 Devices
- TN1074, PCB Layout Recommendations for BGA Packages
- iCE40 Pinout Files
- Thermal Management document
- Lattice design tools
- IBIS
- Package Diagrams Data Sheet
- Schematic Symbols

iCE40 LP/HX Family Data Sheet Revision History

March 2017 **Data Sheet DS1040**

Date	Version	Section	Change Summary
March 2017	3.3	Introduction	Updated Features section. Added 121-ball caBGA package for ICE40 HX4K/8K to Table 1-1, iCE40 Family Selection Guide.
		Architecture	Updated PLB Blocks section. Changed “subtracters” to “subtractors” in the Carry Logic description.
			Updated Clock/Control Distribution Network section. Switched the “Clock Enable“ and the “Reset” headings in Table 2-2, Global Buffer (GBUF) Connections to Programmable Logic Blocks.
		Pinout Information	Updated Pin Information Summary section. Added BG121information under iCE40HX4K and iCE40HX8K.
		Ordering Information	Updated iCE40 Part Number Description section. Added Shipping Method and BG121 package under High Performance (HX) Devices.
			Updated Ordering Information section. Added part numbers for BG121 under High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging.
		Supplemental Information	Corrected reference to “Package Diagrams Data Sheet”.
October 2015	3.2	Introduction	Updated Features section. Added footnote to 16 WLCSP Programmable I/O: Max Inputs (LVDS25) in Table 1-1, iCE40 Family Selection Guide.
		DC and Switching Characteristics	Updated sysCLOCK PLL Timing section. Changed t_{DT} conditions.
			Updated Programming NVCM Supply Current – LP Devices section. Changed I_{PP_2V5} and I_{CCIO}, I_{CC_SPI} units.
March 2015	3.1	DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics section. Changed LVCMOS 3.3 and LVCMOS 2. 5 V_{OH} Min. (V) from 0.5 to 0.4.
July 2014	3.0	DC and Switching Characteristics	Revised and/or added Typ. V_{CC} data in the following sections. — Static Supply Current – LP Devices — Static Supply Current – HX Devices — Programming NVCM Supply Current – LP Devices — Programming NVCM Supply Current – HX Devices In each section table, the footnote indicating Advanced device status was removed.
		Pinout Information	Updated Pin Information Summary section. Added footnote 1 to CM49 under iCE40LP1K.
April 2014	02.9	Ordering Information	Changed “i” to “I” in part number description and ordering part numbers.
			Added part numbers to the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table.

Date	Version	Section	Change Summary
April 2013	02.2	Introduction	Added the LP8K 81 ucBGA.
		Architecture	Corrected typos.
		DC and Switching Characteristics	Corrected typos. Added 7:1 LVDS waveforms.
		Pinout Information	Corrected typos in signal descriptions. Added the LP8K 81 ucBGA.
		Ordering Information	Added the LP8K 81 ucBGA.
March 2013	02.1	DC and Switching Characteristics	Recommended operating conditions added requirement for Master SPI.
			Updated Recommended Operating Conditions for V_{PP_2V5}.
			Updated Power-On-Reset Voltage Levels and sequence requirements.
			Updated Static Supply Current conditions.
			Changed unit for t_{SKEW_IO} from ns to ps.
			Updated range of CCLK f_{MAX}.
		Ordering Information	Updated ordering information to include tape and reel part numbers.
September 2012	02.0	—	Merged SiliconBlue iCE40 LP and HX data sheets and updated to Lattice format.
	01.31	—	Updated Table 1.
	01.3	—	Production release.
			Updated notes on Table 3: Recommended Operating Conditions.
			Updated values in Table 4, Table 5, Table 12, Table 13 and Table 17.
	01.21	—	Updated Figure 3 and Figure 4 to specify iCE40.
Aug 2012	01.2	—	Updated company name.
July 2011	01.1	—	Moved package specifications to iCE40 pinout Excel files.
			Updated Table 1 maximum I/Os.
	01.01	—	Added 640, 1K and 4K to Table 13 configuration times. Updated Table 1 maximum I/Os.
	01.0	—	Initial release.