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### Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

#### Details

Product Status	Active
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	35
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	49-VFBGA
Supplier Device Package	49-UCBGA (3x3)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lp1k-cm49">https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lp1k-cm49</a>

## Features

- **Flexible Logic Architecture**
  - Five devices with 384 to 7,680 LUT4s and 10 to 206 I/Os
- **Ultra Low Power Devices**
  - Advanced 40 nm low power process
  - As low as 21  $\mu$ A standby power
  - Programmable low swing differential I/Os
- **Embedded and Distributed Memory**
  - Up to 128 kbits sysMEM™ Embedded Block RAM
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
- **High Current LED Drivers**
  - Three High Current Drivers used for three different LEDs or one RGB LED
- **High Performance, Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8
    - LVDS25E, subLVDS
    - Schmitt trigger inputs, to 200 mV typical hysteresis
- Programmable pull-up mode
- **Flexible On-Chip Clocking**
  - Eight low-skew global clock resources
  - Up to two analog PLLs per device
- **Flexible Device Configuration**
  - SRAM is configured through:
    - Standard SPI Interface
    - Internal Nonvolatile Configuration Memory (NVCM)
- **Broad Range of Package Options**
  - WLCSP, QFN, VQFP, TQFP, ucBGA, caBGA, and csBGA package options
  - Small footprint package options
    - As small as 1.40 mm x 1.48 mm
  - Advanced halogen-free packaging

**Table 1-1. iCE40 Family Selection Guide**

Part Number	LP384	LP640	LP1K	LP4K	LP8K	HX1K	HX4K	HX8K
Logic Cells (LUT + Flip-Flop)	384	640	1,280	3,520	7,680	1,280	3,520	7,680
RAM4K Memory Blocks	0	8	16	20	32	16	20	32
RAM4K RAM bits	0	32K	64K	80K	128K	64K	80K	128K
Phase-Locked Loops (PLLs)	0	0	1 <sup>1</sup>	2 <sup>2</sup>	2 <sup>2</sup>	1 <sup>1</sup>	2	2
Maximum Programmable I/O Pins	63	25	95	167	178	95	95	206
Maximum Differential Input Pairs	8	3	12	20	23	11	12	26
High Current LED Drivers	0	3	3	0	0	0	0	0
Package	Code	Programmable I/O: Max Inputs (LVDS25)						
16 WLCSP (1.40 mm x 1.48 mm, 0.35 mm)	SWG16		10(0) <sup>1</sup>	10(0) <sup>1</sup>				
32 QFN (5 mm x 5 mm, 0.5 mm)	SG32	21(3)						
36 ucBGA (2.5 mm x 2.5 mm, 0.4 mm)	CM36	25(3)		25(3) <sup>1</sup>				
49 ucBGA (3 mm x 3 mm, 0.4 mm)	CM49	37(6)		35(5) <sup>1</sup>				
81 ucBGA (4 mm x 4 mm, 0.4 mm)	CM81			63(8)	63(9) <sup>2</sup>	63(9) <sup>2</sup>		
81 csBGA (5 mm x 5 mm, 0.5 mm)	CB81			62(9) <sup>1</sup>				

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**Table 1-1. iCE40 Family Selection Guide (continued)**

84 QFN (7 mm x 7 mm, 0.5 mm)	QN84			67(7) <sup>1</sup>					
100 VQFP (14 mm x 14 mm, 0.5 mm)	VQ100						72(9) <sup>1</sup>		
121 ucBGA (5 mm x 5 mm, 0.4 mm)	CM121			95(12)	93(13)	93(13)			
121 csBGA (6 mm x 6 mm, 0.5 mm)	CB121			92(12)					
121 caBGA (9 mm x 9 mm, 0.8 mm)	BG121							93(13)	93(13)
132 csBGA (8 mm x 8 mm, 0.5 mm)	CB132						95(11)	95(12)	95(12)
144 TQFP (20 mm x 20 mm, 0.5 mm)	TQ144						96(12)	107(14)	
225 ucBGA (7 mm x 7 mm, 0.4 mm)	CM225				178(23)	178(23)			178(23)
256-ball caBGA (14 mm x 14 mm, 0.8 mm)	CT256								206(26)

1. No PLL available on the 16 WLCSP, 36 ucBGA, 81 csBGA, 84 QFN and 100 VQFP packages.

2. Only one PLL available on the 81 ucBGA package.

3. High Current I/Os only available on the 16 WLCSP package.

## Introduction

The iCE40 family of ultra-low power, non-volatile FPGAs has five devices with densities ranging from 384 to 7680 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic, these devices feature Embedded Block RAM (EBR), Non-volatile Configuration Memory (NVCM) and Phase Locked Loops (PLLs). These features allow the devices to be used in low-cost, high-volume consumer and system applications. Select packages offer High-Current drivers that are ideal to drive three white LEDs, or one RGB LED.

The iCE40 devices are fabricated on a 40 nm CMOS low power process. The device architecture has several features such as programmable low-swing differential I/Os and the ability to turn off on-chip PLLs dynamically. These features help manage static and dynamic power consumption, resulting in low static power for all members of the family. The iCE40 devices are available in two versions – ultra low power (LP) and high performance (HX) devices.

The iCE40 FPGAs are available in a broad range of advanced halogen-free packages ranging from the space saving 1.40x1.48 mm WLCSP to the PCB-friendly 20x20 mm TQFP. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The iCE40 devices offer enhanced I/O features such as pull-up resistors. Pull-up features are controllable on a “per-pin” basis.

The iCE40 devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash or be configured by an external master such as a CPU.

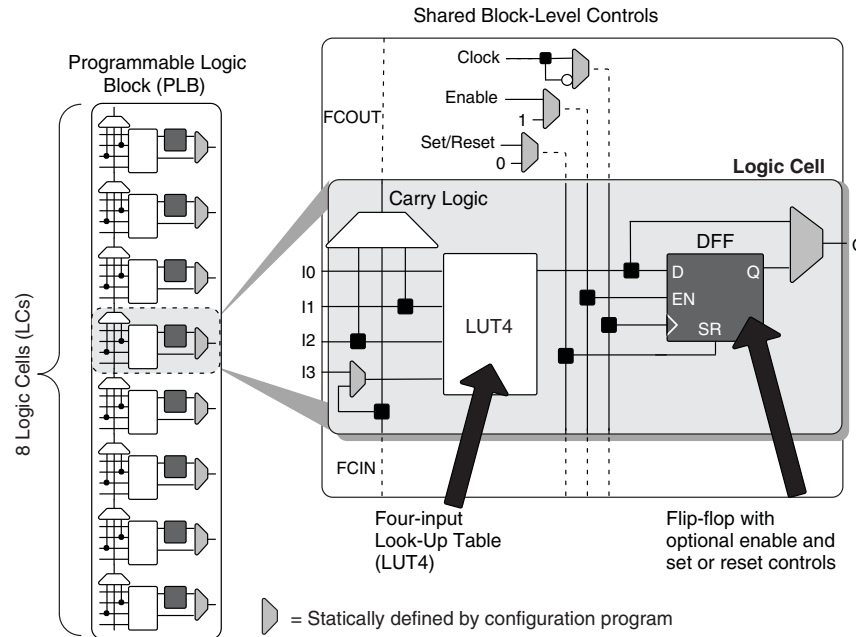
Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 family of devices. Popular logic synthesis tools provide synthesis library support for iCE40. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40 FPGA family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

**PLB Blocks**

The core of the iCE40 device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

**Figure 2-2. PLB Block Diagram**



**Logic Cells**

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT4) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT4 element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUT4s to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtractors, comparators, binary counters and some wide, cascaded logic functions.

**Table 2-1. Logic Cell Signal Descriptions**

Function	Type	Signal Names	Description
Input	Data signal	I0, I1, I2, I3	Inputs to LUT4
Input	Control signal	Enable	Clock enable shared by all LCs in the PLB
Input	Control signal	Set/Reset <sup>1</sup>	Asynchronous or synchronous local set/reset shared by all LCs in the PLB.
Input	Control signal	Clock	Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB
Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT4 or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

## Routing

There are many resources provided in the iCE40 devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

## Clock/Control Distribution Network

Each iCE40 device has eight global inputs, two pins on each side of the device. Note that not all GBINs are available in all packages.

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as GBIN[7:0] and the global buffers are identified as-GBUF[7:0]. These eight inputs may be used as general purpose I/O if they are not used to drive the clock nets. Global buffer GBUF7 in I/O Bank 3 also provides an optional direct LVDS25 or subLVDS differential clock input.

Table 2-2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input.

**Table 2-2. Global Buffer (GBUF) Connections to Programmable Logic Blocks**

Global Buffer	LUT Inputs	Clock	Reset	Clock Enable
GBUF0	Yes, any 4 of 8 GBUF Inputs	Yes	Yes	
GBUF1		Yes		Yes
GBUF2		Yes	Yes	
GBUF3		Yes		Yes
GBUF4		Yes	Yes	
GBUF5		Yes		Yes
GBUF6		Yes	Yes	
GBUF7		Yes		Yes

The maximum frequency for the global buffers are shown in the iCE40 External Switching Characteristics tables later in this document.

## Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

**Global Reset Control**

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

**sysCLOCK Phase Locked Loops (PLLs)**

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 devices have one or more sysCLOCK PLLs. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 6. The PLLOUT outputs can all be used to drive the iCE40 global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the  $t_{LOCK}$  parameter has been satisfied.

For more details on the PLL, see TN1251, [iCE40 sysCLOCK PLL Design and Usage Guide](#).

**Figure 2-3. PLL Diagram**

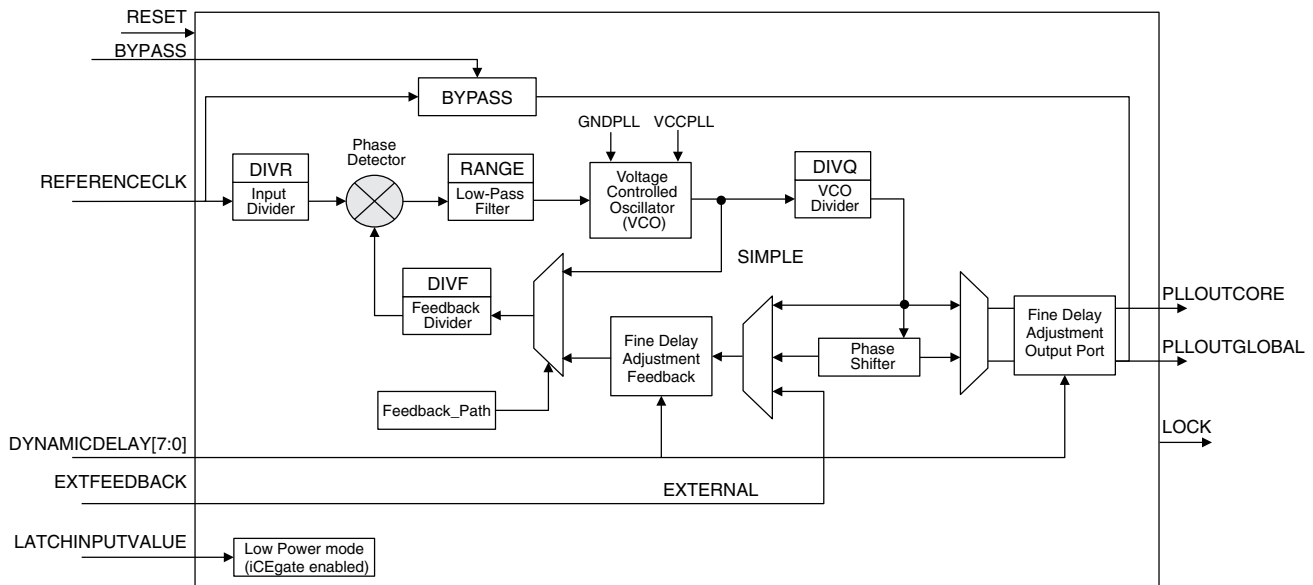


Table 2-3 provides signal descriptions of the PLL block.

**Table 2-3. PLL Signal Descriptions**

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	When FEEDBACK_PATH is set to SIMPLE, the BYPASS control selects which clock signal connects to the PLLOUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[3:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, forces the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.

### sysMEM Embedded Block RAM Memory

Larger iCE40 device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

#### sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

**Table 2-4. sysMEM Block Configurations<sup>1</sup>**

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4K)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4K)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4K)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4K)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40 EBR primitives with a negative-edged Read or Write clock, the base primitive name is appended with a 'N' and a 'R' or 'W' depending on the clock that is affected.

**RAM Initialization and ROM Operation**

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Note the sysMEM Embedded Block RAM Memory address 0 cannot be initialized.

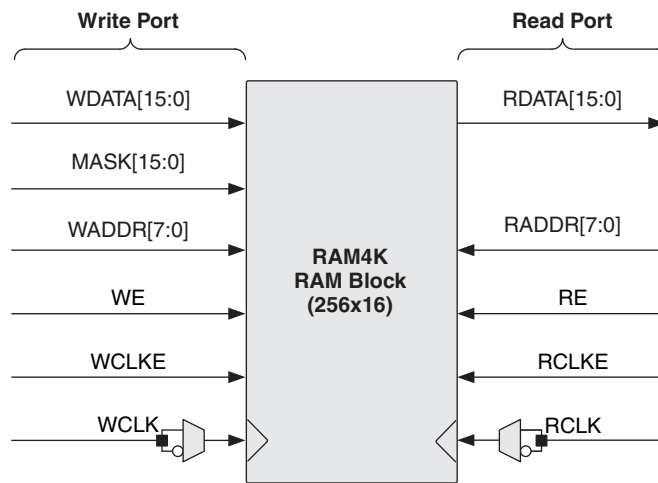
**Memory Cascading**

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

**RAM4k Block**

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

**Figure 2-4. sysMEM Memory Primitives**



**Table 2-5. EBR Signal Descriptions**

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = write bit; 1 = don't write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

For further information on the sysMEM EBR block, please refer to TN1250, [Memory Usage Guide for iCE40 Devices](#).



Figure 2-6. iCE I/O Register Block Diagram

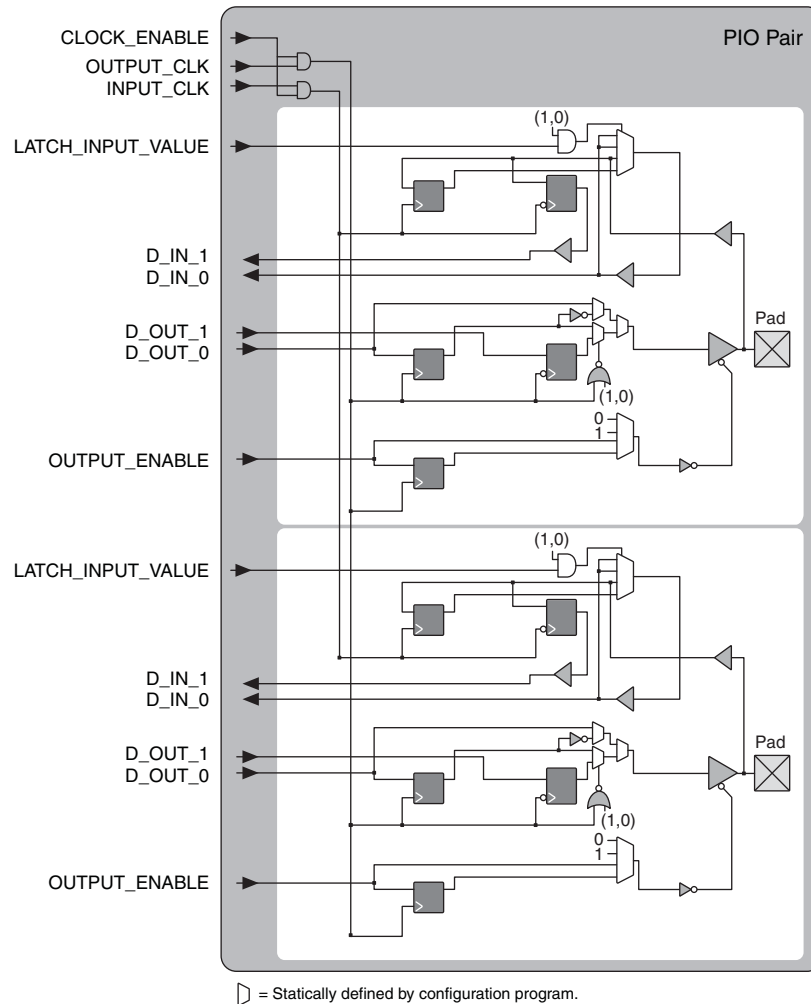


Table 2-6. PIO Signal List

Pin Name	I/O Type	Description
OUTPUT_CLK	Input	Output register clock
CLOCK_ENABLE	Input	Clock enable
INPUT_CLK	Input	Input register clock
OUTPUT_ENABLE	Input	Output enable
D_OUT_0/1	Input	Data from the core
D_IN_0/1	Output	Data to the core
LATCH_INPUT_VALUE	Input	Latches/holds the Input Value

### sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS and LVDS25.

High Current LED Drivers combine three sysIO buffers together. This allows for programmable drive strength. This also allows for high current drivers that are ideal to drive three white LEDs, or one RGB LED. Each bank is capable of supporting multiple I/O standards including single-ended LVCMOS buffers and differential LVDS25E output buf-

## DC Electrical Characteristics

### Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^{1,3,4,5,6,7}$	Input or I/O Leakage	$0V < V_{IN} < V_{CCIO} + 0.2 V$	—	—	+/-10	$\mu A$
$C_1^{6,7}$	I/O Capacitance <sup>2</sup>	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V$ $V_{CC} = \text{Typ.}, V_{IO} = 0 \text{ to } V_{CCIO} + 0.2 V$	—	6	—	pf
$C_2^{6,7}$	Global Input Buffer Capacitance <sup>2</sup>	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V$ $V_{CC} = \text{Typ.}, V_{IO} = 0 \text{ to } V_{CCIO} + 0.2 V$	—	6	—	pf
$V_{HYST}$	Input Hysteresis	$V_{CCIO} = 1.8 V, 2.5 V, 3.3 V$	—	200	—	mV
$I_{PU}^{6,7}$	Internal PIO Pull-up Current	$V_{CCIO} = 1.8 V, 0 < V_{IN} <= 0.65 V_{CCIO}$	-3	—	-31	$\mu A$
		$V_{CCIO} = 2.5 V, 0 < V_{IN} <= 0.65 V_{CCIO}$	-8	—	-72	$\mu A$
		$V_{CCIO} = 3.3 V, 0 < V_{IN} <= 0.65 V_{CCIO}$	-11	—	-128	$\mu A$

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2.  $T_J = 25^\circ C, f = 1.0 \text{ MHz}$ .
3. Please refer to  $V_{IL}$  and  $V_{IH}$  in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Only applies to IOs in the SPI bank following configuration.
5. Some products are clamped to a diode when  $V_{IN}$  is larger than  $V_{CCIO}$ .
6. High current IOs has three sysIO buffers connected together.
7. The iCE40LP640 and iCE40LP1K SWG16 package has CDONE and a sysIO buffer are connected together.

## Static Supply Current – LP Devices<sup>1, 2, 3, 4</sup>

Symbol	Parameter	Device	Typ. $V_{CC}^4$	Units
$I_{CC}$	Core Power Supply	iCE40LP384	21	$\mu A$
		iCE40LP640	100	$\mu A$
		iCE40LP1K	100	$\mu A$
		iCE40LP4K	250	$\mu A$
		iCE40LP8K	250	$\mu A$
$I_{CCPLL}^{5,6}$	PLL Power Supply	All devices	0.5	$\mu A$
$I_{PP\_2V5}$	NVCM Power Supply	All devices	1.0	$\mu A$
$I_{CCIO}, I_{CC\_SPI}$	Bank Power Supply <sup>4</sup> $V_{CCIO} = 2.5 V$	All devices	3.5	$\mu A$

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at  $V_{CCIO}$  or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3.  $T_J = 25^\circ C$ , power supplies at nominal voltage.
4. Does not include pull-up.
5. No PLL available on the iCE40LP384 and iCE40LP640 device.
6.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.

## Programming NVCM Supply Current – HX Devices<sup>1, 2, 3, 4</sup>

Symbol	Parameter	Device	Typ. $V_{CC}^5$	Units
$I_{CC}$	Core Power Supply	iCE40HX1K	278	$\mu A$
		iCE40HX4K	1174	$\mu A$
		iCE40HX8K	1174	$\mu A$
$I_{CCPLL}^6$	PLL Power Supply	All devices	0.5	$\mu A$
$I_{PP\_2V5}$	NVCM Power Supply	All devices	2.5	mA
$I_{CCIO}^7, I_{CC\_SPI}$	Bank Power Supply <sup>5</sup>	All devices	3.5	mA

1. Assumes all inputs are held at  $V_{CCIO}$  or GND and all outputs are tri-stated.
2. Typical user pattern.
3. SPI programming is at 8 MHz.
4.  $T_J = 25^\circ C$ , power supplies at nominal voltage.
5. Per bank.  $V_{CCIO} = 2.5 V$ . Does not include pull-up.
6.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.
7.  $V_{PP\_FAST}$ , used only for fast production programming, must be left floating or unconnected in applications.

## Peak Startup Supply Current – LP Devices

Symbol	Parameter	Device	Max	Units
$I_{CCPEAK}$	Core Power Supply	iCE40LP384	7.7	mA
		iCELP640	6.4	mA
		iCE40LP1K	6.4	mA
		iCE40LP4K	15.7	mA
		iCE40LP8K	15.7	mA
$I_{CCPLLPEAK}^{1, 2, 4}$	PLL Power Supply	iCE40LP1K	1.5	mA
		iCELP640	1.5	mA
		iCE40LP4K	8.0	mA
		iCE40LP8K	8.0	mA
$I_{PP\_2V5PEAK}$	NVCM Power Supply	iCE40LP384	3.0	mA
		iCELP640	7.7	mA
		iCE40LP1K	7.7	mA
		iCE40LP4K	4.2	mA
		iCE40LP8K	4.2	mA
$I_{PP\_FASTPEAK}^3$	NVCM Programming Supply	iCE40LP384	5.7	mA
		iCELP640	8.1	mA
		iCE40LP1K	8.1	mA
$I_{CCIOPEAK}^5, I_{CC\_SPIPEAK}$	Bank Power Supply	iCE40LP384	8.4	mA
		iCELP640	3.3	mA
		iCE40LP1K	3.3	mA
		iCE40LP4K	8.2	mA
		iCE40LP8K	8.2	mA

1. No PLL available on the iCE40LP384 and iCE40LP640 device.
2.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.
3.  $V_{PP\_FAST}$ , used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the  $V_{PP\_FAST}$  ball connected to  $V_{CCIO\_0}$  ball externally.
4. While no PLL is available in the iCE40-LP640 the  $I_{CCPLLPEAK}$  is additive to  $I_{CCPEAK}$ .
5. iCE40LP384 requires  $V_{CC}$  to be greater than 0.7 V when  $V_{CCIO}$  and  $V_{CC\_SPI}$  are above GND.

### Peak Startup Supply Current – HX Devices

Symbol	Parameter	Device	Max	Units
$I_{CCPEAK}$	Core Power Supply	iCE40HX1K	6.9	mA
		iCE40HX4K	22.3	mA
		iCE40HX8K	22.3	mA
$I_{CCPLLPEAK}^1$	PLL Power Supply	iCE40HX1K	1.8	mA
		iCE40HX4K	6.4	mA
		iCE40HX8K	6.4	mA
$I_{PP\_2V5PEAK}$	NVCM Power Supply	iCE40HX1K	2.8	mA
		iCE40HX4K	4.1	mA
		iCE40HX8K	4.1	mA
$I_{CCIOPEAK}, I_{CC\_SPIPEAK}$	Bank Power Supply	iCE40HX1K	6.8	mA
		iCE40HX4K	6.8	mA
		iCE40HX8K	6.8	mA

1.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.

### sysIO Recommended Operating Conditions

Standard	$V_{CCIO}$ (V)		
	Min.	Typ.	Max.
LVC MOS 3.3	3.14	3.3	3.46
LVC MOS 2.5	2.37	2.5	2.62
LVC MOS 1.8	1.71	1.8	1.89
LVDS25E <sup>1,2</sup>	2.37	2.5	2.62
subLV DSE <sup>1,2</sup>	1.71	1.8	1.89

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.

2. Does not apply to Configuration Bank  $V_{CC\_SPI}$ .

### sysIO Single-Ended DC Electrical Characteristics

Input/ Output Standard	$V_{IL}$		$V_{IH}^1$		$V_{OL}$ Max. (V)	$V_{OH}$ Min. (V)	$I_{OL}$ Max. (mA)	$I_{OH}$ Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVC MOS 3.3	-0.3	0.8	2.0	$V_{CCIO} + 0.2$ V	0.4	$V_{CCIO} - 0.4$	8, 16 <sup>2</sup> , 24 <sup>2</sup>	-8, -16 <sup>2</sup> , -24 <sup>2</sup>
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVC MOS 2.5	-0.3	0.7	1.7	$V_{CCIO} + 0.2$ V	0.4	$V_{CCIO} - 0.4$	6, 12 <sup>2</sup> , 18 <sup>2</sup>	-6, -12 <sup>2</sup> , -18 <sup>2</sup>
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVC MOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	$V_{CCIO} + 0.2$ V	0.4	$V_{CCIO} - 0.4$	4, 8 <sup>2</sup> , 12 <sup>2</sup>	-4, -8 <sup>2</sup> , -12 <sup>2</sup>
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1

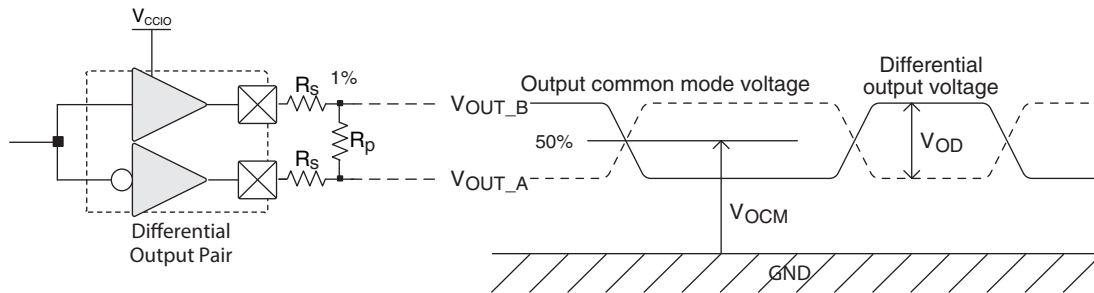
1. Some products are clamped to a diode when  $V_{IN}$  is larger than  $V_{CCIO}$ .

2. Only for High Drive LED outputs.

## SubLVDS Emulation

The iCE40 family supports the differential subLVDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all banks of the devices. The subLVDS input standard is supported by the LVDS25 differential input buffer. The scheme shown in Figure 3-2 is one possible solution for subLVDS output standard implementation. Use LVDS25E mode with suggested resistors for subLVDS operation. Resistor values in Figure 3-2 are industry standard values for 1% resistors.

**Figure 3-2. subLVDS**



**Table 3-2. subLVDS DC Conditions**

### Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
$Z_{OUT}$	Output impedance	20	Ohms
$R_S$	Driver series resistor	270	Ohms
$R_P$	Driver parallel resistor	120	Ohms
$R_T$	Receiver termination	100	Ohms
$V_{OH}$	Output high voltage	1.43	V
$V_{OL}$	Output low voltage	1.07	V
$V_{OD}$	Output differential voltage	0.35	V
$V_{CM}$	Output common mode voltage	0.9	V
$Z_{BACK}$	Back impedance	100.5	Ohms
$I_{DC}$	DC output current	2.8	mA

## Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

## Maximum sysIO Buffer Performance<sup>2</sup>

I/O Standard	Max. Speed	Units
<b>Inputs</b>		
LVDS25 <sup>1</sup>	400	MHz
subLVDS18 <sup>1</sup>	400	MHz
LVC MOS33	250	MHz
LVC MOS25	250	MHz
LVC MOS18	250	MHz
<b>Outputs</b>		
LVDS25E	250	MHz
subLVDS18E	155	MHz
LVC MOS33	250	MHz
LVC MOS25	250	MHz
LVC MOS18	155	MHz

1. Supported in Bank 3 only.
2. Measured with a toggling pattern

## iCE40 Family Timing Adders

Over Recommended Commercial Operating Conditions - LP Devices<sup>1, 2, 3, 4, 5</sup>

Buffer Type	Description	Timing	Units
<b>Input Adjusters</b>			
LVDS25	LVDS, $V_{CCIO} = 2.5\text{ V}$	-0.18	ns
subLVDS	subLVDS, $V_{CCIO} = 1.8\text{ V}$	0.82	ns
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3\text{ V}$	0.18	ns
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	0.00	ns
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	0.19	ns
<b>Output Adjusters</b>			
LVDS25E	LVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	0.00	ns
subLVDS25E	subLVDS, Emulated, $V_{CCIO} = 1.8\text{ V}$	1.32	ns
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3\text{ V}$	-0.12	ns
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	0.00	ns
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	1.32	ns

1. Timing adders are relative to LVC MOS25 and characterized but not tested on every device.
2. LVC MOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Commercial timing numbers are shown.
5. Not all I/O standards are supported for all banks. See the Architecture section of this data sheet for details.

## iCE40 External Switching Characteristics – LP Devices <sup>1, 2</sup>

Over Recommended Operating Conditions

Parameter	Description	Device	Min.	Max.	Units
<b>Clocks</b>					
<b>Global Clocks</b>					
f <sub>MAX_GBUF</sub>	Frequency for Global Buffer Clock network	All iCE40LP devices	—	275	MHz
t <sub>W_GBUF</sub>	Clock Pulse Width for Global Buffer	All iCE40LP devices	0.92	—	ns
t <sub>SKEW_GBUF</sub>	Global Buffer Clock Skew Within a Device	iCE40LP384	—	370	ps
		iCE40LP640	—	230	ps
		iCE40LP1K	—	230	ps
		iCE40LP4K	—	340	ps
		iCE40LP8K	—	340	ps
<b>Pin-LUT-Pin Propagation Delay</b>					
t <sub>PD</sub>	Best case propagation delay through one LUT-4	All iCE40LP devices	—	9.36	ns
<b>General I/O Pin Parameters (Using Global Buffer Clock without PLL)<sup>3</sup></b>					
t <sub>SKEW_IO</sub>	Data bus skew across a bank of IOs	iCE40LP384	—	300	ps
		iCE40LP640	—	200	ps
		iCE40LP1K	—	200	ps
		iCE40LP4K	—	280	ps
		iCE40LP8K	—	280	ps
t <sub>CO</sub>	Clock to Output - PIO Output Register	iCE40LP384	—	6.33	ns
		iCE40LP640	—	5.91	ns
		iCE40LP1K	—	5.91	ns
		iCE40LP4K	—	6.58	ns
		iCE40LP8K	—	6.58	ns
t <sub>SU</sub>	Clock to Data Setup - PIO Input Register	iCE40LP384	-0.08	—	ns
		iCE40LP640	-0.33	—	ns
		iCE40LP1K	-0.33	—	ns
		iCE40LP4K	-0.63	—	ns
		iCE40LP8K	-0.63	—	ns
t <sub>H</sub>	Clock to Data Hold - PIO Input Register	iCE40LP384	1.99	—	ns
		iCE40LP640	2.81	—	ns
		iCE40LP1K	2.81	—	ns
		iCE40LP4K	3.48	—	ns
		iCE40LP8K	3.48	—	ns
<b>General I/O Pin Parameters (Using Global Buffer Clock with PLL)<sup>3</sup></b>					
t <sub>COPLL</sub>	Clock to Output - PIO Output Register	iCE40LP1K	—	2.20	ns
		iCE40LP4K	—	2.30	ns
		iCE40LP8K	—	2.30	ns
t <sub>SUPLL</sub>	Clock to Data Setup - PIO Input Register	iCE40LP1K	5.23	—	ns
		iCE40LP4K	6.13	—	ns
		iCE40LP8K	6.13	—	ns

## sysCLOCK PLL Timing

### Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
$f_{IN}$	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)		10	133	MHz
$f_{OUT}$	Output Clock Frequency (PLLOUT)		16	275	MHz
$f_{VCO}$	PLL VCO Frequency		533	1066	MHz
$f_{PFD}$	Phase Detector Input Frequency		10	133	MHz
<b>AC Characteristics</b>					
$t_{DT}$	Output Clock Duty Cycle	$f_{OUT} < 175$ MHz	40	50	%
		$175 \text{ MHz} < f_{OUT} < 275$ MHz	35	65	"%
$t_{PH}$	Output Phase Accuracy		—	+/-12	deg
$t_{OPJIT}^{1,5}$	Output Clock Period Jitter	$f_{OUT} \leq 100$ MHz	—	450	ps p-p
		$f_{OUT} > 100$ MHz	—	0.05	UIPP
	Output Clock Cycle-to-cycle Jitter	$f_{OUT} \leq 100$ MHz	—	750	ps p-p
		$f_{OUT} > 100$ MHz	—	0.10	UIPP
	Output Clock Phase Jitter	$f_{PFD} \leq 25$ MHz	—	275	ps p-p
		$f_{PFD} > 25$ MHz	—	0.05	UIPP
$t_W$	Output Clock Pulse Width	At 90% or 10%	1.3	—	ns
$t_{LOCK}^{2,3}$	PLL Lock-in Time		—	50	us
$t_{UNLOCK}$	PLL Unlock Time		—	50	ns
$t_{IPJIT}^4$	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
$t_{FDTAP}$	Fine Delay adjustment, per Tap		147	195	ps
$t_{STABLE}^3$	LATCHINPUTVALUE LOW to PLL Stable		—	500	ns
$t_{STABLE\_PW}^3$	LATCHINPUTVALUE Pulse Width		—	100	ns
$t_{RST}$	RESET Pulse Width		10	—	ns
$t_{RSTREC}$	RESET Recovery Time		10	—	us
$t_{DYNAMIC\_WD}$	DYNAMICDELAY Pulse Width		100	—	VCO Cycles
$t_{PDBYPASS}$	Propagation delay with the PLL in bypass mode	iCE40LP	1.18	4.68	ns
		iCE40HX	1.73	4.07	ns

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after  $t_{LOCK}$  for PLL reset and dynamic delay adjustment.
3. At minimum  $f_{PFD}$ . As the  $f_{PFD}$  increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.



**Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging**

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40LP384-CM36	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM36TR	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM36TR1K	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM49	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-CM49TR	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-CM49TR1K	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-SG32	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP384-SG32TR	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP384-SG32TR1K	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP640-SWG16TR	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP640-SWG16TR50	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP640-SWG16TR1K	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR50	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR1K	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-CM36	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM36TR	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM36TR1K	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM49	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM49TR	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM49TR1K	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM81	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CM81TR	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CM81TR1K	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CB81	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CB81TR	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CB81TR1K	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CM121	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CM121TR	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CM121TR1K	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CB121	1280	1.2 V	Halogen-Free csBGA	121	IND
ICE40LP1K-QN84	1280	1.2 V	Halogen-Free QFN	84	IND
ICE40LP4K-CM81	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM81TR	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM81TR1K	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM121	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM121TR	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM121TR1K	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM225	3520	1.2 V	Halogen-Free ucBGA	225	IND
ICE40LP8K-CM81	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM81TR	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM81TR1K	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM121	7680	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP8K-CM121TR	7680	1.2 V	Halogen-Free ucBGA	121	IND

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40LP8K-CM121TR1K	7680	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP8K-CM225	7680	1.2 V	Halogen-Free ucBGA	225	IND

**High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging**

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40HX1K-CB132	1280	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX1K-VQ100	1280	1.2 V	Halogen-Free VQFP	100	IND
ICE40HX1K-TQ144	1280	1.2 V	Halogen-Free TQFP	144	IND
ICE40HX4K-BG121	3520	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX4K-BG121TR	3520	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX4K-CB132	3520	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX4K-TQ144	3520	1.2 V	Halogen-Free TQFP	144	IND
ICE40HX8K-BG121	7680	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX8K-BG121TR	7680	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX8K-CB132	7680	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX8K-CM225	7680	1.2 V	Halogen-Free ucBGA	225	IND
ICE40HX8K-CT256	7680	1.2 V	Halogen-Free caBGA	256	IND

## For Further Information

A variety of technical notes for the iCE40 family are available on the Lattice web site.

- [TN1248, iCE40 Programming and Configuration](#)
- [TN1250, Memory Usage Guide for iCE40 Devices](#)
- [TN1251, iCE40 sysCLOCK PLL Design and Usage Guide](#)
- [TN1252, iCE40 Hardware Checklist](#)
- [TN1253, Using Differential I/O \(LVDS, Sub-LVDS\) in iCE40 Devices](#)
- [TN1074, PCB Layout Recommendations for BGA Packages](#)
- [iCE40 Pinout Files](#)
- [Thermal Management](#) document
- [Lattice design tools](#)
- [IBIS](#)
- [Package Diagrams Data Sheet](#)
- [Schematic Symbols](#)

Date	Version	Section	Change Summary
March 2017	3.3	Introduction	Updated <a href="#">Features</a> section. Added 121-ball caBGA package for ICE40 HX4K/8K to Table 1-1, iCE40 Family Selection Guide.
		Architecture	Updated <a href="#">PLB Blocks</a> section. Changed “subtractors” to “subtractions” in the Carry Logic description.
			Updated <a href="#">Clock/Control Distribution Network</a> section. Switched the “Clock Enable” and the “Reset” headings in Table 2-2, Global Buffer (GBUF) Connections to Programmable Logic Blocks.
		Pinout Information	Updated <a href="#">Pin Information Summary</a> section. Added BG121 information under iCE40HX4K and iCE40HX8K.
		Ordering Information	Updated <a href="#">iCE40 Part Number Description</a> section. Added Shipping Method and BG121 package under High Performance (HX) Devices.
			Updated <a href="#">Ordering Information</a> section. Added part numbers for BG121 under High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging.
Supplemental Information	Corrected reference to “Package Diagrams Data Sheet”.		
October 2015	3.2	Introduction	Updated Features section. Added footnote to 16 WLCSP Programmable I/O: Max Inputs (LVDS25) in Table 1-1, iCE40 Family Selection Guide.
		DC and Switching Characteristics	Updated sysCLOCK PLL Timing section. Changed $t_{DT}$ conditions. Updated Programming NVCM Supply Current – LP Devices section. Changed $I_{PP\_2V5}$ and $I_{CCIO}$ , $I_{CC\_SPI}$ units.
March 2015	3.1	DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics section. Changed LVCMOS 3.3 and LVCMOS 2.5 $V_{OH}$ Min. (V) from 0.5 to 0.4.
July 2014	3.0	DC and Switching Characteristics	Revised and/or added Typ. $V_{CC}$ data in the following sections. <ul style="list-style-type: none"> <li>— Static Supply Current – LP Devices</li> <li>— Static Supply Current – HX Devices</li> <li>— Programming NVCM Supply Current – LP Devices</li> <li>— Programming NVCM Supply Current – HX Devices</li> </ul> In each section table, the footnote indicating Advanced device status was removed.
		Pinout Information	Updated Pin Information Summary section. Added footnote 1 to CM49 under iCE40LP1K.
April 2014	02.9	Ordering Information	Changed “I” to “l” in part number description and ordering part numbers.
			Added part numbers to the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table.

Date	Version	Section	Change Summary
April 2013	02.2	Introduction	Added the LP8K 81 ucBGA.
		Architecture	Corrected typos.
		DC and Switching Characteristics	Corrected typos. Added 7:1 LVDS waveforms.
		Pinout Information	Corrected typos in signal descriptions. Added the LP8K 81 ucBGA.
		Ordering Information	Added the LP8K 81 ucBGA.
March 2013	02.1	DC and Switching Characteristics	Recommended operating conditions added requirement for Master SPI.
			Updated Recommended Operating Conditions for $V_{PP\_2V5}$ .
			Updated Power-On-Reset Voltage Levels and sequence requirements.
			Updated Static Supply Current conditions.
			Changed unit for $t_{SKEW\_IO}$ from ns to ps.
		Updated range of CCLK $f_{MAX}$ .	
Ordering Information	Updated ordering information to include tape and reel part numbers.		
September 2012	02.0	—	Merged SiliconBlue iCE40 LP and HX data sheets and updated to Lattice format.
	01.31	—	Updated Table 1.
	01.3	—	Production release.
			Updated notes on Table 3: Recommended Operating Conditions. Updated values in Table 4, Table 5, Table 12, Table 13 and Table 17.
	01.21	—	Updated Figure 3 and Figure 4 to specify iCE40.
Aug 2012	01.2	—	Updated company name.
July 2011	01.1	—	Moved package specifications to iCE40 pinout Excel files.
			Updated Table 1 maximum I/Os.
	01.01	—	Added 640, 1K and 4K to Table 13 configuration times. Updated Table 1 maximum I/Os.
	01.0	—	Initial release.