Lattice Semiconductor Corporation - ICE40LP1K-SWG16TR1K Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	10
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	16-XFBGA, WLCSP
Supplier Device Package	16-WLCSP (1.4x1.48)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lp1k-swg16tr1k

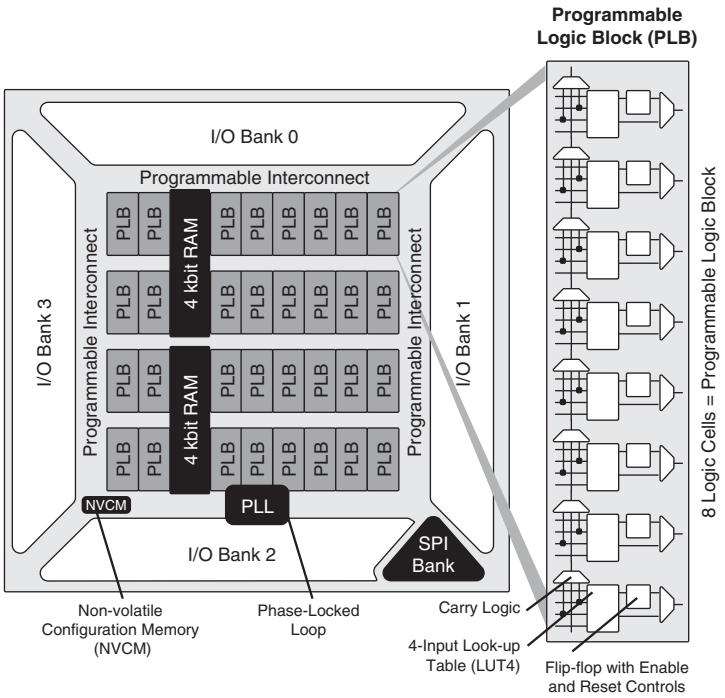
iCE40 LP/HX Family Data Sheet Architecture

March 2017 Data Sheet DS1040

Architecture Overview

The iCE40 family architecture contains an array of Programmable Logic Blocks (PLB), sysCLOCK™ PLLs, Nonvolatile Programmable Configuration Memory (NVCM) and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 2-1 shows the block diagram of the iCE40LP/HX1K device.

Figure 2-1. iCE40LP/HX1K Device, Top View



The logic blocks, Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either logic blocks or EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40 family, there are up to four independent sysIO banks. Note on some packages V_{CCIO} banks are tied together. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large 4 kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO.

The iCE40 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

Every device in the family has a SPI port that supports programming and configuration of the device. The iCE40 includes on-chip, Nonvolatile Configuration Memory (NVCM).

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sysIO

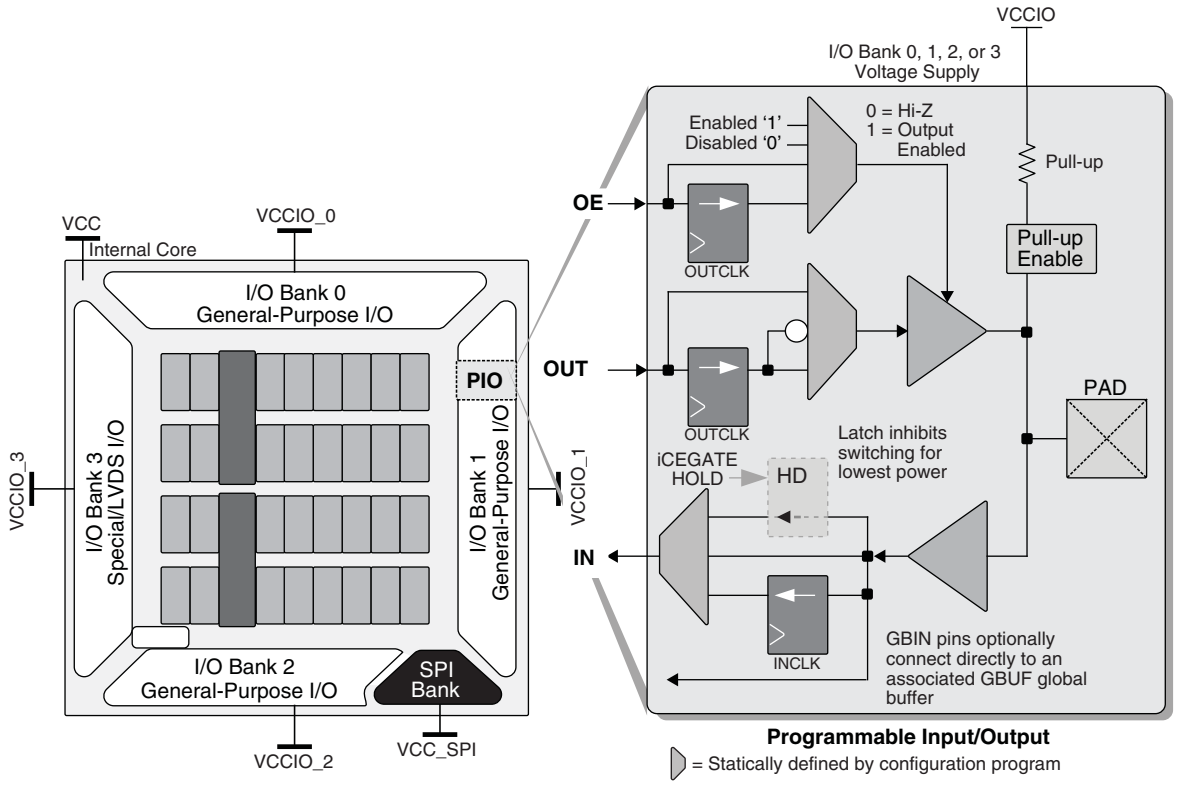
Buffer Banks

iCE40 devices have up to four I/O banks with independent V_{CCIO} rails with an additional configuration bank V_{CC_SPI} for the SPI I/Os.

Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. The PIOs are placed on all four sides of the device.

Figure 2-5. I/O Bank and Programmable I/O Cell



The PIO contains three blocks: an input register block, output register block iCEgate™ and tri-state register block. To save power, the optional iCEgate™ latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock signal, creating two data streams.

Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers. In Generic DDR mode, two registers are used to capture the data on the positive and negative edge of the system clock and then muxed creating one data stream.

Figure 2-6 shows the input/output register block for the PIOs.

Power On Reset

iCE40 devices have power-on reset circuitry to monitor V_{CC}, V_{CCIO_2}, V_{PP_2V5}, and V_{CC_SPI} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CC}, V_{CCIO_2}, V_{PP_2V5}, and V_{CC_SPI} (controls configuration) voltage levels. It then triggers download from the on-chip NVCM or external Flash memory after reaching the power-up levels specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

Programming and Configuration

This section describes the programming and configuration of the iCE40 family.

Device Programming

The NVCM memory can be programmed through the SPI port.

Device Configuration

There are various ways to configure the Configuration RAM (CRAM) including:

1. Internal NVCM Download
2. From a SPI Flash (Master SPI mode)
3. System microprocessor to drive a Serial Slave SPI port (SSPI mode)

The image to configure the CRAM can be selected by the user on power up (Cold Boot) or once powered up (Warm Boot).

For more details on programming and configuration, see TN1248, iCE40 Programming and Configuration Usage Guide.

Power Saving Options

iCE40 devices are available in two options for maximum flexibility: LP and HX devices. The LP devices have ultra low static and dynamic power consumption. HX devices are designed to provide high performance. Both the LP and the HX devices operate at 1.2 V V_{CC}.

iCE40 devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. While these features are available in both device types, these features are mainly intended for use with iCE40 LP devices to manage power consumption.

Table 2-9. iCE40 Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, forces the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEgate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

iCE40 LP/HX Family Data Sheet DC and Switching Characteristics

October 2015 Data Sheet DS1040

Absolute Maximum Ratings[1, 2, 3, 4]

	iCE40 LP/HX
Supply Voltage V_{CC}	–0.5 V to 1.42 V
Output Supply Voltage V_{CCIO}, V_{CC_SPI}	–0.5 V to 3.60 V
NVCM Supply Voltage V_{PP_2V5}	–0.5 V to 3.60 V
PLL Supply Voltage V_{CCPLL}	–0.5 V to 1.30 V
I/O Tri-state Voltage Applied	–0.5 V to 3.60 V
Dedicated Input Voltage Applied	–0.5 V to 3.60 V
Storage Temperature (Ambient)	–65 °C to 150 °C
Junction Temperature (T_J)	–55 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. IOs can support a 200 mV Overshoot above the Recommend Operating Conditions V_{CCIO} (Max) and -200mV Undershoot below V_{IL} (Min). Overshoot and Undershoot is permitted for 25% duty cycle but must not exceed 1.6 ns.

Recommended Operating Conditions[1]

Symbol	Parameter		Min.	Max.	Units
V_{CC}[1]	Core Supply Voltage		1.14	1.26	V
V_{PP_2V5}	V_{PP_2V5} NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configure from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
V_{PP_FAST}[4]	Optional fast NVCM programming supply. Leave unconnected.		N/A	N/A	V
V_{CCPLL}[5, 6]	PLL Supply Voltage		1.14	1.26	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	$V_{CCIO0-3}$	1.71	3.46	V
		V_{CC_SPI}	1.71	3.46	V
t_{JIND}	Junction Temperature Industrial Operation		–40	100	°C
t_{PROG}	Junction Temperature NVCM Programming		10	30	°C

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC_SPI} are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the V_{PP_FAST} ball connected to V_{CCIO_0} ball externally.
5. No PLL available on the iCE40LP384 and iCE40LP640 device.
6. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.

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Static Supply Current – HX Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ. V_{CC}[4]	Units
I_{CC}	Core Power Supply	iCE40HX1K	296	µA
		iCE40HX4K	1140	µA
		iCE40HX8K	1140	µA
I_{CCPLL}[5]	PLL Power Supply	All devices	0.5	µA
I_{PP_2V5}	NVCM Power Supply	All devices	1.0	µA
I_{CCIO}, I_{CC_SPI}	Bank Power Supply[4] V_{CCIO} = 2.5 V	All devices	3.5	µA

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. T_J = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up.
5. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.

Programming NVCM Supply Current – LP Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ. V_{CC}[5]	Units
I_{CC}	Core Power Supply	iCE40LP384	60	µA
		iCE40LP640	120	µA
		iCE40LP1K	120	µA
		iCE40LP4K	350	µA
		iCE40LP8K	350	µA
I_{CCPLL}[6, 7]	PLL Power Supply	All devices	0.5	µA
I_{PP_2V5}	NVCM Power Supply	All devices	2.5	mA
I_{CCIO}[8], I_{CC_SPI}	Bank Power Supply[5]	All devices	3.5	mA

1. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
2. Typical user pattern.
3. SPI programming is at 8 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up.
6. No PLL available on the iCE40-LP384 and iCE40-LP640 device.
7. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.
8. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the V_{PP_FAST} ball connected to V_{CCIO_0} ball externally.

Programming NVCM Supply Current – HX Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ. V_{CC}[5]	Units
I_{CC}	Core Power Supply	iCE40HX1K	278	µA
		iCE40HX4K	1174	µA
		iCE40HX8K	1174	µA
I_{CCPLL}[6]	PLL Power Supply	All devices	0.5	µA
I_{PP_2V5}	NVCM Power Supply	All devices	2.5	mA
I_{CCIO}[7], I_{CC_SPI}	Bank Power Supply[5]	All devices	3.5	mA

1. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
2. Typical user pattern.
3. SPI programming is at 8 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up.
6. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.
7. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications.

Peak Startup Supply Current – LP Devices

Symbol	Parameter	Device	Max	Units
I_{CCPEAK}	Core Power Supply	iCE40LP384	7.7	mA
		iCELP640	6.4	mA
		iCE40LP1K	6.4	mA
		iCE40LP4K	15.7	mA
		iCE40LP8K	15.7	mA
$I_{CCPLLPEAK}$[1, 2, 4]	PLL Power Supply	iCE40LP1K	1.5	mA
		iCELP640	1.5	mA
		iCE40LP4K	8.0	mA
		iCE40LP8K	8.0	mA
$I_{PP_2V5PEAK}$	NVCM Power Supply	iCE40LP384	3.0	mA
		iCELP640	7.7	mA
		iCE40LP1K	7.7	mA
		iCE40LP4K	4.2	mA
		iCE40LP8K	4.2	mA
$I_{PP_FASTPEAK}$[3]	NVCM Programming Supply	iCE40LP384	5.7	mA
		iCELP640	8.1	mA
		iCE40LP1K	8.1	mA
$I_{CCIOPEAK}$[5], $I_{CC_SPIPEAK}$	Bank Power Supply	iCE40LP384	8.4	mA
		iCELP640	3.3	mA
		iCE40LP1K	3.3	mA
		iCE40LP4K	8.2	mA
		iCE40LP8K	8.2	mA

1. No PLL available on the iCE40LP384 and iCE40LP640 device.
2. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.
3. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the V_{PP_FAST} ball connected to V_{CCIO_0} ball externally.
4. While no PLL is available in the iCE40-LP640 the $I_{CCPLLPEAK}$ is additive to I_{CCPEAK}.
5. iCE40LP384 requires V_{CC} to be greater than 0.7 V when V_{CCIO} and V_{CC_SPI} are above GND.

SubLVDS Emulation

The iCE40 family supports the differential subLVDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all banks of the devices. The subLVDS input standard is supported by the LVDS25 differential input buffer. The scheme shown in Figure 3-2 is one possible solution for subLVDSE output standard implementation. Use LVDS25E mode with suggested resistors for subLVDSE operation. Resistor values in Figure 3-2 are industry standard values for 1% resistors.

Figure 3-2. subLVDSE

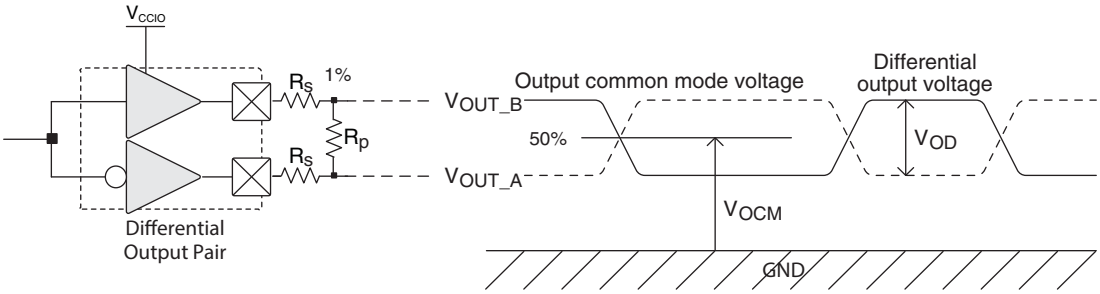

Table 3-2. subLVDSE DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	270	Ohms
R_P	Driver parallel resistor	120	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	0.9	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	2.8	mA

Typical Building Block Function Performance – LP Devices[1, 2]

Pin-to-Pin Performance (LVCMOS25)

Function	Timing	Units
Basic Functions		
16-bit decoder	11.0	ns
4:1 MUX	12.0	ns
16:1 MUX	13.0	ns

Register-to-Register Performance

Function	Timing	Units
Basic Functions		
16:1 MUX	190	MHz
16-bit adder	160	MHz
16-bit counter	175	MHz
64-bit counter	65	MHz
Embedded Memory Functions		
256x16 Pseudo-Dual Port RAM	240	MHz

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a V_{CC} of 1.14 V at Junction Temp 85 °C.

Typical Building Block Function Performance – HX Devices[1, 2]

Pin-to-Pin Performance (LVCMOS25)

Function	Timing	Units
Basic Functions		
16-bit decoder	10.0	ns
4:1 MUX	9.0	ns
16:1 MUX	9.5	ns

Register-to-Register Performance

Function	Timing	Units
Basic Functions		
16:1 MUX	305	MHz
16-bit adder	220	MHz
16-bit counter	255	MHz
64-bit counter	105	MHz
Embedded Memory Functions		
256x16 Pseudo-Dual Port RAM	403	MHz

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a V_{CC} of 1.14 V at Junction Temp 85 °C.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

Maximum sysIO Buffer Performance[2]

I/O Standard	Max. Speed	Units
Inputs		
LVDS25[1]	400	MHz
subLVDS18[1]	400	MHz
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	250	MHz
Outputs		
LVDS25E	250	MHz
subLVDS18E	155	MHz
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	155	MHz

1. Supported in Bank 3 only.
2. Measured with a toggling pattern

iCE40 Family Timing Adders

Over Recommended Commercial Operating Conditions - LP Devices[1, 2, 3, 4, 5]

Buffer Type	Description	Timing	Units
Input Adjusters			
LVDS25	LVDS, V_{CCIO} = 2.5 V	–0.18	ns
subLVDS	subLVDS, V_{CCIO} = 1.8 V	0.82	ns
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.18	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	0.19	ns
Output Adjusters			
LVDS25E	LVDS, Emulated, V_{CCIO} = 2.5 V	0.00	ns
subLVDSE	subLVDS, Emulated, V_{CCIO} = 1.8 V	1.32	ns
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	–0.12	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	1.32	ns

1. Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Commercial timing numbers are shown.
5. Not all I/O standards are supported for all banks. See the Architecture section of this data sheet for details.

iCE40 External Switching Characteristics – LP Devices (Continued)[1, 2]

Over Recommended Operating Conditions

Parameter	Description	Device	Min.	Max.	Units
t_{HPLL}	Clock to Data Hold - PIO Input Register	iCE40LP1K	–0.90	—	ns
		iCE40LP4K	–0.80	—	ns
		iCE40LP8K	–0.80	—	ns

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions can be extracted from the iCECube2 software.
2. General I/O timing numbers based on LVCMOS 2.5, 0pf load.
3. Supported on devices with a PLL.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)		10	133	MHz
f_{OUT}	Output Clock Frequency (PLLOUT)		16	275	MHz
f_{VCO}	PLL VCO Frequency		533	1066	MHz
f_{PFD}	Phase Detector Input Frequency		10	133	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	f_{OUT} < 175 MHz	40	50	%
		175 MHz < f_{OUT} < 275 MHz	35	65	"%
t_{PH}	Output Phase Accuracy		—	+/–12	deg
t_{OPJIT}[1, 5]	Output Clock Period Jitter	f_{OUT} <= 100 MHz	—	450	ps p-p
		f_{OUT} > 100 MHz	—	0.05	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} <= 100 MHz	—	750	ps p-p
		f_{OUT} > 100 MHz	—	0.10	UIPP
	Output Clock Phase Jitter	f_{PFD} <= 25 MHz	—	275	ps p-p
		f_{PFD} > 25 MHz	—	0.05	UIPP
t_W	Output Clock Pulse Width	At 90% or 10%	1.3	—	ns
t_{LOCK}[2, 3]	PLL Lock-in Time		—	50	us
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}[4]	Input Clock Period Jitter	$f_{PFD} \geq$ 20 MHz	—	1000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{FDTAP}	Fine Delay adjustment, per Tap		147	195	ps
t_{STABLE}[3]	LATCHINPUTVALUE LOW to PLL Stable		—	500	ns
t_{STABLE_PW}[3]	LATCHINPUTVALUE Pulse Width		—	100	ns
t_{RST}	RESET Pulse Width		10	—	ns
t_{RSTREC}	RESET Recovery Time		10	—	us
$t_{DYNAMIC_WD}$	DYNAMICDELAY Pulse Width		100	—	VCO Cycles
$t_{PDBYPASS}$	Propagation delay with the PLL in bypass mode	iCE40LP	1.18	4.68	ns
		iCE40HX	1.73	4.07	ns

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. At minimum f_{PFD}. As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

SPI Master or NVCM Configuration Time[1, 2]

Symbol	Parameter	Conditions	Typ.	Units
t_{CONFIG}	POR/CRESET_B to Device I/O Active	iCE40LP384 - Low Frequency (Default)	25	ms
		iCE40LP384 - Medium Frequency	15	ms
		iCE40LP384 - High Frequency	11	ms
		iCE40LP640 - Low Frequency (Default)	53	ms
		iCE40LP640 - Medium Frequency	25	ms
		iCE40LP640 - High Frequency	13	ms
		iCE40LP/HX1K - Low Frequency (Default)	53	ms
		iCE40LP/HX1K - Medium Frequency	25	ms
		iCE40LP/HX1K - High Frequency	13	ms
		iCE40LP/HX4K - Low Frequency (Default)	230	ms
		iCE40LP/HX4K - Medium Frequency	110	ms
		iCE40LP/HX4K - High Frequency	70	ms
		iCE40LP/HX8K - Low Frequency (Default)	230	ms
		iCE40LP/HX8K - Medium Frequency	110	ms
		iCE40LP/HX8K - High Frequency	70	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

sysCONFIG Port Timing Specifications[1] (Continued)

Symbol	Parameter		Min.	Typ.	Max.	Units
t_{MCLK}	CRESET_B high to first MCLK edge	iCE40LP384 - Low Frequency (Default)	600	—	—	us
		iCE40LP384 - Medium Frequency	600	—	—	us
		iCE40LP384 - High Frequency	600	—	—	us
		iCE40LP640, iCE40LP/HX1K - Low Frequency (Default)	800	—	—	us
		iCE40LP640, iCE40LP/HX1K - Medium Frequency	800	—	—	us
		iCE40LP640, iCE40LP/HX1K - High Frequency	800	—	—	us
		iCE40LP/HX1K -Low Frequency (Default)	800	—	—	us
		iCE40LP/HX1K - Medium Frequency	800	—	—	us
		iCE40LP/HX1K - High Frequency	800	—	—	us
		iCE40LP/HX4K - Low Frequency (Default)	1200	—	—	us
		iCE40LP/HX4K - Medium Frequency	1200	—	—	us
		iCE40LP/HX4K - high frequency	1200	—	—	us
		iCE40LP/HX8K - Low Frequency (Default)	1200	—	—	us
		iCE40LP/HX8K - Medium Frequency	1200	—	—	us
		iCE40LP/HX8K - High Frequency	1200	—	—	us

1. Does not apply for NVCM.
2. Supported only with 1.2 V V_{CC} and at 25 °C.
3. Extended range f_{MAX} Write operations support up to 53 MHz only with 1.2 V V_{CC} and at 25 °C.

Switching Test Conditions

Figure 3-3 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-3.

Figure 3-3. Output Test Load, LVCMOS Standards

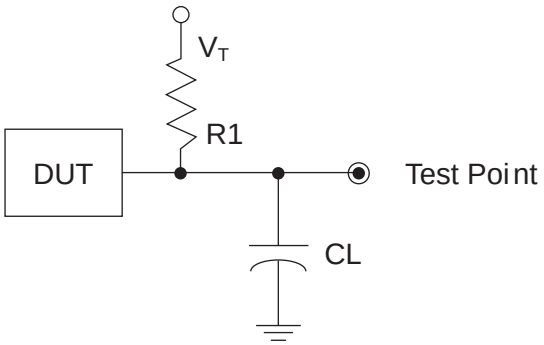

Table 3-3. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Reference	V_T
LVCMOS settings (L -> H, H -> L)	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
LVCMOS 3.3 (Z -> H)	188	0 pF	1.5	V_{OL}
LVCMOS 3.3 (Z -> L)			1.5	V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVCMOS (H -> Z)			V_{OH} - 0.15	V_{OL}
LVCMOS (L -> Z)			V_{OL} - 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
IO[Bank]_[Row/Column Number][A/B]	I/O	[Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number on the device.
IO[Bank]_[Row/Column Number][A/B]	I/O	[Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number on the device. [A/B] indicates the differential I/O. 'A' = negative input. 'B' = positive input.
HCIO[Bank]_[Number]	I/O	High Current IO. [Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number.
NC	—	No connect
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together.
VCC	—	VCC – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.
VCCIO_x	—	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. All VCCIOs located in the same bank are tied to the same supply.
PLL and Global Functions (Used as user-programmable I/O pins when not used for PLL or clock pins)		
VCCPLLx	—	PLL VCC – Power. Dedicated pins. The PLL requires a separate power and ground that is quiet and stable to reduce the output clock jitter of the PLL.
GNDPLLx	—	PLL GND – Ground. Dedicated pins. The sysCLOCK PLL has the DC ground connection made on the FPGA, so the external PLL ground connection (GNDPLL) must NOT be connected to the board's ground.
GBINx	—	Global pads. Two per side.
Programming and Configuration		
CBSEL[0:1]	I/O	Dual function pins. I/Os when not used as CBSEL. Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled.
CRESET_B	I	Configuration Reset, active Low. Dedicated input. No internal pull-up resistor. Either actively drive externally or connect a 10 KOhm pull-up resistor to VCCIO_2.
CDONE	I/O	Configuration Done. Includes a permanent weak pull-up resistor to VCCIO_2. If driving external devices with CDONE output, an external pull-up resistor to VCCIO_2 may be required. Refer to the TN1248, iCE40 Programming and Configuration for more details. Following device configuration the iCE40LP640 and iCE40LP1K in the SWG16 package CDONE pin can be used as a user output.
VCC_SPI	—	SPI interface voltage supply input. Must have a valid voltage even if configuring from NVCM.
SPI_SCK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA configuration modes.
SPI_SS_B	I/O	SPI Slave Select. Active Low. Includes an internal weak pull-up resistor to VCC_SPI during configuration. During configuration, the logic level sampled on this pin determines the configuration mode used by the iCE40 device. An input when sampled at the start of configuration. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in Master SPI Flash configuration mode.
SPI_SI	I/O	Slave SPI serial data input and master SPI serial data output
SPI_SO	I/O	Slave SPI serial data output and master SPI serial data input

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iCE40 LP/HX Family Data Sheet Ordering Information

March 2017 Data Sheet DS1040

iCE40 Part Number Description

Ultra Low Power (LP) Devices

ICE40LPXXX – XXXXXXX

Device Family
iCE40 FPGA

Series
LP = Low Power Series

Logic Cells
384 = 384 Logic Cells
640 = 640 Logic Cells
1K = 1,280 Logic Cells
4K = 3,520 Logic Cells
8K = 7,680 Logic Cells

Shipping Method
TR = Tape and Reel
TR50 = Tape and Reel 50 units
TR1K = Tape and Reel 1,000 units

Package
SWG16 = 16-Ball WLCSP (0.35 mm Pitch)
CM36 = 36-Ball ucBGA (0.4 mm Pitch)
CM49 = 49-Ball ucBGA (0.4 mm Pitch)
CM81 = 81-Ball ucBGA (0.4 mm Pitch)
CB81 = 81-Ball csBGA (0.5 mm Pitch)
CM121 = 121-Ball ucBGA (0.4 mm Pitch)
CB121 = 121-Ball csBGA (0.5 mm Pitch)
CM225 = 225-Ball ucBGA (0.4 mm Pitch)
SG32 = 32-Pin QFN (0.5 mm Pitch)
QN84 = 84-Pin QFN (0.5 mm Pitch)

High Performance (HX) Devices

ICE40HXXX – XXXXXXX

Device Family
iCE40 mobileFPGA

Series
HX = High-Performance Series

Logic Cells
1K = 1,280 Logic Cells
4K = 3,520 Logic Cells
8K = 7,680 Logic Cells

Shipping Method
TR = Tape and Reel

Package
CB132 = 132-Ball csBGA (0.5 mm Pitch)
CM225 = 225-Ball ucBGA (0.4 mm Pitch)
CT256 = 256-Ball caBGA (0.8 mm Pitch)
TQ144 = 144-Pin TQFP (0.5 mm Pitch)
VQ100 = 100-Pin VQFP (0.5 mm Pitch)
BG121 = 121-Ball caBGA (0.8 mm Pitch)

All parts shipped in trays unless noted.

Ordering Information

iCE40 devices have top-side markings as shown below:

Industrial

Note: Markings are abbreviated for small packages.

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Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40LP384-CM36	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM36TR	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM36TR1K	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM49	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-CM49TR	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-CM49TR1K	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-SG32	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP384-SG32TR	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP384-SG32TR1K	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP640-SWG16TR	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP640-SWG16TR50	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP640-SWG16TR1K	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR50	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR1K	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-CM36	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM36TR	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM36TR1K	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM49	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM49TR	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM49TR1K	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM81	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CM81TR	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CM81TR1K	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CB81	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CB81TR	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CB81TR1K	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CM121	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CM121TR	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CM121TR1K	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CB121	1280	1.2 V	Halogen-Free csBGA	121	IND
ICE40LP1K-QN84	1280	1.2 V	Halogen-Free QFN	84	IND
ICE40LP4K-CM81	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM81TR	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM81TR1K	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM121	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM121TR	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM121TR1K	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM225	3520	1.2 V	Halogen-Free ucBGA	225	IND
ICE40LP8K-CM81	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM81TR	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM81TR1K	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM121	7680	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP8K-CM121TR	7680	1.2 V	Halogen-Free ucBGA	121	IND

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40LP8K-CM121TR1K	7680	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP8K-CM225	7680	1.2 V	Halogen-Free ucBGA	225	IND

High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40HX1K-CB132	1280	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX1K-VQ100	1280	1.2 V	Halogen-Free VQFP	100	IND
ICE40HX1K-TQ144	1280	1.2 V	Halogen-Free TQFP	144	IND
ICE40HX4K-BG121	3520	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX4K-BG121TR	3520	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX4K-CB132	3520	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX4K-TQ144	3520	1.2 V	Halogen-Free TQFP	144	IND
ICE40HX8K-BG121	7680	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX8K-BG121TR	7680	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX8K-CB132	7680	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX8K-CM225	7680	1.2 V	Halogen-Free ucBGA	225	IND
ICE40HX8K-CT256	7680	1.2 V	Halogen-Free caBGA	256	IND

Date	Version	Section	Change Summary
April 2013	02.2	Introduction	Added the LP8K 81 ucBGA.
		Architecture	Corrected typos.
		DC and Switching Characteristics	Corrected typos. Added 7:1 LVDS waveforms.
		Pinout Information	Corrected typos in signal descriptions. Added the LP8K 81 ucBGA.
		Ordering Information	Added the LP8K 81 ucBGA.
March 2013	02.1	DC and Switching Characteristics	Recommended operating conditions added requirement for Master SPI.
			Updated Recommended Operating Conditions for V_{PP_2V5}.
			Updated Power-On-Reset Voltage Levels and sequence requirements.
			Updated Static Supply Current conditions.
			Changed unit for t_{SKEW_IO} from ns to ps.
			Updated range of CCLK f_{MAX}.
		Ordering Information	Updated ordering information to include tape and reel part numbers.
September 2012	02.0	—	Merged SiliconBlue iCE40 LP and HX data sheets and updated to Lattice format.
	01.31	—	Updated Table 1.
	01.3	—	Production release.
			Updated notes on Table 3: Recommended Operating Conditions.
			Updated values in Table 4, Table 5, Table 12, Table 13 and Table 17.
	01.21	—	Updated Figure 3 and Figure 4 to specify iCE40.
Aug 2012	01.2	—	Updated company name.
July 2011	01.1	—	Moved package specifications to iCE40 pinout Excel files.
			Updated Table 1 maximum I/Os.
	01.01	—	Added 640, 1K and 4K to Table 13 configuration times. Updated Table 1 maximum I/Os.
	01.0	—	Initial release.